

Features

- Measures Temperature Rate of Change Calculation with Preemptive Alert(s) Limits
- Up to Four External Temperature Monitors: $\pm 1^{\circ}\text{C}$ Maximum Accuracy
- Internal Temperature Sensor: $\pm 1^{\circ}\text{C}$ Maximum Accuracy
- Temperature Sensor Resolution (Internal/External): 0.125°C
- Resistor Programmable System Shutdown Temperature
- Configurable Alert Pins
- Operating Voltage: 1.62V to 3.6V
- Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Other Features: Auto-Beta Compensation, Configurable Ideality Factor, Hottest Diode Compare, Resistance Error Correction
- Available in 8-Lead 2x2 mm WDFN, 10-Lead 2.5x2.0 mm VDFN and 10-Lead MSOP Packages

Typical Applications

- Temperature-Sensitive Storage
- Industrial
- IoT for Low System Voltage
- Portable Electronics
- Handheld Gaming
- Computing
- Food Storage

Description

The EMC1822/23/24/25/43 devices are high-accuracy, two-wire (I²C) temperature sensors with resistor programmable system shutdown. These devices monitor up to five temperature channels. Advanced features, such as Resistance Error Correction (REC), beta compensation (to support CPU diodes requiring the BJT/Transistor model), and rate of temperature change measurement, combine to provide a robust solution for complex environmental monitoring applications.

This device family introduces Rate of Change (ROC) temperature measurement with associated alerts. This provides a preemptive system alert and an additional protective measurement layer to catch and manage variable system temperatures.

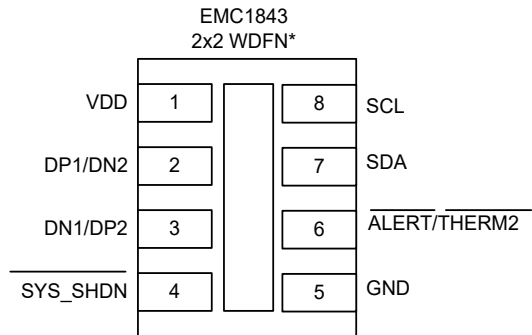
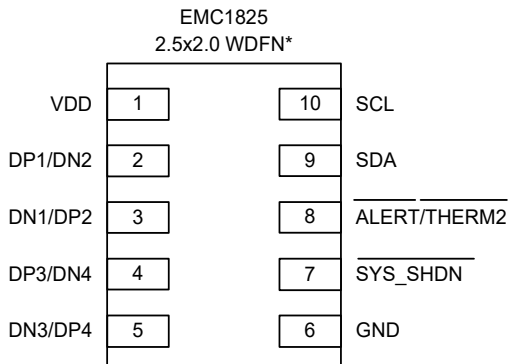
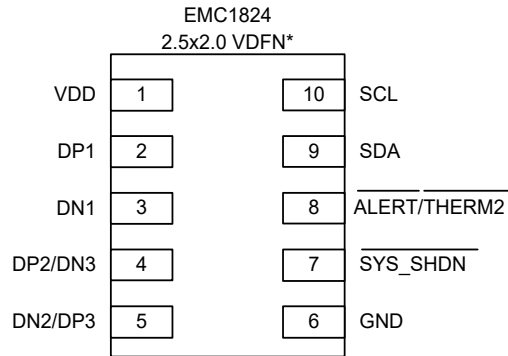
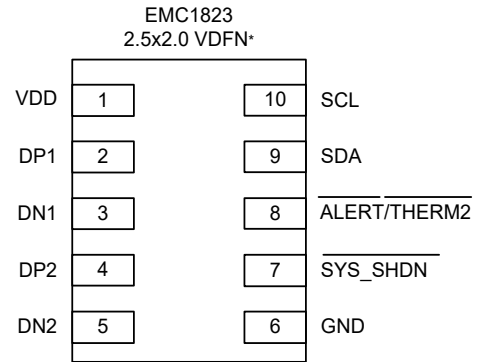
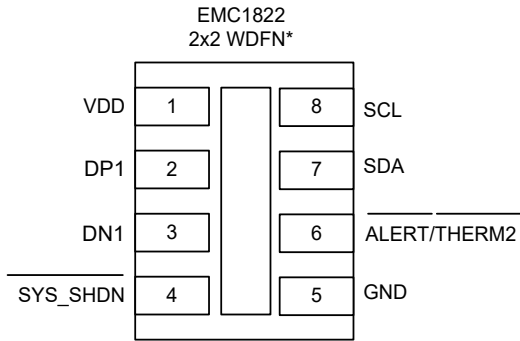
The Resistance Error Correction feature automatically eliminates the temperature error caused by series resistance, allowing for greater flexibility in routing thermal diodes. Beta compensation eliminates temperature errors caused by low, variable beta transistors common in current fine geometry processors. The automatic beta detection feature determines the optimal sensor external diode/transistor settings, freeing the user from providing unique sensor configurations for each temperature monitoring application. These advanced features, along with $\pm 1^{\circ}\text{C}$ measurement accuracy for both external and internal diode temperatures, provide a low-cost, highly flexible and accurate solution for critical temperature monitoring applications.

Table of Contents

| | |
|---|----|
| Features..... | 1 |
| Typical Applications..... | 1 |
| Description..... | 2 |
| 1. Package Types..... | 5 |
| 2. Functional Block Diagram..... | 6 |
| 3. Electrical Characteristics..... | 7 |
| 3.1. Absolute Maximum Ratings..... | 7 |
| 4. Typical Operating Curves..... | 10 |
| 5. Pin Descriptions..... | 11 |
| 5.1. Power Supply (V_{DD})..... | 12 |
| 5.2. Diode 1 Pair (DN1/DP1)..... | 12 |
| 5.3. System Shutdown..... | 12 |
| 5.4. Ground (GND)..... | 12 |
| 5.5. Maskable ALERT ($\overline{\text{ALERT/THERM2}}$)..... | 12 |
| 5.6. SMBus/I ² C Data (SDA)..... | 12 |
| 5.7. DP/DP1..... | 12 |
| 5.8. DN/DN1..... | 12 |
| 5.9. DP2..... | 12 |
| 5.10. DN2..... | 12 |
| 5.11. Anti-Parallel Diode Pair (DP2/DN3 and DN2/DP3)..... | 12 |
| 5.12. Anti-Parallel Diode Pair (DP1/DN2 and DN1/DP2)..... | 12 |
| 5.13. Anti-Parallel Diode Pair (DP3/DN4 and DN3/DP4)..... | 13 |
| 5.14. SMBus Clock (SCL)..... | 13 |
| 5.15. Exposed Thermal Pad (EP)..... | 13 |
| 6. Detailed Description..... | 14 |
| 7. System Block Diagram..... | 15 |
| 7.1. Temperature Measurement..... | 15 |
| 7.2. Temperature Measurement Results and Data..... | 15 |
| 7.3. Limit Registers..... | 16 |
| 7.4. Limit Register Interaction..... | 16 |
| 7.5. $\overline{\text{ALERT/THERM2}}$ Output..... | 17 |
| 7.6. System Shutdown..... | 17 |
| 7.7. External Diode Connections..... | 19 |
| 7.8. Power States..... | 20 |
| 7.9. Conversion Rates..... | 20 |
| 7.10. Dynamic Averaging..... | 20 |
| 7.11. Digital Filter..... | 21 |
| 7.12. Beta Compensation..... | 22 |
| 7.13. Resistance Error Correction (REC)..... | 23 |
| 7.14. Programmable External Diode Ideality Factor..... | 23 |

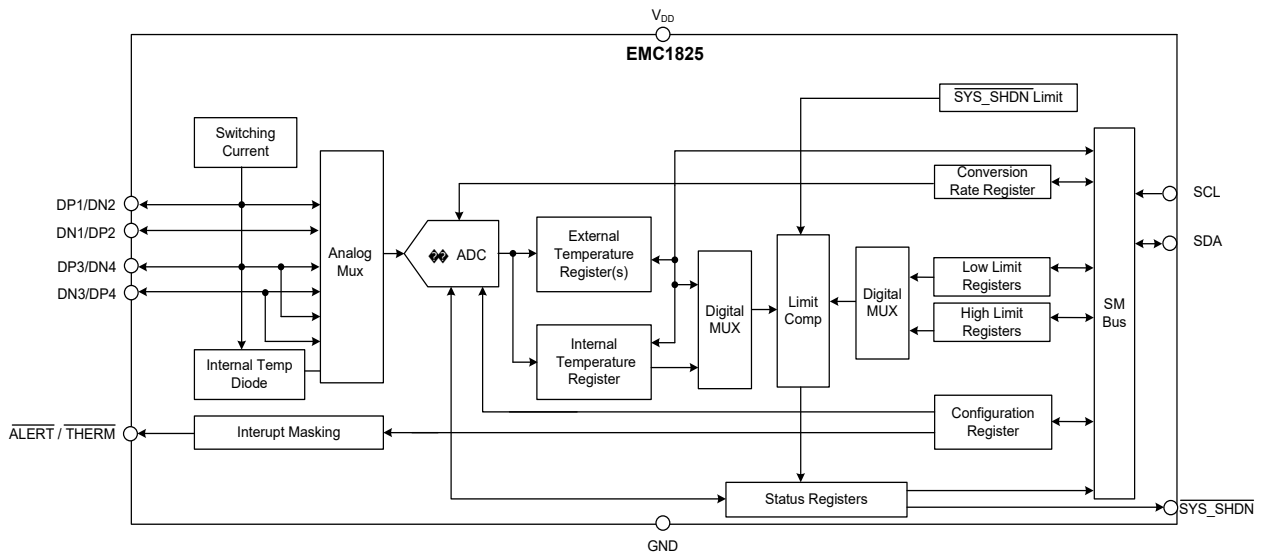
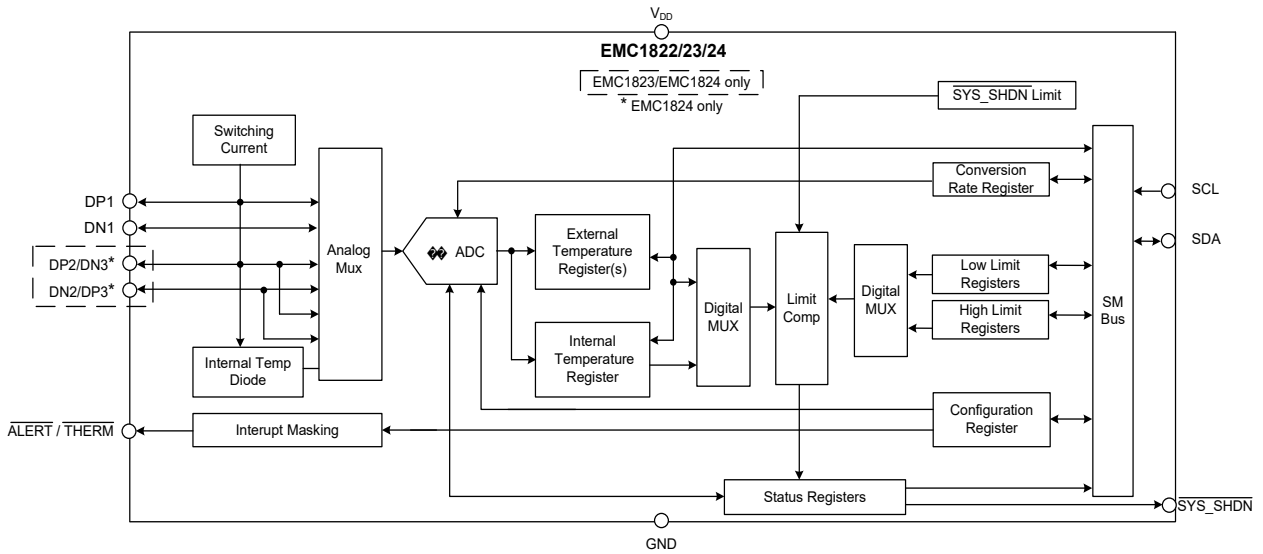
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|--|----|
| 7.15. Diode Faults..... | 24 |
| 7.16. Consecutive Alerts..... | 25 |
| 7.17. "Hottest Of" Comparison..... | 27 |
| 7.18. Rate of Change..... | 27 |
| 8. System Management Bus Protocol..... | 30 |
| 8.1. SMBus Start Bit..... | 30 |
| 8.2. SMBus Address and RD/ $\overline{\text{WR}}$ Bit..... | 30 |
| 8.3. SMBus Data Bytes..... | 30 |
| 8.4. SMBus ACK and NACK Bits..... | 30 |
| 8.5. SMBus Stop Bit..... | 30 |
| 8.6. SMBus Time-out..... | 30 |
| 8.7. SMBus and I ² C Compliance..... | 31 |
| 8.8. SMBus Protocols..... | 31 |
| 8.9. $\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ Pin Considerations..... | 32 |
| 8.10. Register Summary | 34 |
| 8.11. Data Read Interlock..... | 36 |
| 9. Packaging Information..... | 89 |
| 9.1. Package Marking Information..... | 89 |
| 10. Product Identification System..... | 96 |
| 11. Revision History..... | 97 |
| Microchip Information..... | 98 |
| Trademarks..... | 98 |
| Legal Notice..... | 98 |
| Microchip Devices Code Protection Feature..... | 98 |

1. Package Types



Note: * Includes Exposed Thermal Pad (EP); see [Pin Descriptions](#)

2. Functional Block Diagram



3. Electrical Characteristics

3.1. Absolute Maximum Ratings

| | |
|--|--------------------|
| V _{DD} | 4.0V |
| Voltage at all Input/ Output Pins | GND – 0.3V to 4.0V |
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature with Power Applied | -40°C to +125°C |
| Junction Temperature (T _J) | +150°C |
| ESD Protection on All Pins (HBM:MM) | (8 kV:400V) |
| Latch-up Current at Each Pin (+25°C) | ±200 mA |

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to conditions above the maximum ratings for extended periods may affect device reliability.

Table 3-1. DC Characteristics

Electrical Specifications: Unless otherwise specified, all limits apply for typical values at ambient temperature
1.62V ≤ V_{DD} ≤ +3.6V at -40°C ≤ T_A ≤ +125°C

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|----------------------------------|--------------------|------|-------|------|-------|--|
| Supply Voltage | V _{DD} | 1.62 | — | 3.6 | V | |
| Supply Current | I _{DD} | — | 20 | 80 | μA | 0.0625 conversion/second, dynamic averaging disabled |
| | | — | 25 | 164 | μA | 1 conversion/second, dynamic averaging disabled |
| | | — | 205 | 432 | μA | 4 conversions/second, dynamic averaging disabled |
| | | — | 800 | — | μA | > 16 conversions/second, dynamic averaging enabled |
| Standby Supply Current | I _{DD_OS} | — | 15 | 75 | μA | Device in One-Shot state, no active I ² C communications, ALERT and THERM pins not asserted |
| Power-on Reset Release Voltage | PORR | — | 1.45 | — | V | Rising V _{DD} |
| Power-up Timer | tPWRT | — | 15 | — | ms | |
| V _{DD} Rise Rate | VDD_RISE | 0.05 | — | — | V/ms | 0 to 2.75V in ~ 60 ms |
| Internal Temperature Monitor | | | | | | |
| Temperature Accuracy | — | — | ±0.25 | ±1 | °C | |
| External Temperature Monitor | | | | | | |
| Temperature Accuracy - 8-Lead | — | — | ±0.25 | ±1 | °C | -20°C < T _A < 105°C, -40°C < T _D < +125°C, 2N3904 |
| | | — | ±0.25 | ±1.5 | °C | -40°C < T _A < +125°C, -40°C < T _D < +125°C, 2N3904 |

Table 3-1. DC Characteristics (continued)

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|--|---------------------|---------------------|----------------------|---------------------|-------|---|
| Temperature Accuracy - 10-Lead | — | — | ±0.25 | ±1 | °C | -20°C < T _A < 125°C, -40°C < T _D < +125°C, 2N3904 |
| | | — | ±0.25 | ±1.5 | °C | -40°C < T _A < +125°C, -40°C < T _D < +125°C, 2N3904 |
| Temperature Resolution | — | — | 0.125 | — | °C | |
| Timing and Capacitive Filter | | | | | | |
| Time to First Communications | t _{INT_T} | — | 15 | 20 | ms | Time after power-up before ready to begin communications and measurement |
| Conversion Time per Channel | t _{CONV} | — | 25 | — | ms | Default settings |
| Time to First Conversion from One-Shot | | — | 5 | — | ms | |
| Time to First Conversion from Standby | t _{CONV1} | — | 220 | — | ms | Default settings |
| Capacitive Filter | C _{FILTER} | — | 2.2 | 2.7 | nF | Connected across external diode |
| ALERT and THERM Pins | | | | | | |
| Output Low Voltage | V _{OL} | 0.4 | — | — | V | I _{SINK} = 8 mA |
| Leakage Current | I _{LEAK} | — | — | ±5 | µA | ALERT and THERM pins, device powered, pull-up voltage < 3.6V |
| SCL and SDA | | | | | | |
| Input | | | | | | |
| High-Level Voltage | V _{IH} | 0.7 V _{DD} | — | — | V | |
| Low-Level Voltage | V _{IL} | — | — | 0.3 V _{DD} | V | |
| Input Current | I _{IN} | — | — | ±5 | µA | SDA and SCL only |
| Output (SDA only) | | | | | | |
| Low-Level Voltage | V _{OL} | — | — | 0.4 | V | I _O = 20 mA, V _{DD} = 1.7V to 3.6V |
| High-Level Current (leakage) | I _{OH} | — | — | 1 | µA | V _{OH} = V _{DD} |
| Low-Level Current | I _{OL} | — | — | 20 | mA | V _{OL} = 0.4V, V _{DD} = 1.62V to 3.6V |
| Capacitance | C _{IN} | — | 5 | — | pF | |
| SDA and SCL Inputs | | | | | | |
| Hysteresis | V _{HYST} | — | 0.05 V _{DD} | — | V | |

Table 3-2. Thermal Specifications

Electrical Characteristics: Unless otherwise specified, 1.62V ≤ V_{DD} ≤ 3.6V at -40°C ≤ T_A ≤ +125°C

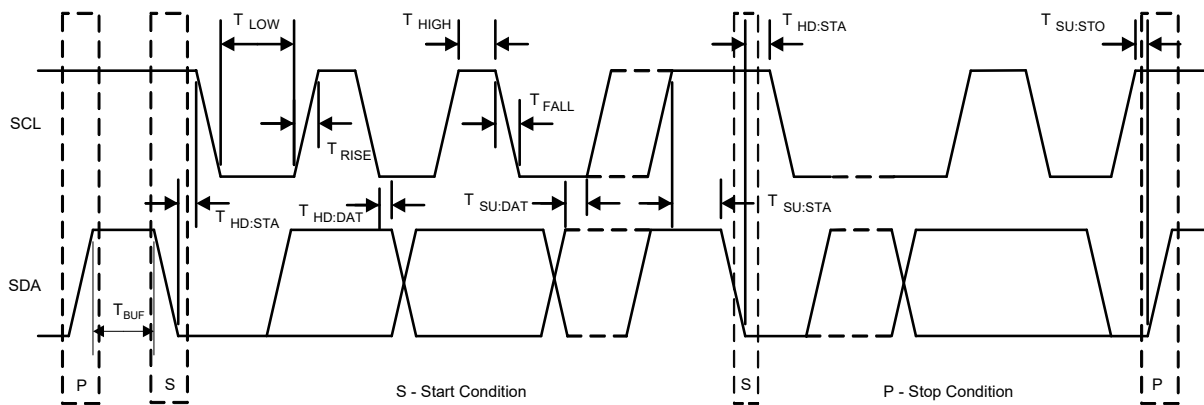
| Parameters | Sym. | Min. | Typ. | Max. | Units | Test Conditions |
|--|-----------------|------|-------|------|-------|--|
| Temperature Ranges | | | | | | |
| Specified Temperature Range | T _A | -40 | — | +125 | °C | |
| Operating Temperature Range | T _A | -40 | — | +125 | °C | |
| Storage Temperature Range | T _A | -65 | — | +125 | °C | |
| Thermal Package Resistances | | | | | | |
| Thermal Resistance, 8-Lead WDFN, 2x2 mm | θ _{JA} | — | 141.3 | — | °C/W | JEDEC 2s2p, board size 76.2 x 114.3 x 1.6 mm, one thermal via, airflow = 0 m/s |
| Thermal Resistance, 10-Lead VDFN, 2.5x2.0 mm | θ _{JA} | — | 78 | — | °C/W | |
| Thermal Resistance, 10-Lead MSOP, 3x3 mm | θ _{JA} | — | 132.2 | — | °C/W | |

Table 3-3. SMBus Module Specifications

Operating Conditions: Unless otherwise indicated, $1.62V \leq V_{DD} \leq 3.6V$ at $-40^{\circ}C \leq T_A \leq +85^{\circ}C$

| Characteristic | Sym. | Min. | Typ. | Max. | Units | Conditions |
|-----------------------------|---------------|------|------|------|---------|-------------------------------|
| SMBus Timing | | | | | | |
| Clock Frequency | f_{SMB} | 10 | — | 400 | kHz | |
| Spike Suppression | t_{SP} | — | — | 50 | ns | |
| Bus Free Time Stop to Start | t_{BUF} | 1.3 | — | — | μs | |
| Hold Time: Start | $t_{HD:STA}$ | 0.6 | — | — | μs | |
| Setup Time: Start | $t_{SU:STA}$ | 0.6 | — | — | μs | |
| Setup Time: Stop | $t_{SU:STO}$ | 0.6 | — | — | μs | |
| Data Hold Time | $t_{HD:DAT}$ | 0 | — | — | μs | When transmitting to the host |
| Data Hold Time | $t_{HD:DAT}$ | 0 | — | — | μs | When receiving from the host |
| Data Setup Time | $t_{SU:DAT}$ | 100 | — | — | ns | |
| Clock Low Period | t_{LOW} | 1.3 | — | — | μs | |
| Clock High Period | t_{HIGH} | 0.6 | — | — | μs | |
| Clock/Data Fall Time | t_{FALL} | — | — | 300 | ns | Min = $20 + 0.1 C_{LOAD}$ ns |
| Clock/Data Rise Time | t_{RISE} | — | — | 300 | ns | Min = $20 + 0.1 C_{LOAD}$ ns |
| Capacitive Load | C_{LOAD} | — | — | 400 | pF | Per bus line |
| Time-out | $t_{TIMEOUT}$ | 25 | — | 35 | ms | Disabled by default |

Figure 3-1. SMBus Timing Diagram



4. Typical Operating Curves

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (for example, outside specified power supply range) and therefore outside the warranted range.

Figure 4-1. Internal Temperature Error vs. Ambient Temperature ($V_{DD} = 2.5V$, $T_D = +25^\circ C$, 2N3904)

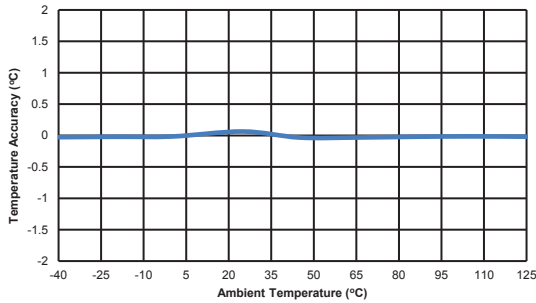


Figure 4-2. Temperature Accuracy vs. Remote Diode Temperature, $V_{DD} = 1.8V$

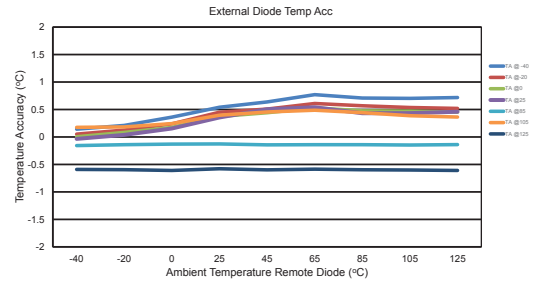


Figure 4-3. Temperature Error vs. Filter Capacitor ($V_{DD} = 2.5V$, $T_A = T_D = +25^\circ C$, 2N3904)

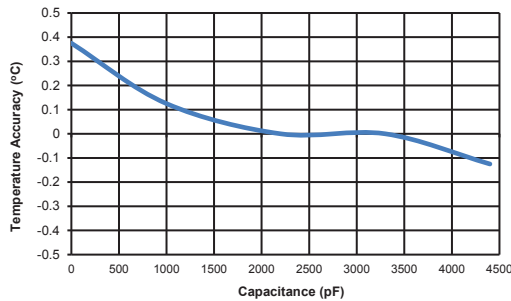


Figure 4-4. Temperature Error vs. Series Resistance ($T_A = +25^\circ C$, $V_{DD} = 1.8V$)

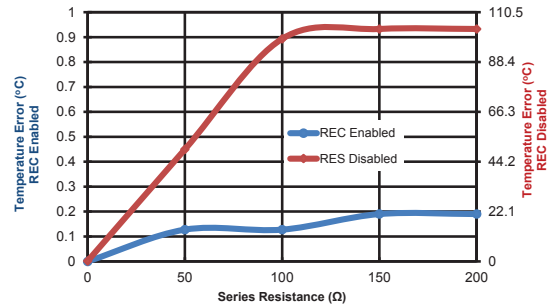


Figure 4-5. I_{DD} vs. V_{DD} Across Temperature

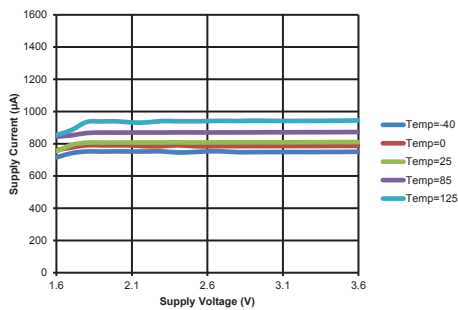
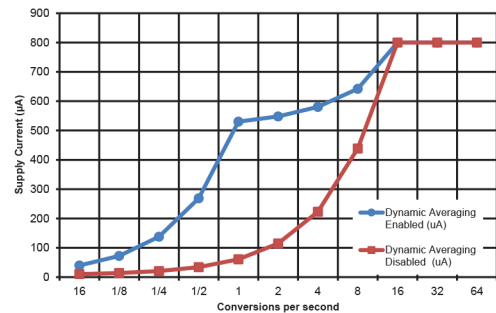


Figure 4-6. Supply Current vs. Conversion Rate ($T_A = +25^\circ C$, $V_{DD} = 1.8V$)



5. Pin Descriptions

The EMC1822/23/24/25/43 has five variants that include features unique to each device. Refer to the table to determine applicability of the pin descriptions.

The description of the pins is listed in the following table.

Table 5-1. Pin Function Table

| Pin Name | EMC1822 | EMC1823 | EMC1824 | EMC1825 | EMC1843 | Pin Type | Description |
|-----------------|---------|---------|---------|---------|---------|----------|----------------------------|
| V _{DD} | 1 | 1 | 1 | 1 | 1 | P | Power |
| GND | 5 | 6 | 6 | 6 | 5 | P | Ground |
| ALERT/THERM2 | 6 | 8 | 8 | 8 | 6 | OD | I ² C alert pin |
| SYS_SHDN | 4 | 7 | 7 | 7 | 4 | OD | System shutdown |
| SDA | 7 | 9 | 9 | 9 | 7 | OD | I ² C data |
| SCL | 8 | 10 | 10 | 10 | 8 | OD | I ² C clock |
| DP1 | 2 | 2 | 2 | — | — | A | Diode 1 connection |
| DN1 | 3 | 3 | 3 | — | — | A | Diode 1 connection |
| DP2 | — | 4 | — | — | — | A | Diode 2 connection |
| DN2 | — | 5 | — | — | — | A | Diode 2 connection |
| DP2/DN3 | — | — | 4 | — | — | A | Diode 2/3 connection |
| DN2/DP3 | — | — | 5 | — | — | A | Diode 2/3 connection |
| DP1/DN2 | — | — | — | 2 | 2 | A | Diode 1/2 connection |
| DN1/DP2 | — | — | — | 3 | 3 | A | Diode 1/2 connection |
| DP3/DN4 | — | — | — | 4 | — | A | Diode 3/4 connection |
| DN3/DP4 | — | — | — | 5 | — | A | Diode 3/4 connection |

Legend: P = Power pin; A = Analog pin; OD = Open-Drain pin

5.1. Power Supply (V_{DD})

This pin is used to supply power to the device.

5.2. Diode 1 Pair (DN1/DP1)

Remote Diode 1 anode (DP1) and cathode (DN1) pins.

5.3. System Shutdown

The EMC1822/23/24/25/43 devices contain a hardware configured temperature limit circuit that controls the $\overline{SYS_SHDN}$ pin. The threshold temperature is determined by the pull-up resistors on both the $\overline{SYS_SHDN}$ and \overline{ALERT} pins. Note, Standby and One-Shot modes cannot be enabled in device configurations including system shutdown functionality .

The final temperature decode is the responsibility of the digital block. The overall decode is shown in [Table 7-3](#).

The hardware shutdown circuitry measures the External Diode 1 channel and compares it against the hardware thermal shutdown limit. The \overline{THERM} pin consecutive alert counter (default 4 for the $\overline{SYS_SHDN}$ pin) applies to this comparison. If the temperature meets or exceeds the limit for the number of consecutive measurements, the $\overline{SYS_SHDN}$ pin is asserted. The $\overline{SYS_SHDN}$ pin remains asserted until the temperature drops below the limit minus 10°C. As well, all of the measurement channels (including the External Diode 1 channel) can be configured to assert the $\overline{SYS_SHDN}$ pin. If a channel is configured to assert the $\overline{SYS_SHDN}$ pin, the temperature on the measured channel must exceed the programmed therm limit value. This is treated in the same way as the \overline{THERM} output.

5.4. Ground (GND)

This pin is used to ground the device.

5.5. Maskable ALERT ($\overline{ALERT/THERM2}$)

This pin asserts when a diode temperature exceeds the ALERT threshold. This pin can be masked by register settings.

5.6. SMBus/I²C Data (SDA)

This is the open-drain, bidirectional data pin for SMBus communication.

5.7. DP/DP1

- DP/DP1: DP and DP1 anode

5.8. DN/DN1

- DN/DN1: DN and DN1 cathode

5.9. DP2

- DP2: DP2 anode

5.10. DN2

- DN2: DN2 cathode

5.11. Anti-Parallel Diode Pair (DP2/DN3 and DN2/DP3)

- DP2/DN3: DP2 anode and DN3 cathode
- DN2/DP3: DN2 cathode and DP3 anode

5.12. Anti-Parallel Diode Pair (DP1/DN2 and DN1/DP2)

- DP1/DN2: DP1 anode and DN2 cathode
- DN1/DP2: DN1 cathode and DP2 anode

5.13. Anti-Parallel Diode Pair (DP3/DN4 and DN3/DP4)

- DP3/DN4: DP3 anode and DN4 cathode
- DN3/DP4: DN3 cathode and DP4 anode

5.14. SMBus Clock (SCL)

This is the SMBus/I²C input clock pin for SMBus communication.

5.15. Exposed Thermal Pad (EP)

There is no internal connection between the Exposed Thermal Pad (EP) and the GND pin. They must be connected to the same electric potential on the Printed Circuit Board (PCB). Grounding is recommended for mechanical support.

6. Detailed Description

The EMC1822/23/24/25/43 devices monitor one internal diode and up to four externally connected temperature diodes.

Thermal management is performed in cooperation with a host device. This involves the host reading the temperature data from both the external and internal temperature diodes of the EMC1822/23/24/25/43 and using that data to manage thermal events or control the speed of one or more fans.

This device family introduces Rate of Change temperature measurement with associated alerts. This provides a preemptive system alert and an additional protective measurement layer to catch and manage variable system temperatures. Resistance Error Correction automatically eliminates the temperature error caused by series resistance. This feature allows for routing long traces and off-board connections with wires, if desired. Automatic beta compensation eliminates the need for substrate diode and transistor configurations.

The EMC1822/23/24/25/43 family has two levels of monitoring. The first level provides a maskable $\overline{\text{ALERT}}$ signal to the host when the measured temperatures exceed user-programmable limits. This allows the EMC1822/23/24/25/43 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host. The second level of monitoring provides a nonmaskable interrupt on the $\overline{\text{THERM}}$ pin if the measured temperatures meet or exceed a second programmable limit.

The EMC1822 is a single-channel remote temperature sensor, while the EMC1823 is a dual-channel remote temperature sensor. The remote channels for this selection of devices can support substrate diodes, discrete diode-connected transistors or CPU/GPU thermal diodes.

The EMC1824 supports Anti-Parallel Diode (APD) only on one channel. For the channel that does not support APD functionality, substrate diodes, discrete diode-connected transistors or CPU/GPU thermal diodes are supported. For the channel that supports APD, only discrete diode-connected transistors may be implemented. However, if APD is disabled on the EMC1824, then the channel that supports APD will be functional with substrate diodes, discrete diode-connected transistors and CPU/GPU thermal diodes.

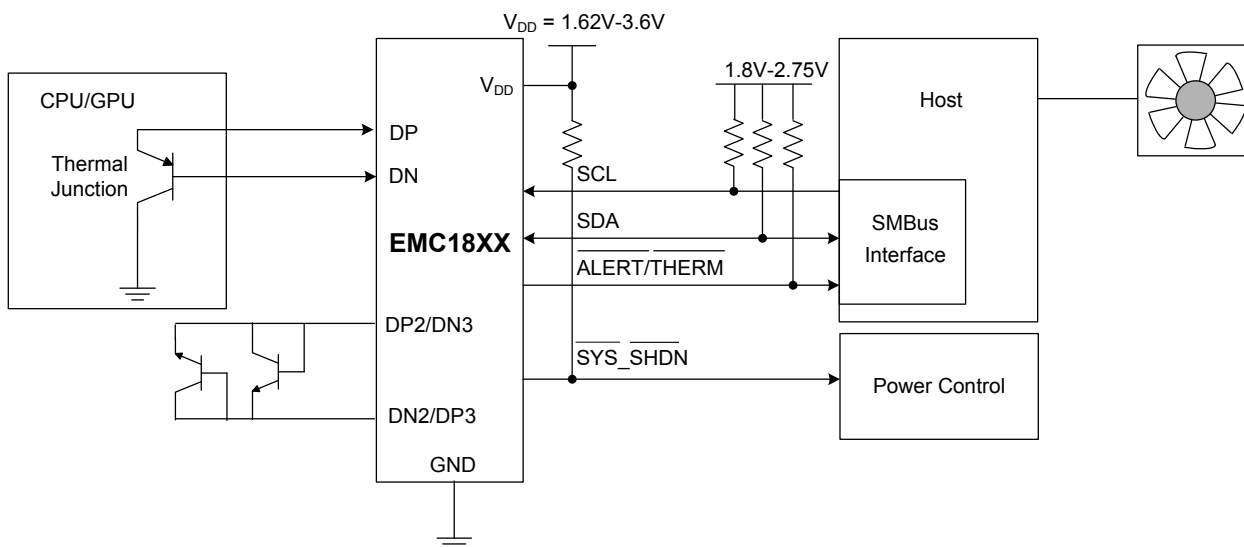
The EMC1825 and EMC1843 support APD on all channels. When APD is enabled, the channels support only diode-connected transistors. If APD is disabled, then the channels will support substrate transistors, discrete diode-connected transistors and CPU/GPU thermal diodes.

Note: Disabling APD functionality to implement substrate diodes on devices that support APD eliminates the benefit of APD (two diodes on one channel).

7. System Block Diagram

The figure below shows a system-level block diagram of the EMC1822/23/24/25/43.

Figure 7-1. EMC1822/23/24/25/43 System Diagram



7.1. Temperature Measurement

The EMC1822/23/24/25/43 device family can monitor the temperature of up to four externally connected diodes. Each external diode channel is configured with Resistance Error Correction and beta compensation based on user settings and system requirements.

The devices contain programmable high, low and therm limits for all measured temperature channels. If the measured temperature goes below the low limit or above the high limit, the $\overline{\text{ALERT}}$ pin can be asserted (based on user settings). If the measured temperature meets or exceeds the therm limit, the $\overline{\text{THERM}}$ pin is asserted unconditionally, providing two tiers of temperature detection.

7.2. Temperature Measurement Results and Data

The temperature measurement results are stored in the internal and external Temperature registers. These are then compared with the values stored in the High and Low Limit registers. Both external and internal temperature measurements are stored in an 11-bit format, with the eight Most Significant bits (MSBs) stored in a high byte register and the three Least Significant bits (LSBs) stored in the three MSB positions of the low byte register. All other bits of the low byte register are set to zero.

The EMC1822/23/24/25/43 family has two selectable temperature ranges. The default range is from 0°C to +127°C and the temperature is represented as a binary number able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended range is from -64°C to +191°C. The data format is a binary number offset by 64°C. The extended range is used to measure temperature diodes with a large known offset (such as CPU/GPU processor diodes), where the diode temperature plus the offset would be equivalent to a temperature higher than +127°C.

Table 7-1 shows the default and extended range formats.

Table 7-1. Temperature Data Format

| Temperature (°C) | Default Range 0°C to 127°C | Extended Range -64°C to +191°C |
|------------------|----------------------------|--------------------------------|
| Diode Fault | 000 0000 0000 | 000 0000 0000 |
| -64 | 000 0000 0000 | 000 0000 0000 (Note 1) |
| -1 | 000 0000 0000 | 001 1111 1000 |
| 0 | 000 0000 0000 (Note 2) | 010 0000 0000 |
| 0.125 | 000 0000 0001 | 010 0000 0001 |
| 1 | 000 0000 1000 | 010 0000 1000 |
| 64 | 010 0000 0000 | 100 0000 0000 |
| 65 | 010 0000 1000 | 100 0000 1000 |
| 127 | 011 1111 1000 | 101 1111 1000 |
| 127.875 | 011 1111 1111 | 101 1111 1111 |
| 128 | 011 1111 1111 (Note 3) | 110 0000 0000 |
| 190 | 011 1111 1111 | 111 1111 0000 |
| 191 | 011 1111 1111 | 111 1111 1000 |
| ≥ 191.875 | 011 1111 1111 | 111 1111 1111 (Note 4) |

Notes:

1. In the extended range, all temperatures below -64°C are reported as -64°C.
2. In Default mode, all temperatures below 0°C are reported as 0°C.
3. For the default range, all temperatures above +127.875°C are reported as +127.875°C.
4. For the extended range, all temperatures above +191.875°C are reported as +191.875°C.

7.3. Limit Registers

The device contains both high and low limits for all temperature channels. If the measured temperature exceeds the high limit, then the corresponding status bit is set and the $\overline{\text{ALERT}}$ pin is asserted. Likewise, if the measured temperature is less than or equal to the low limit, the corresponding status bit is set and the $\overline{\text{ALERT}}$ pin is asserted.

The data format for the limits must match the selected data format for the temperature. Therefore, if the extended temperature range is used, the limits must be programmed in the extended data format.

The Limit registers with multiple addresses are fully accessible at either address.

When the device is in the Standby state, updating the Limit registers will have no effect until the next conversion cycle occurs. This can be initiated via a write to the ONE SHOT register (Address 0Fh; [ONE SHOT](#)) or by clearing the RUN/STANDBY bit (see [CONFIG](#), Address 03h).

7.4. Limit Register Interaction

The various Limit registers in the device interact based on both external conditions present on the diode pins, as well as changes in register bits in the I²C interface.

7.4.1. High Limit Register

The High Limit Status register contains the status bits that are set when a temperature channel high limit is exceeded. If any of these bits are set, the HIGH Status bit in the Status register is also set. Reading from the High Limit Status register clears all bits. Reading from the register will also clear the HIGH Status bit in the Status register.

The $\overline{\text{ALERT}}$ pin will be set if the programmed number of consecutive alert counts has been met and any of these status bits are set.

The status bits remain set until a read is performed, unless the $\overline{\text{ALERT}}$ pin is configured as a comparator output (see [ALERT/THERM2 Pin in Therm Mode](#)).

7.4.2. Low Limit Register

The Low Limit Status register contains the status bits that are set when a temperature channel drops below the low limit. If any of these bits are set, then the LOW Status bit in the Status register is set. Reading from the Low Limit Status register clears all bits.

The $\overline{\text{ALERT}}$ pin will be set if the programmed number of consecutive alert counts has been met and any of these status bits are set.

The status bits will remain set until a read is performed, unless the $\overline{\text{ALERT}}$ pin is configured as a comparator output (see [ALERT/THERM2 Pin in Therm Mode](#)).

7.4.3. Therm Limit Register

The Therm Limit registers are used to determine whether a critical thermal event has occurred. If the measured temperature exceeds the therm limit, the $\overline{\text{THERM}}$ pin is asserted. The limit setting must match the chosen data format of the temperature reading registers.

Unlike the $\overline{\text{ALERT}}$ pin, the $\overline{\text{THERM}}$ pin cannot be masked. Additionally, the $\overline{\text{THERM}}$ pin is released once the temperature drops below the corresponding threshold, minus the Therm Hysteresis.

7.5. $\overline{\text{ALERT/THERM2}}$ Output

The $\overline{\text{ALERT/THERM2}}$ pin is an open-drain output and requires a pull-up resistor to V_{DD} . It has two modes of operation: Interrupt mode and Comparator mode. The mode of the $\overline{\text{ALERT/THERM2}}$ output is selected through the $\overline{\text{ALERT/THERM2}}$ bit (see [CONFIG](#), Address 03h).

7.5.1. $\overline{\text{ALERT/THERM2}}$ Pin Interrupt Mode

When configured to operate in Interrupt mode, the $\overline{\text{ALERT/THERM2}}$ pin asserts low when an out-of-limit measurement (less than or equal to the low limit or greater than the high limit) is detected on any diode or when a diode fault is detected. The $\overline{\text{ALERT/THERM2}}$ pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been resolved, the $\overline{\text{ALERT/THERM2}}$ pin remains asserted until the appropriate status bits are cleared.

The $\overline{\text{ALERT/THERM2}}$ pin can be masked by setting the MASK_ALL bit. Once the $\overline{\text{ALERT/THERM2}}$ pin has been masked, it is deasserted and remains so until the MASK_ALL bit is cleared by the user. Any interrupt conditions that occur while the $\overline{\text{ALERT/THERM2}}$ pin is masked causes the Status register to be updated normally. There are also individual channel masks (see [DIODE FAULT MASK](#)).

The $\overline{\text{ALERT/THERM2}}$ pin is used as an interrupt signal or as an I²C alert signal that allows an SMBus/I²C client to communicate an error condition to the host. One or more $\overline{\text{ALERT/THERM2}}$ outputs can be hard-wired together.

7.5.2. $\overline{\text{ALERT/THERM2}}$ Pin in Therm Mode

When the $\overline{\text{ALERT/THERM2}}$ pin is configured to operate in Therm mode, it becomes asserted if any of the measured temperatures exceed the respective high limit. The $\overline{\text{ALERT/THERM2}}$ pin remains asserted until all temperatures drop below the corresponding high limit, minus the Therm Hysteresis value.

When the $\overline{\text{ALERT/THERM2}}$ pin is asserted in Therm mode, the corresponding High Limit Status bits are set. Reading these bits does not clear them until the $\overline{\text{ALERT/THERM2}}$ pin is deasserted. Once the $\overline{\text{ALERT/THERM2}}$ pin is deasserted, the status bits are automatically cleared.

The MASK_ALL bit does not block the $\overline{\text{ALERT/THERM2}}$ pin in this mode; however, the individual channel masks prevent the respective channel from asserting the $\overline{\text{ALERT/THERM2}}$ pin.

7.6. System Shutdown

The EMC1822/23/24/25/43 devices contain a hardware configured temperature limit circuit that controls the $\overline{\text{SYS_SHDN}}$ pin. The threshold temperature is determined by the pull-up resistors on both the $\overline{\text{SYS_SHDN}}$ and $\overline{\text{ALERT}}$ pins. Note, Standby and One-shot modes cannot be enabled in device configurations, including system shutdown functionality.

Table 7-2. Pull-Up Resistor Values

| Pull-up Resistor ($\pm 1\%$) | Bit 2 | Bit 1 | Bit 0 |
|--------------------------------|-------|-------|-------|
| 4.7k | 0 | 0 | 0 |
| 6.8k | 0 | 0 | 1 |
| 10k | 0 | 1 | 0 |
| 15.8k | 0 | 1 | 1 |
| 20k | 1 | 0 | 0 |
| 47k | 1 | 0 | 1 |

The final temperature decode is the responsibility of the digital block. The overall decode is shown in [Table 7-3](#).

Table 7-3. Temperature Select Encoding

| SYS_SHDN Pull-up Decode | | | ALERT Pull-up Decode | | | Combined Decode (HEX) | Threshold Temperature |
|-------------------------|---|---|----------------------|---|---|-----------------------|-----------------------|
| 2 | 1 | 0 | 2 | 1 | 0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 00h | 77°C |
| 0 | 0 | 0 | 0 | 0 | 1 | 01h | 78°C |
| 0 | 0 | 0 | 0 | 1 | 0 | 02h | 79°C |
| 0 | 0 | 0 | 0 | 1 | 1 | 03h | 80°C |
| 0 | 0 | 0 | 1 | 0 | 0 | 04h | 81°C |
| 0 | 0 | 0 | 1 | 0 | 1 | 05h | 82°C |
| 0 | 0 | 1 | 0 | 0 | 0 | 08h | 83°C |
| 0 | 0 | 1 | 0 | 0 | 1 | 09h | 84°C |
| 0 | 0 | 1 | 0 | 1 | 0 | 0Ah | 85°C |
| 0 | 0 | 1 | 0 | 1 | 1 | 0Bh | 86°C |
| 0 | 0 | 1 | 1 | 0 | 0 | 0Ch | 87°C |
| 0 | 0 | 1 | 1 | 0 | 1 | 0Dh | 88°C |
| 0 | 1 | 0 | 0 | 0 | 0 | 10h | 89°C |
| 0 | 1 | 0 | 0 | 0 | 1 | 11h | 90°C |
| 0 | 1 | 0 | 0 | 1 | 0 | 12h | 91°C |
| 0 | 1 | 0 | 0 | 1 | 1 | 13h | 92°C |
| 0 | 1 | 0 | 1 | 0 | 0 | 14h | 93°C |
| 0 | 1 | 0 | 1 | 0 | 1 | 15h | 94°C |
| 0 | 1 | 1 | 0 | 0 | 0 | 18h | 95°C |
| 0 | 1 | 1 | 0 | 0 | 1 | 19h | 96°C |
| 0 | 1 | 1 | 0 | 1 | 0 | 1Ah | 97°C |
| 0 | 1 | 1 | 0 | 1 | 1 | 1Bh | 98°C |
| 0 | 1 | 1 | 1 | 0 | 0 | 1Ch | 99°C |
| 0 | 1 | 1 | 1 | 0 | 1 | 1Dh | 100°C |
| 1 | 0 | 0 | 0 | 0 | 0 | 20h | 101°C |
| 1 | 0 | 0 | 0 | 0 | 1 | 21h | 102°C |
| 1 | 0 | 0 | 0 | 1 | 0 | 22h | 103°C |
| 1 | 0 | 0 | 0 | 1 | 1 | 23h | 104°C |
| 1 | 0 | 0 | 1 | 0 | 0 | 24h | 105°C |
| 1 | 0 | 0 | 1 | 0 | 1 | 25h | 106°C |
| | 0 | 1 | 0 | 0 | 0 | 28h | 107°C |
| 1 | 0 | 1 | 0 | 0 | 1 | 29h | 108°C |

Table 7-3. Temperature Select Encoding (continued)

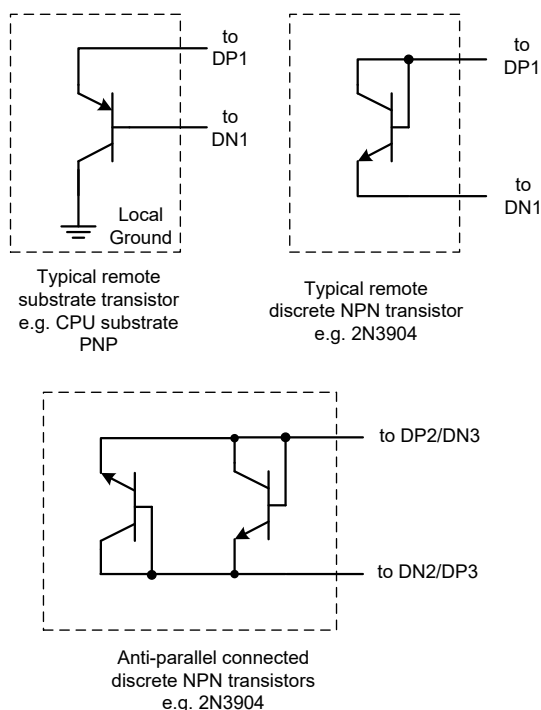
| SYS_SHDN Pull-up Decode | | | ALERT Pull-up Decode | | | Combined Decode (HEX) | Threshold Temperature |
|-------------------------|---|---|----------------------|---|---|-----------------------|-----------------------|
| 1 | 0 | 1 | 0 | 1 | 0 | 2Ah | 109°C |
| 1 | 0 | 1 | 0 | 1 | 1 | 2Bh | 110°C |
| 1 | 0 | 1 | 1 | 0 | 0 | 2Ch | 111°C |
| 1 | 0 | 1 | 1 | 0 | 1 | 2Dh | 112°C |

The hardware shutdown circuitry measures the External Diode 1 channel and compares it against the hardware thermal shutdown limit. The $\overline{\text{THERM}}$ pin consecutive alert counter (Default 4 for the $\overline{\text{SYS_SHDN}}$ pin) applies to this comparison. If the temperature meets or exceeds the limit for the number of consecutive measurements, the $\overline{\text{SYS_SHDN}}$ pin is asserted. The $\overline{\text{SYS_SHDN}}$ pin remains asserted until the temperature drops below the limit minus 10°C. As well, all of the measurement channels (including the External Diode 1 channel) can be configured to assert the $\overline{\text{SYS_SHDN}}$ pin. If a channel is configured to assert the $\overline{\text{SYS_SHDN}}$ pin, the temperature on the measured channel must exceed the programmed therm limit value. This is treated in the same way as the $\overline{\text{THERM}}$ output. For additional information, see [HARDWARE THERMAL SHUTDOWN LIMIT](#).

7.7. External Diode Connections

The EMC1822 can be configured to measure a CPU substrate transistor, a discrete 2N3904 thermal diode or a CPU/GPU processor diode. The diodes can be connected as indicated in [Figure 7-2](#).

The EMC1823 can be configured to measure a CPU substrate transistor, a discrete 2N3904 thermal diode or a CPU/GPU processor diode on the External Diode 1 or External Diode 2 channels. For the EMC1824, External Diode 2 and External Diode 3 channels are configured to measure a pair of discrete anti-parallel diodes (shared on pins DP2 and DN2). The supported configurations for the external diode channels are shown in [Figure 7-2](#).

Figure 7-2. Diode Configurations

7.8. Power States

The EMC1822/23/24/25/43 devices have two power states: Active and Standby.

- Active (Run) – In this state, the ADC is converting on all temperature channels at the programmed conversion rate. The temperature data are updated at the end of every conversion, and the limits are checked. In the Active state, writing to the One-Shot register has no effect.
- Standby (One-Shot) – While the device is in Standby, the host can initiate a conversion cycle on demand. After the conversion cycle is complete, the device returns to the Standby state.

7.9. Conversion Rates

The EMC1822/23/24/25/43 devices can be configured for different conversion rates based on the system requirements. The default conversion rate is four conversions per second. Other available conversion rates are shown in [Table 7-4](#).

Table 7-4. Conversion Rate

| HEX | CONV[3:0] | | | | Conversions/ Second |
|-------|------------|---|---|---|---------------------|
| | 3 | 2 | 1 | 0 | |
| 0h | 0 | 0 | 0 | 0 | 1/16 |
| 1h | 0 | 0 | 0 | 1 | 1/8 |
| 2h | 0 | 0 | 1 | 0 | 1/4 |
| 3h | 0 | 0 | 1 | 1 | 1/2 |
| 4h | 0 | 1 | 0 | 0 | 1 |
| 5h | 0 | 1 | 0 | 1 | 2 |
| 6h | 0 | 1 | 1 | 0 | 4 (default) |
| 7h | 0 | 1 | 1 | 1 | 8 |
| 8h | 1 | 0 | 0 | 0 | 16 |
| 9h | 1 | 0 | 0 | 1 | 32 |
| Ah | 1 | 0 | 1 | 0 | 64 |
| Bh-Fh | All Others | | | | 1 |

7.10. Dynamic Averaging

Dynamic averaging causes the EMC1822/23/24/25/43 devices to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates. When dynamic averaging is enabled, the devices automatically adjust the sampling and measurement time for the external diode channels. This allows the devices to average 2x to 16x longer than the normal 11-bit operation (nominally 21 ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time, as well as less random variation in the temperature measurement.

When enabled, dynamic averaging applies when a one-shot command is issued. The devices perform the desired averaging during the one-shot operation according to the selected conversion rate.

When enabled, dynamic averaging affects the average supply current based on the chosen conversion rate as shown in [Table 7-5](#).

Table 7-5. Supply Current vs. Conversion Rate for EMC1825

| Conversion Rate | Average Supply Current | | Averaging Factor (based on 11-bit operation) | |
|-----------------|-------------------------|------------|--|----------|
| | Dynamic Averaging State | | | |
| | Enabled (default) | Disabled | Enabled (default) | Disabled |
| 1/16s | 144 μ A | 80 μ A | 16x | 1x |

Table 7-5. Supply Current vs. Conversion Rate for EMC1825 (continued)

| Conversion Rate | Average Supply Current | | Averaging Factor (based on 11-bit operation) | |
|-----------------|-------------------------|--------------|--|----------|
| | Dynamic Averaging State | | | |
| | Enabled (default) | Disabled | Enabled (default) | Disabled |
| 1/8s | 213 μ A | 86 μ A | 16x | 1x |
| 1/4s | 351 μ A | 97 μ A | 16x | 1x |
| 1/2s | 627 μ A | 120 μ A | 16x | 1x |
| 1/s | 637 μ A | 164 μ A | 16x | 1x |
| 2/s | 659 μ A | 253 μ A | 16x | 1x |
| 4/s (default) | 703 μ A | 432 μ A | 8x | 1x |
| 8/s | 790 μ A | 790 μ A | 4x | 1x |
| 16/s | 830 μ A | 830 μ A | 2x | 1x |
| 32/s | 830 μ A | 830 μ A | 1x | 1x |
| 64/s | 1065 μ A | 1065 μ A | 0.5x | 0.5x |

7.11. Digital Filter

To reduce the effect of noise and temperature spikes on the reported temperature, the external diode channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2 or disabled (default). The typical filter performance is shown in the figures below. The Filter Configuration register controls the digital filter on External Diode Channel 1.

To reduce complexity, the digital filter only applies to External Diode Channels 1 and 2. Furthermore, this is only the case when APD is not enabled for a given channel. It applies after the digital block has taken the appropriate 11 bits based on the dynamic averaging.

Table 7-6. Filter Settings

| FILTER[1:0] | | Averaging |
|-------------|---|--------------------|
| 1 | 0 | |
| 0 | 0 | Disabled (default) |
| 0 | 1 | Level 1 (Note 1) |
| 1 | 0 | Level 1 (Note 1) |
| 1 | 1 | Level 2 (Note 2) |

Notes:

1. Filtering Level 1 corresponds to a 4x attenuation of a temperature spike.
2. Filtering Level 2 corresponds to an 8x attenuation of a temperature spike.

Figure 7-3. Temperature Filter Step Response

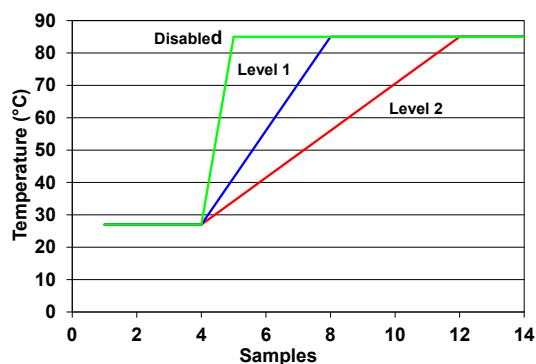
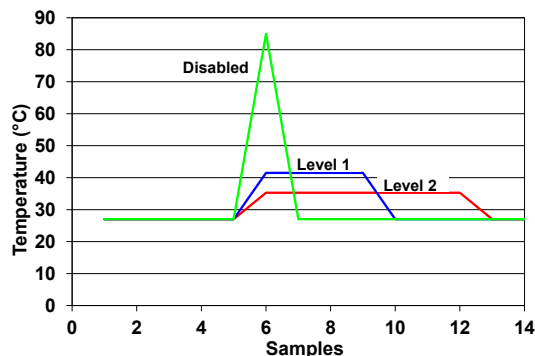


Figure 7-4. Temperature Filter Impulse Response



The filter consists of a running average on the external diode channel. The Level 1 filter is a running average of 4x, while the Level 2 filter is a running average of 8x. For the first measurement immediately after power-up, the filter will be filled with the results of the first measurement. After this, the filter operates normally. Any temperature comparisons are done with the filtered results that are stored in the user register.

7.12. Beta Compensation

The EMC1822/23/24/25/43 devices are configured to monitor the temperature of basic diodes (for example, 2N3904) or CPU thermal diodes. They automatically detect the type of external diode (CPU diode or diode-connected transistor) and determine the optimal setting to reduce temperature errors introduced by beta variation. Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high, such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents, with a transistor whose ideal beta is 50, would contribute approximately 0.25°C error at +100°C. However, for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large errors. For example, a 10% variation in beta for two forced emitter currents, with a transistor whose ideal beta is 0.5, would contribute approximately +8.25°C error at +100°C.

For the EMC1824 and EMC1825 devices, External Diode Channels 2/3 (EMC1824) and External Diode Channels 3/4 (EMC1825) do not support beta compensation.

At the beginning of every conversion, the optimal beta compensation factor setting is determined and applied. The BETA(N)[3:0] bits are automatically updated to indicate the current setting. This is the default for EMC1823. This is the default for EMC1824 for External Diode 1 only, and it is disabled and cannot be enabled for External Diodes 2 or 3. If the auto-detection circuitry is disabled, these bits will determine the beta configuration setting that is used for their respective channels.

It is recommended to be cautious when setting the BETA(N)[3:0] bits when the auto-detection circuitry is disabled. If the beta compensation factor is set at a beta value that is higher than the transistor beta, the circuit may generate measurement errors. When measuring a discrete thermal diode (such as 2N3904) or a CPU diode that functions like a discrete thermal diode (such as a CPU/GPU processor diode), the BETA(N)[3:0] bits must be set to '1111b'.

Table 7-7. CPU Beta Values

| DI_BETA[3:0] | | | | Minimum Beta |
|--------------|---|---|---|--------------|
| 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0.050 |
| 0 | 0 | 0 | 1 | 0.066 |

Table 7-7. CPU Beta Values (continued)

| DI_BETA[3:0] | | | | Minimum Beta |
|--------------|---|---|---|--------------|
| 3 | 2 | 1 | 0 | |
| 0 | 0 | 1 | 0 | 0.087 |
| 0 | 0 | 1 | 1 | 0.114 |
| 0 | 1 | 0 | 0 | 0.150 |
| 0 | 1 | 0 | 1 | 0.197 |
| 0 | 1 | 1 | 0 | 0.260 |
| 0 | 1 | 1 | 1 | 0.342 |
| 1 | 0 | 0 | 0 | 0.449 |
| 1 | 0 | 0 | 1 | 0.591 |
| 1 | 0 | 1 | 0 | 0.778 |
| 1 | 0 | 1 | 1 | 1.024 |
| 1 | 1 | 0 | 0 | 1.348 |
| 1 | 1 | 0 | 1 | 1.773 |
| 1 | 1 | 1 | 0 | 2.333 |
| 1 | 1 | 1 | 1 | Diode mode |

7.13. Resistance Error Correction (REC)

Parasitic resistance in series with the external diodes limits the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents causes the temperature measurement to read higher than the true temperature. Contributors to series resistance include PCB trace resistance, on-die (i.e., on the processor) metal resistance and bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is $+0.7^{\circ}\text{C}/\Omega$. The EMC1822/23/24/25/43 devices automatically correct for up to 100Ω of series resistance.

7.14. Programmable External Diode Ideality Factor

The EMC1822/23/24/25/43 device family is designed for external diodes with an ideality factor of 1.008. Not all external diodes, whether processor or discrete, will have this exact value. This variation in the ideality factor introduces errors in the temperature measurement, which must be corrected. This correction is typically done using programmable offset registers. Since an ideality factor mismatch introduces an error that is a function of temperature, this correction is only accurate within a small range of temperatures. To provide maximum flexibility to the user, the EMC1822/23/24/25/43 devices offer a 6-bit register for each external diode, where the ideality factor of the diode used is programmed to eliminate errors across all temperatures.

When monitoring a substrate transistor or CPU diode and beta compensation is enabled, the ideality factor should not be adjusted. Beta compensation automatically corrects for most ideality errors.

When measuring a 65 nm Intel[®] CPU, the ideality setting should be the default 12h. When measuring a 45 nm Intel CPU, the ideality setting should be 15h.

These registers store the ideality factors that are applied to the external diodes. [Table 7-8](#) defines each setting and the corresponding ideality factor. Since beta compensation and Resistance Error Correction automatically correct for most diode ideality errors, it is not recommended that these settings be updated without consulting Microchip Technology.

Table 7-8. Ideality Factor Look-up Table (Diode Model)

| Setting | Factor | Setting | Factor | Setting | Factor |
|---------|--------|---------|--------|---------|--------|
| 08h | 0.9949 | 18h | 1.0159 | 28h | 1.0371 |
| 09h | 0.9962 | 19h | 1.0172 | 29h | 1.0384 |

Table 7-8. Ideality Factor Look-up Table (Diode Model) (continued)

| Setting | Factor | Setting | Factor | Setting | Factor |
|---------|--------|---------|--------|---------|--------|
| 0Ah | 0.9975 | 1Ah | 1.0185 | 2Ah | 1.0397 |
| 0Bh | 0.9988 | 1Bh | 1.0200 | 2Bh | 1.0410 |
| 0Ch | 1.0001 | 1Ch | 1.0212 | 2Ch | 1.0423 |
| 0Dh | 1.0014 | 1Dh | 1.0226 | 2Dh | 1.0436 |
| 0Eh | 1.0027 | 1Eh | 1.0239 | 2Eh | 1.0449 |
| 0Fh | 1.0040 | 1Fh | 1.0253 | 2Fh | 1.0462 |
| 10h | 1.0053 | 20h | 1.0267 | 30h | 1.0475 |
| 11h | 1.0066 | 21h | 1.0280 | 31h | 1.0488 |
| 12h | 1.0080 | 22h | 1.0293 | 32h | 1.0501 |
| 13h | 1.0093 | 23h | 1.0306 | 33h | 1.0514 |
| 14h | 1.0106 | 24h | 1.0319 | 34h | 1.0527 |
| 15h | 1.0119 | 25h | 1.0332 | 35h | 1.0540 |
| 16h | 1.0133 | 26h | 1.0345 | 36h | 1.0553 |
| 17h | 1.0146 | 27h | 1.0358 | 37h | 1.0566 |

For CPU substrate transistors that require the BJT transistor model, the ideality factor behaves slightly differently than for discrete diode-connected transistors. Refer to the following when using a CPU substrate transistor.

Table 7-9. Substrate Diode Ideality Factor Look-up Table (BJT Model)

| Setting | Factor | Setting | Factor | Setting | Factor |
|---------|--------|---------|--------|---------|--------|
| 08h | 0.9869 | 18h | 1.0079 | 28h | 1.0291 |
| 09h | 0.9882 | 19h | 1.0092 | 29h | 1.0304 |
| 0Ah | 0.9895 | 1Ah | 1.0105 | 2Ah | 1.0317 |
| 0Bh | 0.9908 | 1Bh | 1.0120 | 2Bh | 1.0330 |
| 0Ch | 0.9921 | 1Ch | 1.0132 | 2Ch | 1.0343 |
| 0Dh | 0.9934 | 1Dh | 1.0146 | 2Dh | 1.0356 |
| 0Eh | 0.9947 | 1Eh | 1.0159 | 2Eh | 1.0369 |
| 0Fh | 0.9960 | 1Fh | 1.0173 | 2Fh | 1.0382 |
| 10h | 0.9973 | 20h | 1.0187 | 30h | 1.0395 |
| 11h | 0.9986 | 21h | 1.0200 | 31h | 1.0408 |
| 12h | 1.0000 | 22h | 1.0213 | 32h | 1.0421 |
| 13h | 1.0013 | 23h | 1.0226 | 33h | 1.0434 |
| 14h | 1.0026 | 24h | 1.0239 | 34h | 1.0447 |
| 15h | 1.0039 | 25h | 1.0252 | 35h | 1.0460 |
| 16h | 1.0053 | 26h | 1.0265 | 36h | 1.0473 |
| 17h | 1.0066 | 27h | 1.0278 | 37h | 1.0486 |

7.15. Diode Faults

The EMC1822/23/24/25/43 devices detect an open on the DP and DN pins, as well as a short across the DP and DN pins. For each temperature measurement made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the $\overline{\text{ALERT}}$ pin asserts (unless masked), and the temperature data reads 00h in the MSB and LSB registers (note that the low limit is not checked). A diode fault is defined as one of the following: an open between DP and DN, a short from V_{DD} to DP or a short from V_{DD} to DN.

If a short occurs across DP and DN or a short occurs from DP to GND, the Low Limit Status bit is not set and the $\overline{\text{ALERT}}$ pin does not assert. This condition is indistinguishable from a temperature

measurement of 0.000°C (-64°C in extended range), resulting in temperature data of 00h in the MSB and LSB registers.

If a short from DN to GND occurs (with a diode connected), temperature measurements will continue as normal with no alerts.

7.16. Consecutive Alerts

The EMC1822/23/24/25/43 device family contains multiple consecutive alert counters. One set of counters applies to the $\overline{\text{ALERT}}$ pin and the second set of counters applies to the $\overline{\text{THERM}}$ pin. Each temperature measurement channel has a separate consecutive alert counter for each of the $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins. All counters are user-programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding pin is asserted.

The Consecutive Alert register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the $\overline{\text{ALERT}}$ or $\overline{\text{THERM}}$ pin is asserted.

An out-of-limit condition (for example, HIGH, LOW or FAULT) occurring on the same temperature channel in consecutive measurements will increment the consecutive alert counter. The counters will also be reset if no out-of-limit condition or diode fault condition occurs in a consecutive reading.

When the $\overline{\text{ALERT}}$ pin is configured as an interrupt, and the consecutive alert counter reaches its programmed value, the following occurs: the status bit(s) for that channel and the last error condition(s) (for example, E1HIGH, or E2LOW and/or E2FAULT) are set to '1', the $\overline{\text{ALERT}}$ pin is asserted, the consecutive alert counter is cleared and measurements continue to be performed.

When the $\overline{\text{ALERT}}$ pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors, and will only increment if the measured temperature exceeds the high limit. Additionally, once the consecutive alert counter reaches the programmed limit, the $\overline{\text{ALERT}}$ pin is asserted, but the counter does not reset. It remains set until the temperature drops below the high limit minus the Therm Hysteresis value.

Channels that are not enabled are not included in the consecutive alert checking. The signal logic chain is: Limit → Counter → Status → Mask → Pin ($\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$).

For example, if the CALRT[2:0] bits are set for four consecutive alerts on an EMC1822/23/24/25/43 device, the high limits are set at +70°C and none of the channels are masked, then the $\overline{\text{ALERT}}$ pin is asserted after the following five measurements:

- Internal Diode reads +71°C and both external diodes read +69°C. Consecutive alert counter for INT is incremented to 1.
- Both the Internal Diode and the External Diode 1 read +71°C and External Diode 2 reads +68°C. Consecutive alert counter for INT is incremented to 2 and EXT1 is set to 1.
- The External Diode 1 reads +71°C, and both the Internal Diode and External Diode 2 read +69°C. Consecutive alert counters for INT and EXT2 are cleared and EXT1 is incremented to 2.
- The Internal Diode reads +71°C and both external diodes read +71°C. Consecutive alert counter for INT is set to 1, EXT2 is set to 1 and EXT1 is incremented to 3.
- The Internal Diode reads +71°C and both external diodes read +71°C. Consecutive alert counter for INT is incremented to 2, EXT2 is set to 2 and EXT1 is incremented to 4. The appropriate status bits are set for EXT and the $\overline{\text{ALERT}}$ pin is asserted. The EXT1 counter is reset to 0, and all other counters hold the last value until the next temperature measurement.

All temperature channels use this value to set the respective counters. The consecutive therm counter is incremented whenever any measurement exceeds the corresponding therm limit.

If the temperature drops below the therm limit, the counter is reset. If a number of consecutive measurements above the therm limit occurs, the $\overline{\text{THERM}}$ pin is asserted low.

Once the $\overline{\text{THERM}}$ pin has been asserted, the consecutive therm counter will not reset until the corresponding temperature drops below the therm limit minus the therm hysteresis value.

The bits are decoded as shown in [Table 7-10](#). The default setting is four consecutive out-of-limit conversions.

All temperature channels use this value to set the respective counters. The bits are decoded as shown in the table below. The default setting is one consecutive out-of-limit conversion.

When the $\overline{\text{ALERT}}$ pin is in Comparator mode, the low limit and diode fault will bypass the consecutive alert counter and set the appropriate status bits, but will NOT assert the $\overline{\text{ALERT}}$ pin.

When a value is written to [CONSEC ALERT](#) (Address 22h) that is not defined below, the command is ignored and the last valid value is maintained.

Table 7-10. Consecutive $\overline{\text{ALERT}}$ / $\overline{\text{THERM}}$ Settings

| 2 | 1 | 0 | Number of Consecutive Out-of-Limit Measurements |
|---|---|---|---|
| 0 | 0 | 0 | 1 (default for CALRT[2:0]) |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 1 | 1 | 4 (default for CTHRM[2:0]) |

7.17. “Hottest Of” Comparison

At the end of every measurement cycle, the EMC1822/23/24/25/43 devices compare all of the user-selectable internal and external diode channels to determine which of these channels is reporting the hottest temperature. The hottest temperature is stored in the Hottest Temperature registers and the appropriate status bit is set in the Hottest Status register. If multiple temperature channels measure the same temperature and are equal to the hottest temperature, the hottest status will be displayed for all selected temperature channels with the hottest temperature measurement.

As an optional feature, the EMC1822/23/24/25/43 devices can also flag an event if the hottest temperature channel changes by enabling the REMHOT (Remember Hottest) bit (see [HOTTEST CONFIG](#)). For example, suppose that External Diode Channels 1, 3 and 4 are programmed to be compared in the “Hottest Of” comparison. If the External Diode 1 channel reports the hottest temperature of the three, its temperature is copied into the Hottest Temperature registers (in addition to the External Diode 1 Temperature registers) and it is flagged in the Hottest Status bit. If, on the next measurement, the External Diode 3 channel temperature has increased, such that it is now the hottest temperature, the EMC1822/23/24/25/43 devices can flag this event as an interrupt condition and assert the $\overline{\text{ALERT}}$ pin.

7.18. Rate of Change

The Rate of Change (ROC) function approximates the derivative of the temperature using a difference equation. The equation below is the basis for calculation.

The ROC can be enabled for the first two standard diode connections. If Diode 2 is an anti-parallel connected diode, the ROC feature is applied to Diode 3. For the EMC1843, the ROC only applies to External Diode 1.

Equation: Rate of Change

$$\frac{\Delta T}{\Delta t} = \frac{[T(t_{\max}) - T(t_0)] \times \text{gain}}{(\text{sample} - 1)}$$

Where:

| | | |
|---------------|---|--|
| $T(t_{\max})$ | = | Temperature at the end of the interval |
| $T(t_0)$ | = | Temperature at the beginning of the interval |

The ROC period (t_0 to t_{\max}) can be approximated by the combination of conversion rate (see [Table 7-4](#)) and ROC samples (Address 43h, 48h). The table below shows the samples defined by the bit settings.

For example, setting the conversion rate to one conversion per second and the number of ROC samples to 65 samples would give an approximate ROC period of 65 seconds or approximately one minute.

The gain applied to the result is stored in [ROC GAIN](#) (Address 3Dh). The effective gains are shown in the register definition.

Since this is sampled over time, there is a bit for each channel that indicates a change in slope has occurred. These bits (one for each channel) assert when the result of two consecutive sample

differences exceeds the threshold limit, as defined by the hysteresis value defined in [ROC CONFIG](#) (Address 3Eh). The ROC calculations are not affected.

The Limit registers ([R LIMH](#) and [R LIML](#)) and Results registers ([R RESH](#) and [R2/3 RESL](#)) are signed, two's complement numbers stored in two consecutive registers.

If the Rate of Change result stored in registers 40h and 44h exceeds the programmed limit, the appropriate Status register bits will be set in [ROC STATUS](#) (Address 3Fh). The $\overline{\text{ALERT}}$ pin may be asserted or masked, as set by [ROC CONFIG](#) (Address 3Eh). The MASK bit does not prevent the status bits from updating, but if set, it prevents the $\overline{\text{ALERT}}$ pin from asserting.

In addition to the functions described above, two additional temperature values are stored in registers for retrieval. The maximum temperature for a given sample period is stored in a register (4Ah) that updates every sample period and in a second register (4Dh, 4Fh) that stores a "global value", and cleared only when read. The purpose of this register is to determine a maximum or minimum temperature, independent of the sample period.

Below is an example of setting up the Rate of Change feature and interpreting the results.

1. Enable Standby mode: Write a value of 40h into register 03h.
2. Set ROC gain: Write a value of 09h in register 3Dh. This sets the gain value of two for both Ext1 and Ext2/3.
3. Set ROC samples Ext1, Ext2/3: Write a value of 02h/02h in registers 43h/48h. This sets the ROC samples to five for both EXT1 and Ext2/3.
4. Set ROC Alert Limit Ext1/Ext2: Write a value of 01h/01h in registers 41h/46h. This sets the ROC limit to two for both Ext1 and Ext2/3.
5. Enable ROC and Hysteresis: Write a value of 20h in register 3Eh. This enables the ROC and sets the hysteresis value to zero.

ROC example:

1. Stabilize ambient temperature of device to +25°C.
2. Initiate one-shot conversion: Write a value of FFh in register 0Fh.
3. Read ROC Status register: For the first conversion, the ROC Status register (3Fh) reads 00h. Note that the initial slope of the sample period is determined using the first and second samples of the sample period.
4. Stabilize ambient temperature of device to +35°C.
5. Initiate one-shot conversion: Write a value of FFh in register 0Fh.
6. Read ROC Status register: For the second conversion, the ROC Status register (3Fh) should read 00h. Again, the initial slope of the sample period is determined using the first and second samples of the sample period.
7. Stabilize ambient temperature of device to +30°C.
8. Initiate one-shot conversion: Write a value of FFh in register 0Fh.
9. Read ROC Status register: For the third conversion, the ROC Status register (3Fh) reads F0h. The initial slope of the sample period is positive, going from +25°C to +35°C. A change in temperature from +35°C to +30°C causes a slope change; the number of slope changes is now one (odd). See ROC Status register (3Fh) bit descriptions for more clarification.
10. Stabilize ambient temperature of device to +45°C.
11. Initiate one-shot conversion: Write a value of FFh in register 0Fh.
12. Read ROC Status register: For the fourth conversion, the ROC Status register (3Fh) should read C0h. The previous slope was negative, going from +35°C to +30°C. A change in temperature from +30°C to +45°C causes a slope change; the number of slope changes is now two (even).
13. Stabilize ambient temperature of device to +35°C.

14. Initiate one-shot conversion: Write a value of FFh in register 0Fh.
15. Read ROC Status register: For the fifth conversion, the ROC Status register (3Fh) should read FCh. The previous slope was positive, going from +30°C to +45°C. A change in temperature from +45°C to +35°C causes a slope change; the number of slope changes is now three (odd). Once the final conversion of the sample period is completed, the ROC result is calculated using the equation below and compared to the ROC HB/LB Limit registers. In this scenario, the ROC limit was exceeded and the appropriate bits were set in the ROC Status register.
16. Read ROC HB/LB Result ROC register: Once the final conversion of the sample period is completed, the ROC result is calculated using the following equation. This value is loaded into the ROC HB/LB Result register. Based on the equation, the result is five:

$$\text{ROC Results} = \frac{(35 - 25) \times 2}{4} = 5:$$

The ROCx high byte and low byte are in 9-bit signed two's complement format. The MSB of the low byte is the LSB of the corresponding high byte. For this example the ROC HB and LB would be as follows:

Table 7-11. ROC1,2/3 High Byte (40h, 44h)

| Sign | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|------|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

Table 7-12. ROC Low Byte (45h)

| LSB | 2 | 1 | 0 | LSB | 3 | 2 | 1 |
|-----|---|---|---|-----|----------|----------|----------|
| HB2 | — | — | — | HB1 | — | — | — |
| 1 | 0 | 0 | 0 | 1 | 0 (Note) | 0 (Note) | 0 (Note) |

Note: Fractional value.

17. Read Global Max register (4Dh): The Global Max value is 2Dh or +45°C. The Global Max register contains a history of the highest temperature value. This value is reset only at POR and it is updated at the end of each ROC sample period.
18. Read Sample Period Max register (49h): The Sample Period Max value should be 2Dh or +45°C. This register contains the highest temperature value for a given sample period and is updated after each temperature conversion.

8. System Management Bus Protocol

The EMC1822/23/24/25/43 devices communicate with a host controller through the SMBus/I²C. The SMBus/I²C is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in [Figure 3-1](#). Stretching of the SMCLK signal is supported; however, the EMC1822/23/24/25/43 devices do not stretch the clock signal.

8.1. SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus/I²C data line from a logic '1' state to a logic '0' state, while the SMBus/I²C clock line is in a logic '1' state.

8.2. SMBus Address and RD/ $\overline{\text{WR}}$ Bit

The SMBus address byte consists of the 7-bit client address followed by the RD/ $\overline{\text{WR}}$ indicator bit. If the RD/ $\overline{\text{WR}}$ bit is a logic '0', the SMBus host is writing data to the client device. If the RD/ $\overline{\text{WR}}$ bit is a logic '1', the SMBus host is reading data from the client device.

The response to the client address is '1001_100xb' for -1 parts and '1001_101xb' for -2 parts.

8.3. SMBus Data Bytes

All SMBus data bytes are sent Most Significant bit first and are composed of eight bits of information.

8.4. SMBus ACK and NACK Bits

The SMBus client acknowledges all data bytes that it receives. This is done by the client device pulling the SMBus data line low after the 8th bit of each byte that is transmitted. This applies to both the write byte and block write protocols.

The host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent. For the block read protocol, the host will ACK (acknowledge) each data byte that it receives, except the last data byte.

8.5. SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When a EMC1822/23/24/25/43 device detects an SMBus Stop bit and has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

8.6. SMBus Time-out

The EMC1822/23/24/25/43 device family includes an SMBus time-out feature. Following a 30 ms period of inactivity on the SMBus, where the SMCLK pin is held low, the device will time-out and reset the SMBus interface.

The time-out function defaults to disabled. It can be enabled by setting the TIMEOUT bit in the Consecutive Alert register (see [Consecutive Alert Register \(address 22h\)](#)).

8.7. SMBus and I²C Compliance

The major differences between SMBus and I²C devices include the following:

- Minimum frequency for SMBus communications is 10 kHz
- The client protocol resets if the clock is held low for longer than 30 ms
- Except when operating in Standby mode, the client protocol resets if both the clock and data line are high for longer than 150 μs (Idle condition)
- I²C devices do not support the Alert Response Address functionality (which is optional for SMBus)

For complete compliance information, refer to “AN14.0, *Microchip Dedicated Slave Devices in I²C™ Systems*” (DS00001853).

8.8. SMBus Protocols

The EMC1822/23/24/25/43 devices are SMBus 2.0 compatible and support send byte, read byte, block read and receive byte as valid protocols, as shown in [Table 8-1](#). They also support the I²C block read and block write protocols. The device supports write byte, read byte and block read/block write.

All of the protocols below use the convention in [Table 8-1](#).

Table 8-1. SMBus Protocol

| Data Sent to Device | Data Sent to the Host |
|---------------------|-----------------------|
| # of bits sent | # of bits sent |

8.8.1. SMBus Write Byte

The write byte is used to write one byte of data to a specific register, as shown in the following table.

Table 8-2. SMBus Write Byte Protocol

| START | Client Address | WR | ACK | Register Address | ACK | Register Data | ACK | STOP |
|-------|----------------|----|-----|------------------|-----|---------------|-----|-------|
| 1 → 0 | YYYY_YYY | 0 | 0 | XXh | 0 | XXh | 0 | 0 → 1 |

8.8.2. Block Write

The block write is used to write multiple data bytes to a group of contiguous registers, as shown in [Table 8-3](#). It is an extension of the write byte protocol.

Table 8-3. Block Write Protocol

| START | Client Address | WR | ACK | Register Address | ACK | Repeat N Times | | STOP |
|-------|----------------|----|-----|------------------|-----|----------------|-----|-------|
| | | | | | | Register Data | ACK | |
| 1 → 0 | YYYY_YYY | 0 | 0 | XXh | 0 | XXh | 0 | 0 → 1 |

Note: When using the block write protocol, the internal Address Pointer will be automatically incremented after every data byte is received; it will wrap from FFh to 00h.

Note: The block write and block read protocols require that the Address Pointer be automatically incremented. For a write command, the Address Pointer will be automatically incremented when the ACK is sent to the host. There is no over or underbound limit checking and the Address Pointer will wrap around from FFh to 00h if necessary.

8.8.3. SMBus Read Byte

The read byte protocol is used to read one byte of data from the registers, as in [Table 8-4](#).

Table 8-4. Read Byte Protocol

| START | Client Address | WRITE | ACK | Register Data | ACK |
|-------|----------------|-------|-----|---------------|-----|
| 1 → 0 | YYYY_YYY | 0 | 0 | XXh | 0 |

| START | Client Address | READ | ACK | Register Data | NACK | STOP |
|-------|----------------|------|-----|---------------|------|-------|
| 1 → 0 | 0101_000 | 1 | 0 | XXh | 1 | 0 → 1 |

8.8.4. Block Read

The block read is used to read multiple data bytes from a group of contiguous registers, as shown in [Table 8-5](#). It is an extension of the read byte protocol.

Note: When using the block read protocol, the internal Address Pointer will be automatically incremented after every data byte is received; it will wrap from FFh to 00h.

Table 8-5. Block Read Protocol

| START | Client Address | Write | ACK | Register Address | ACK |
|-------|----------------|-------|-----|------------------|-----|
| 1 → 0 | YYYY_YYY | 0 | 0 | XXh | 0 |

| START | Client Address | Read | ACK | Register Data | ACK | Register Data | NACK | STOP |
|-------|----------------|------|-----|---------------|-----|---------------|------|-------|
| 1 → 0 | YYYY_YYY | 1 | 0 | XXh | 0 | XXh | 1 | 0 → 1 |

Note: The block write and block read protocols require that the Address Pointer be automatically incremented. For a read command, the Address Pointer will be automatically incremented when the ACK is sent by the host. There is no over or underbound limit checking and the Address Pointer will wrap around from FFh to 00h if necessary.

8.8.5. SMBus Send Byte

The send byte protocol is used to set the internal Address Register Pointer to the correct address location. No data are transferred during the send byte protocol, as shown in [Table 8-6](#).

Table 8-6. Send Byte Protocol

| START | Client Address | WR | ACK | Register Data | ACK | STOP |
|-------|----------------|----|-----|---------------|-----|-------|
| 1 → 0 | YYYY_YYY | 0 | 0 | XXh | 0 | 0 → 1 |

8.8.6. SMBus Receive Byte

The receive byte protocol is used to read data from a register when the internal register Address Pointer is known to be at the correct location (e.g., set via send byte). This is used for consecutive reads of the same register as shown in [Table 8-7](#).

Table 8-7. Receive Byte Protocol

| START | Client Address | RD | ACK | Register Data | NACK | STOP |
|-------|----------------|----|-----|---------------|------|-------|
| 1 → 0 | YYYY_YYY | 1 | 0 | XXh | 1 | 0 → 1 |

8.9. $\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ Pin Considerations

Because of the decode method used to determine the system shutdown temperature value, it is important that the pull-up resistance on the $\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ pins be within the tolerances shown in [Table 7-2](#).

For $t_{\text{INT_T}}$ after power-up, the $\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ pins must not be pulled low or the I²C address will not be decoded properly. If the system requirements do not permit these conditions, the $\overline{\text{ALERT}}$ and $\overline{\text{SYS_SHDN}}$ pins must be isolated from their hard-wired OR'd bus during this time.

One method of isolating these pins is shown in the following figures.

Figure 8-1. $\overline{\text{ALERT}}$ Pin Isolation

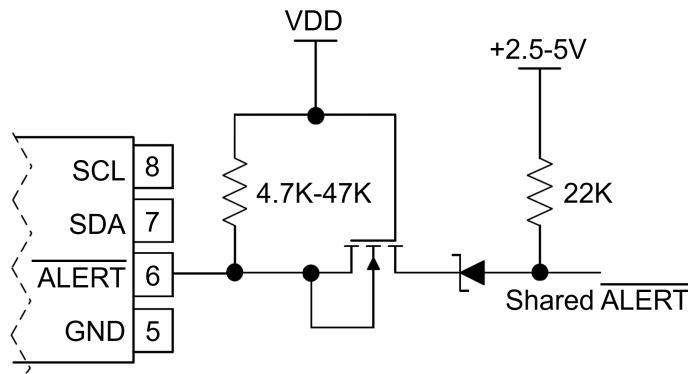
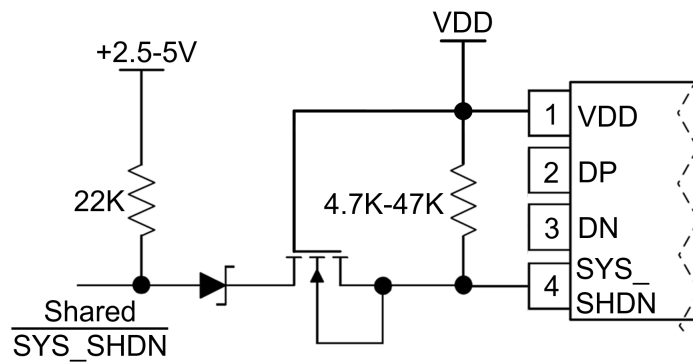


Figure 8-2. $\overline{\text{SYS_SHDN}}$ Pin Isolation



8.10. Register Summary

| Offset | Name | Bit Pos. | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------------------------|----------|-----------------|------------|--------|---------|--------------|--------|--------|---------|
| 0x00 | INT HIGH BYTE | 7:0 | IHB[7:0] | | | | | | | |
| 0x01 | EXT1 HIGH BYTE | 7:0 | EXT(N)HB[7:0] | | | | | | | |
| 0x02 | STATUS | 7:0 | ROCF | HOTCHG | BUSY | HIGH | LOW | FAULT | ETHRM | ITHRM |
| 0x03 | CONFIG | 7:0 | MSKAL | R/S | AT/THM | RECD1/2 | RECD3/4 | RANGE | DA_ENA | APDD |
| 0x04 | CONVERT | 7:0 | CONV[3:0] | | | | | | | |
| 0x05 | INT DIODE HIGH LIMIT | 7:0 | IDHL[7:0] | | | | | | | |
| 0x06 | INT DIODE LOW LIMIT | 7:0 | IDLL[7:0] | | | | | | | |
| 0x07 | EXT1 HIGH LIMIT HIGH BYTE | 7:0 | EXT(N)HLHB[7:0] | | | | | | | |
| 0x08 | EXT1 LOW LIMIT HIGH BYTE | 7:0 | EXT(N)LLHB[7:0] | | | | | | | |
| 0x09 | CONFIG | 7:0 | MSKAL | R/S | AT/THM | RECD1/2 | RECD3/4 | RANGE | DA_ENA | APDD |
| 0x0A | CONVERT | 7:0 | CONV[3:0] | | | | | | | |
| 0x0B | INT DIODE HIGH LIMIT | 7:0 | IDHL[7:0] | | | | | | | |
| 0x0C | INT DIODE LOW LIMIT | 7:0 | IDLL[7:0] | | | | | | | |
| 0x0D | EXT1 HIGH LIMIT HIGH BYTE | 7:0 | EXT(N)HLHB[7:0] | | | | | | | |
| 0x0E | EXT1 LOW LIMIT HIGH BYTE | 7:0 | EXT(N)LLHB[7:0] | | | | | | | |
| 0x0F | ONE SHOT | 7:0 | ONSH[7:0] | | | | | | | |
| 0x10 | EXT1 LOW BYTE | 7:0 | EXT(N)LB[2:0] | | | | | | | |
| 0x11 | SCRTPD1 | 7:0 | SPD(N)[7:0] | | | | | | | |
| 0x12 | SCRTPD2 | 7:0 | SPD(N)[7:0] | | | | | | | |
| 0x13 | EXT1 HIGH LIMIT LOW BYTE | 7:0 | EXT(N)HLLB[2:0] | | | | | | | |
| 0x14 | EXT1 LOW LIMIT LOW BYTE | 7:0 | EXT(N)LLLB[2:0] | | | | | | | |
| 0x15 | EXT2 HIGH LIMIT HIGH BYTE | 7:0 | EXT(N)HLHB[7:0] | | | | | | | |
| 0x16 | EXT2 LOW LIMIT HIGH BYTE | 7:0 | EXT(N)LLHB[7:0] | | | | | | | |
| 0x17 | EXT2 HIGH LIMIT LOW BYTE | 7:0 | EXT(N)HLLB[2:0] | | | | | | | |
| 0x18 | EXT2 LOW LIMIT LOW BYTE | 7:0 | EXT(N)LLLB[2:0] | | | | | | | |
| 0x19 | EXT1 THERM LIMIT | 7:0 | EXT(N)THL[7:0] | | | | | | | |
| 0x1A | EXT2 THERM LIMIT | 7:0 | EXT(N)THL[7:0] | | | | | | | |
| 0x1B | EXTERNAL DIODE FAULT STATUS | 7:0 | | | | E4FLT | E3FLT | E2FLT | E1FLT | |
| 0x1C | Reserved | | | | | | | | | |
| 0x1D | SW THERMAL SHUTDOWN CONFIG | 7:0 | | | | E4SYS | E3SYS | E2SYS | E1SYS | INTSYS |
| 0x1E | HARDWARE THERMAL SHUTDOWN LIMIT | 7:0 | SSDNL[7:0] | | | | | | | |
| 0x1F | DIODE FAULT MASK | 7:0 | | | | E4MASK | E3MASK | E2MASK | E1MASK | INTMASK |
| 0x20 | INT DIODE THERM LIMIT | 7:0 | IDTHL[7:0] | | | | | | | |
| 0x21 | THRM HYS | 7:0 | THRMH[7:0] | | | | | | | |
| 0x22 | CONSEC ALERT | 7:0 | TMOUT | CTHRM[2:0] | | | CALRT[2:0] | | | |
| 0x23 | EXT2 HIGH BYTE | 7:0 | EXT(N)HB[7:0] | | | | | | | |
| 0x24 | EXT2 LOW BYTE | 7:0 | EXT(N)LB[2:0] | | | | | | | |
| 0x25 | EXT1 BETA CONFIG | 7:0 | | | | ENBL(N) | BETA(N)[3:0] | | | |
| 0x26 | EXT2 BETA CONFIG | 7:0 | | | | ENBL(N) | BETA(N)[3:0] | | | |

Register Summary (continued)

| Offset | Name | Bit Pos. | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------------------|----------|---------|-------|-----------------|---------|---------|---------|---------|-----------------|
| 0x27 | EXT1 IDEALITY FACTOR | 7:0 | | | | | | | | IDEAL(N)[5:0] |
| 0x28 | EXT2 IDEALITY FACTOR | 7:0 | | | | | | | | IDEAL(N)[5:0] |
| 0x29 | INT LOW BYTE | 7:0 | | | ILB[2:0] | | | | | |
| 0x2A | EXT3 HIGH BYTE | 7:0 | | | | | | | | EXT(N)HB[7:0] |
| 0x2B | EXT3 LOW BYTE | 7:0 | | | EXT(N)LB[2:0] | | | | | |
| 0x2C | EXT3 HIGH LIMIT HIGH BYTE | 7:0 | | | | | | | | EXT(N)HLHB[7:0] |
| 0x2D | EXT3 LOW LIMIT HIGH BYTE | 7:0 | | | | | | | | EXT(N)LLHB[7:0] |
| 0x2E | EXT3 HIGH LIMIT LOW BYTE | 7:0 | | | EXT(N)HLLB[2:0] | | | | | |
| 0x2F | EXT3 LOW LIMIT LOW BYTE | 7:0 | | | EXT(N)LLLB[2:0] | | | | | |
| 0x30 | EXT3 THERM LIMIT | 7:0 | | | | | | | | EXT(N)THL[7:0] |
| 0x31 | EXT3 IDEALITY FACTOR | 7:0 | | | | | | | | IDEAL(N)[5:0] |
| 0x32 | EXT4 HIGH BYTE | 7:0 | | | | | | | | EXT(N)HB[7:0] |
| 0x33 | EXT4 LOW BYTE | 7:0 | | | EXT(N)LB[2:0] | | | | | |
| 0x34 | EXT4 HIGH LIMIT HIGH BYTE | 7:0 | | | | | | | | EXT(N)HLHB[7:0] |
| 0x35 | EXT4 LOW LIMIT HIGH BYTE | 7:0 | | | | | | | | EXT(N)LLHB[7:0] |
| 0x36 | EXT4 HIGH LIMIT LOW BYTE | 7:0 | | | EXT(N)HLLB[2:0] | | | | | |
| 0x37 | EXT4 LOW LIMIT LOW BYTE | 7:0 | | | EXT(N)LLLB[2:0] | | | | | |
| 0x38 | EXT4 THERM LIMIT | 7:0 | | | | | | | | EXT(N)THL[7:0] |
| 0x39 | EXT4 IDEALITY FACTOR | 7:0 | | | | | | | | IDEAL(N)[5:0] |
| 0x3A | HIGH LIMIT STATUS | 7:0 | | | | E4HIGH | E3HIGH | E2HIGH | E1HIGH | IHIGH |
| 0x3B | LOW LIMIT STATUS | 7:0 | | | | E4LOW | E3LOW | E2LOW | E1LOW | ILOW |
| 0x3C | THERM LIMIT STATUS | 7:0 | | | | E4THERM | E3THERM | E2THERM | E1THERM | ITHERM |
| 0x3D | ROC GAIN | 7:0 | | | | | | | | RC1G[7:0] |
| 0x3E | ROC CONFIG | 7:0 | | | EN_ROC | MASK2/3 | MASK1 | | | RCHY[2:0] |
| 0x3F | ROC STATUS | 7:0 | SLCG2/3 | SLCG1 | R2/3ODD | R1ODD | RC2/3HI | RC1HI | RC2/3LO | RC1LO |
| 0x40 | R1 RESH | 7:0 | | | | | | | | R(N)RH[7:0] |
| 0x41 | R1 LIMH | 7:0 | | | | | | | | R(N)LIMH[7:0] |
| 0x42 | R1 LIML | 7:0 | | | | | | | | R(N)LIML[3:0] |
| 0x43 | R1 SMPL | 7:0 | | | | | | | | R(N)SH[3:0] |
| 0x44 | R2 RESH | 7:0 | | | | | | | | R(N)RH[7:0] |
| 0x45 | R2/3 RESL | 7:0 | | | | | | | | R2/3_RL[3:0] |
| 0x46 | R2 LIMH | 7:0 | | | | | | | | R1_RL[3:0] |
| 0x47 | R2 LIML | 7:0 | | | | | | | | R(N)LIMH[7:0] |
| 0x48 | R2 SMPL | 7:0 | | | | | | | | R(N)LIML[3:0] |
| 0x49 | PER MAXTH | 7:0 | | | | | | | | R(N)SH[3:0] |
| 0x4A | PER MAXT1L | 7:0 | | | | | | | | GM(N)HB[7:0] |
| 0x4B | PER MAXTH | 7:0 | | | PM(N)L[2:0] | | | | | GM(N)HB[7:0] |
| 0x4C | PER MAXT2/3L | 7:0 | | | PM(N)L[2:0] | | | | | GM(N)HB[7:0] |
| 0x4D | GBL MAXT1H | 7:0 | | | | | | | | GM(N)HB[7:0] |
| 0x4E | GBL MAXT1L | 7:0 | | | | | | | | GM(N)HB[7:0] |
| 0x4F | GBL MAXT2H | 7:0 | | | | | | | | GM(N)LB[2:0] |
| 0x50 | GBL MAXT2L | 7:0 | | | | | | | | GM(N)HB[7:0] |
| 0x51 | FILTER SEL | 7:0 | | | | | | | | GM(N)LB[2:0] |
| 0x52 | ... | | | | | | | | | FILTER[1:0] |
| 0x5F | Reserved | | | | | | | | | |
| 0x60 | INT HIGH BYTE | 7:0 | | | | | | | | IHB[7:0] |
| 0x61 | INT LOW BYTE | 7:0 | | | | | | | | ILB[2:0] |

Register Summary (continued)

| Offset | Name | Bit Pos. | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------------------|-------------------------|----------|-----------------|---|--------|-------|-------|-------|-------|------|--|
| 0x62 | EXT1 HIGH BYTE | 7:0 | EXT(N)HB[7:0] | | | | | | | | |
| 0x63 | EXT1 LOW BYTE | 7:0 | EXT(N)LB[2:0] | | | | | | | | |
| 0x64 | EXT2 HIGH BYTE | 7:0 | EXT(N)HB[7:0] | | | | | | | | |
| 0x65 | EXT2 LOW BYTE | 7:0 | EXT(N)LB[2:0] | | | | | | | | |
| 0x66 | EXT3 HIGH BYTE | 7:0 | EXT(N)HB[7:0] | | | | | | | | |
| 0x67 | EXT3 LOW BYTE | 7:0 | EXT(N)LB[2:0] | | | | | | | | |
| 0x68 | EXT4 HIGH BYTE | 7:0 | EXT(N)HB[7:0] | | | | | | | | |
| 0x69 | EXT4 LOW BYTE | 7:0 | EXT(N)LB[2:0] | | | | | | | | |
| 0x6A | HOTTEST DIODE HIGH BYTE | 7:0 | HDHB[7:0] | | | | | | | | |
| 0x6B | HOTTEST DIODE LOW BYTE | 7:0 | HDLB[2:0] | | | | | | | | |
| 0x6C | HOTTEST STATUS | 7:0 | | | | E4HOT | E3HOT | E2HOT | E1HOT | IHOT | |
| 0x6D | HOTTEST CONFIG | 7:0 | | | REMHOT | E4ENB | E3ENB | E2ENB | E1ENB | IENB | |
| 0x6E ... 0xFC | Reserved | | | | | | | | | | |
| 0xFD | PRODUCT ID | 7:0 | PRODUCT_ID[7:0] | | | | | | | | |
| 0xFE | MANUFACTURER ID | 7:0 | MCHP_ID[7:0] | | | | | | | | |
| 0xFF | REVISION | 7:0 | REV[7:0] | | | | | | | | |

8.11. Data Read Interlock

When any Temperature Channel High Byte register is read, the corresponding low byte is copied into an internal ‘shadow’ register. The user is free to read the low byte at any time and be ensured that it corresponds to the previously read high byte. Regardless of whether the low byte is read or not, reading from the same high byte register again automatically refreshes this stored low byte data.

8.11.1. Internal Diode High Byte Data Register (Addresses 00h, 60h)

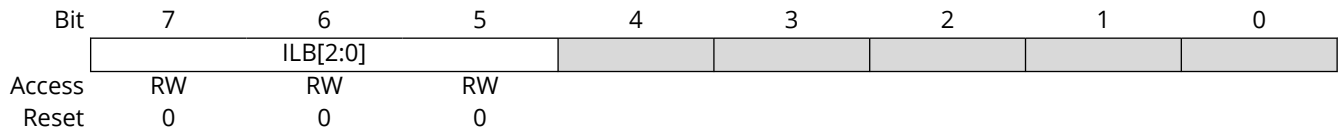
Name: INT HIGH BYTE
Offset: 0x00, 0x60

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|----|----|----|----|----|----|----|
| | IHB[7:0] | | | | | | | |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – IHB[7:0] Unsigned or unsigned offset depending on the RANGE bit.

8.11.2. Internal Diode Low Byte Data Register (Addresses 29h, 61h)

Name: INT LOW BYTE
Offset: 0x29, 0x61



Bits 7:5 – ILB[2:0] Fractional portion of the internal diode temperature to be added to the value at register 00h.

| Value | Description |
|-------|-------------|
| 111 | 0.875°C |
| 110 | 0.750°C |
| 101 | 0.625°C |
| 100 | 0.500°C |
| 011 | 0.375°C |
| 010 | 0.250°C |
| 001 | 0.125°C |
| 000 | 0.000°C |

8.11.3. External Diode High Byte Data Register (Addresses 01h, 23h, 2Ah, 32h, 62h, 64h, 66h and 68h)

Name: EXTn HIGH BYTE

Offset: 0x01, 0x23, 0x2A, 0x32, 0x62, 0x64, 0x66, 0x68

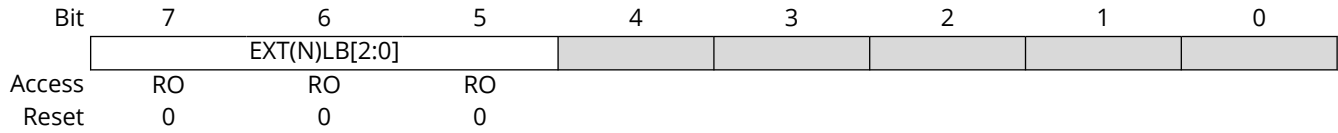
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------|----|----|----|----|----|----|----|
| | EXT(N)HB[7:0] | | | | | | | |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 - EXT(N)HB[7:0] Unsigned or unsigned offset depending on the RANGE bit.

8.11.4. External Diode Low Byte Data Register (Addresses 10h, 24h, 2Bh, 33h, 63h, 65h, 67h and 69h)

Name: EXTn LOW BYTE

Offset: 0x10, 0x24, 0x2B, 0x33, 0x63, 0x65, 0x67, 0x69



Bits 7:5 - EXT(N)LB[2:0] Fractional portion of internal diode temperature to be added to the value at register 00h.

| Value | Description |
|-------|-------------|
| 111 | 0.875°C |
| 110 | 0.750°C |
| 101 | 0.625°C |
| 100 | 0.500°C |
| 011 | 0.375°C |
| 010 | 0.250°C |
| 001 | 0.125°C |
| 000 | 0.000°C |

8.11.5. Diode Status Register (Address 02h)

Name: STATUS
Offset: 0x02

The Status register reports the operating status of the internal diode and external diode channels.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------|--------|------|------|-----|-------|-------|-------|
| | ROCF | HOTCHG | BUSY | HIGH | LOW | FAULT | ETHRM | ITHRM |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 – ROCF This bit indicates if External Diode 1 or 2 has exceeded the programmed Rate of Change limit.

| Value | Description |
|-------|---------------------|
| 1 | ROC above limit |
| 0 | ROC not above limit |

Bit 6 – HOTCHG This bit indicates if the hottest channel has changed from the previous temperature measurement.

| Value | Description |
|-------|---|
| 1 | The hottest channel has changed from the previous temperature measurement |
| 0 | The hottest channel has not changed from the previous temperature measurement |

Bit 5 – BUSY This bit indicates if the ADC is currently converting measured data.

| Value | Description |
|-------|---|
| 1 | The ADC is currently converting measured data |
| 0 | The ADC is not currently converting measured data |

Bit 4 – HIGH This bit indicates if a temperature channel exceeds its programmed high limit. When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

| Value | Description |
|-------|--|
| 1 | Reported temperature above the high limit |
| 0 | Reported temperature is not above the high limit |

Bit 3 – LOW This bit indicates if a temperature channel drops below its programmed low limit. When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

| Value | Description |
|-------|--|
| 1 | Reported temperature below, or equal to, the low limit |
| 0 | Reported temperature is not below the low limit |

Bit 2 – FAULT This bit indicates when a diode fault is detected. When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

| Value | Description |
|-------|---------------------------------|
| 1 | A diode fault has been detected |
| 0 | No fault reported |

Bit 1 – ETHRM This bit indicates that the external diode channel exceeds the programmed therm limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin. This bit will remain set until the $\overline{\text{THERM}}$ pin is released, at which point it will be automatically cleared.

| Value | Description |
|-------|---|
| 1 | Reported temperature above the high limit |

| Value | Description |
|-------|--|
| 0 | Reported temperature is not above the high limit |

Bit 0 - ITHRM This bit is set when the internal diode channel exceeds the programmed therm limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin. This bit will remain set until the $\overline{\text{THERM}}$ pin is released, at which point it will be automatically cleared.

| Value | Description |
|-------|--|
| 1 | Reported temperature above the high limit |
| 0 | Reported temperature is not above the high limit |

8.11.6. Configuration Register (Addresses 03h and 09h)

Name: CONFIG
Offset: 0x03, 0x09

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------|-----|--------|---------|---------|-------|--------|------|
| | MSKAL | R/S | AT/THM | RECD1/2 | RECD3/4 | RANGE | DA_ENA | APDD |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 – MSKAL Masks the $\overline{\text{ALERT}}$ pin from asserting when the $\overline{\text{ALERT}}$ pin is in Interrupt mode. This bit has no effect when the $\overline{\text{ALERT}}$ pin is in Comparator mode.

| Value | Description |
|-------|--|
| 1 | The $\overline{\text{ALERT}}$ pin is masked and will not be asserted for any interrupt condition when the $\overline{\text{ALERT}}$ pin is in Interrupt mode. The Status registers will be updated normally. |
| 0 | The $\overline{\text{ALERT}}$ pin is not masked. If any of the appropriate status bits are set, the $\overline{\text{ALERT}}$ pin will be asserted. |

Bit 6 – R/S Controls Run/Stop states.

| Value | Description |
|-------|---|
| 1 | The device is in Stop (Standby) state and not converting (unless a one-shot has been commanded) |
| 0 | The device is in Run (Active) state and converting on all channels |

Bit 5 – AT/THM Controls the operation of the $\overline{\text{ALERT}}$ pin. When the $\overline{\text{ALERT}}$ pin is in Comparator mode, each channel has a consecutive counter OR'ed to assert the $\overline{\text{ALERT}}$ pin. The $\overline{\text{ALERT}}$ pin is deasserted after one measurement is below the high limit minus the Therm Hysteresis.

| Value | Description |
|-------|---|
| 1 | The $\overline{\text{ALERT}}$ pin acts in Comparator mode as described in ALERT/THERM2 Pin in Therm Mode . In this mode, the MASK_ALL bit is ignored. |
| 0 | The $\overline{\text{ALERT}}$ pin acts in Interrupt mode as described in ALERT/THERM2 Pin Interrupt Mode |

Bit 4 – RECD1/2 Disables the Resistance Error Correction (REC) for the DP1/DN1 pins.

| Value | Description |
|-------|--|
| 1 | REC is disabled for the DP1/DN1 and DP2/DN2 pins |
| 0 | REC is enabled for the DP1/DN1 and DP2/DN2 pins |

Bit 3 – RECD3/4 Disables the Resistance Error Correction (REC) for the DP2/DN2 pins.

| Value | Description |
|-------|--|
| 1 | REC is disabled for the DP2/DN2 and DP4/DN4 pins |
| 0 | REC is enabled for the DP2/DN2 and DP4/DN4 pins |

Bit 2 – RANGE Configures the measurement range and data format of the temperature channels.

| Value | Description |
|-------|--|
| 1 | The temperature measurement range is -64°C to +191.875°C and the data format is offset binary (see Table 7-1) |
| 0 | The temperature measurement range is 0°C to +127.875°C and the data format is binary |

Bit 1 – DA_ENA Enables the dynamic averaging feature on all temperature channels.

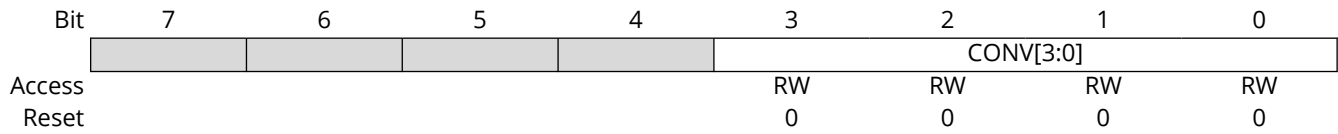
| Value | Description |
|-------|--|
| 1 | The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor based on the conversion rate, as shown in Table 7-4 . |
| 0 | The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates, this averaging factor will be reduced, as shown in Table 7-5 . |

Bit 0 – APDD Disables the anti-parallel diode operation, allowing each APD pin set to bias and measure only one diode.

| Value | Description |
|-------|---|
| 1 | Anti-Parallel Diode mode is disabled. Only one external diode will be measured on the DP1/DN1 and DP2/DN2 pins. |
| 0 | Anti-Parallel Diode mode is enabled. Two external diodes will be measured on the DP1/DN1 and DP2/DN2 pins. |

8.11.7. Temperature Conversion Rate Register (Addresses 04h and 0Ah)

Name: CONVERT
Offset: 0x04, 0x0A



Bits 3:0 – CONV[3:0] The Conversion Rate register controls how often the temperature measurement channels are updated and compared to the limits. This register is fully accessible at either address. It determines the conversion rate, as shown in [Table 7-4](#).

8.11.8. Internal Diode High Limit Register (Addresses 05h and 0Bh)

Name: INT DIODE HIGH LIMIT
Offset: 0x05, 0x0B

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------|----|----|----|----|----|----|----|
| | IDHL[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – IDHL[7:0] Unsigned or unsigned offset depending on the RANGE bit.

8.11.9. Internal Diode Low Limit Register (Addresses 06h and 0Ch)

Name: INT DIODE LOW LIMIT
Offset: 0x06, 0x0C

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------|----|----|----|----|----|----|----|
| | IDLL[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – IDLL[7:0] Integer value of the internal diode temperature reading.

8.11.10. Ext High Limit High Byte Register (Addresses 07h, 0Dh, 15h, 2Ch and 34h)

Name: EXT HIGH LIMIT HIGH BYTE
Offset: 0x07, 0x0D, 0x15, 0x2C, 0x34

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------------|----|----|----|----|----|----|----|
| | EXT(N)HLHB[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – EXT(N)HLHB[7:0] Integer value of the External Diode n temperature reading, where n = 1 to 4, depending on the device.

8.11.11. Ext High Limit Low Byte Register (Addresses 13h, 17h, 2Eh and 36h)

Name: EXT HIGH LIMIT LOW BYTE
Offset: 0x13, 0x17, 0x2E, 0x36

| | | | | | | | | |
|--------|-----------------|----|----|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | EXT(N)HLLB[2:0] | | | | | | | |
| Access | RW | RW | RW | | | | | |
| Reset | 0 | 0 | 0 | | | | | |

Bits 7:5 – EXT(N)HLLB[2:0] Fractional portion of the high limit temperature to be added to the value in the respective high byte registers.

| Value | Description |
|-------|-------------|
| 111 | 0.875°C |
| 110 | 0.750°C |
| 101 | 0.625°C |
| 100 | 0.500°C |
| 011 | 0.375°C |
| 010 | 0.250°C |
| 001 | 0.125°C |
| 000 | 0.000°C |

8.11.12. Ext(n) Low Limit High Byte Register (Addresses 08h, 0Eh, 16h, 2Dh and 35h)

Name: EXT LOW LIMIT HIGH BYTE
Offset: 0x08, 0x0E, 0x16, 0x2D, 0x35

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------------|----|----|----|----|----|----|----|
| | EXT(N)LLHB[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – EXT(N)LLHB[7:0] Integer portion of External Diode n low limit temperature, where n = 1 to 4, depending on the device.

8.11.13. Ext(n) Low Limit Low Byte Register (Addresses 14h, 18h, 2Fh and 37h)

Name: EXT LOW LIMIT LOW BYTE
Offset: 0x14, 0x18, 0x2F, 0x37

| | | | | | | | | |
|--------|----------------|----|----|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | EXT(N)LLL[2:0] | | | | | | | |
| Access | RW | RW | RW | | | | | |
| Reset | 0 | 0 | 0 | | | | | |

Bits 7:5 – EXT(N)LLL[2:0] Fractional portion of the low limit temperature to be added to the value in the respective high byte registers, where n = 1 to 4.

| Value | Description |
|-------|-------------|
| 111 | 0.875°C |
| 110 | 0.750°C |
| 101 | 0.625°C |
| 100 | 0.500°C |
| 011 | 0.375°C |
| 010 | 0.250°C |
| 001 | 0.125°C |
| 000 | 0.000°C |

8.11.14. Scratchpad Register (Addresses 11h and 12h)

Name: SCRTCHPD
Offset: $0x11 + (n-1)*0x01$ [n=1..2]

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------------|----|----|----|----|----|----|----|
| | SPD(N)[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – SPD(N)[7:0] User temporary storage registers, where n = 1 to 2.

8.11.15. One-Shot Register (Address 0Fh)

Name: ONE SHOT
Offset: 0x0F

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------|----|----|----|----|----|----|----|
| | ONSH[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – ONSH[7:0] When the device is in the Standby state, writing to the One-Shot register will initiate a conversion cycle and update the temperature measurements.

Writing to the One-Shot register while the device is in the Active state or when the BUSY bit is set in the Status register (Address 02h) will have no effect.

8.11.16. Software Thermal Shutdown Configuration Register (Address 1Dh)

Name: SW THERMAL SHUTDOWN CONFIG
Offset: 0x1d

| | | | | | | | | |
|--------|---|---|---|-------|-------|-------|-------|--------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | E4SYS | E3SYS | E2SYS | E1SYS | INTSYS |
| Access | | | | RW | RW | RW | RW | |
| Reset | | | | 0 | 0 | 0 | 0 | |

Bit 4 – E4SYS Configures the External Diode 4 channel to assert the $\overline{\text{SYS_SHDN}}$ pin based on the hardware thermal shutdown limit.

| Value | Description |
|-------|--|
| 0 | The External Diode 4 channel is not linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature exceeds the hardware thermal shutdown limit, the E4THRM status bit is set, but the $\overline{\text{SYS_SHDN}}$ pin is not asserted. |
| 1 | The External Diode 4 channel is linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature exceeds the hardware thermal shutdown limit, the E4THRM status bit is set and the $\overline{\text{SYS_SHDN}}$ pin is asserted. It will remain asserted until the temperature drops below its Therm Limit minus the Therm Hysteresis. |

Bit 3 – E3SYS Configures the External Diode 3 channel to assert the $\overline{\text{SYS_SHDN}}$ pin based on the hardware thermal shutdown limit.

| Value | Description |
|-------|--|
| 0 | The External Diode 3 channel is not linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature exceeds the hardware thermal shutdown limit, the E3THRM status bit is set, but the $\overline{\text{SYS_SHDN}}$ pin is not asserted. |
| 1 | The External Diode 3 channel is linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature exceeds the hardware thermal shutdown limit, the E3THRM status bit is set and the $\overline{\text{SYS_SHDN}}$ pin is asserted. It will remain asserted until the temperature drops below its Therm Limit minus the Therm Hysteresis. |

Bit 2 – E2SYS Configures the External Diode 2 channel to assert the $\overline{\text{SYS_SHDN}}$ pin based on the hardware thermal shutdown limit.

| Value | Description |
|-------|--|
| 0 | The External Diode 2 channel is not linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature exceeds the hardware thermal shutdown limit, the E2THRM status bit is set, but the $\overline{\text{SYS_SHDN}}$ pin is not asserted. |
| 1 | The External Diode 2 channel is linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature exceeds the hardware thermal shutdown limit, the E2THRM status bit is set and the $\overline{\text{SYS_SHDN}}$ pin is asserted. It will remain asserted until the temperature drops below its Therm Limit minus the Therm Hysteresis. |

Bit 1 – E1SYS Configures the External Diode 1 channel to assert the $\overline{\text{SYS_SHDN}}$ pin based on the hardware thermal shutdown limit.

| Value | Description |
|-------|--|
| 0 | The External Diode 1 channel is not linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature exceeds its Therm Limit, the E1THRM status bit is set, but the $\overline{\text{SYS_SHDN}}$ pin is not asserted. |
| 1 | The External Diode 1 channel is linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature exceeds the hardware thermal shutdown limit, the E2THRM status bit is set and the $\overline{\text{SYS_SHDN}}$ pin is asserted. It will remain asserted until the temperature drops below its Therm Limit minus the Therm Hysteresis. |

Bit 0 – INTSYS Configures the internal diode channel to assert the $\overline{\text{SYS_SHDN}}$ pin based on the hardware thermal shutdown limit.

| Value | Description |
|-------|--|
| 0 | The internal diode channel is not linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature exceeds the hardware thermal shutdown limit, the INTTHRM status bit is set, but the $\overline{\text{SYS_SHDN}}$ pin is not asserted. |

| Value | Description |
|-------|---|
| 1 | The internal diode channel is linked to the $\overline{\text{SYS_SHDN}}$ pin. If the temperature exceeds the hardware thermal shutdown limit, the INTTHRM status bit is set and the $\overline{\text{SYS_SHDN}}$ pin is asserted. It will remain asserted until the temperature drops below its Therm Limit minus the Therm Hysteresis. |

8.11.17. Hardware Thermal Shutdown Limit Register (Address 1Eh)

Name: HARDWARE THERMAL SHUTDOWN LIMIT
Offset: 0x1E

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|----|----|----|----|----|----|----|
| | SSDNL[7:0] | | | | | | | |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – SSDNL[7:0] Returns the hardware thermal shutdown limit selected by the value of the pull-up resistors on the `ALERT` and `SYS_SHDN` pins. The data represents the hardware set temperature in °C using the active temperature setting set by the `RANGE` bit in the Configuration register. See [CONFIG](#) for the data format. When the External Diode 1 or internal diode for the MCP9822 temperature exceeds this limit, the `SYS_SHDN` pin is asserted and will remain asserted until the External Diode 1 or internal diode for the MCP9822 temperature drops below this limit minus 10°C. For additional information, see [Table 7-3](#).

8.11.18. Ext(n) Therm Limit Register (Addresses 19h, 1Ah, 30h and 38h)

Name: EXTn THERM LIMIT
Offset: 0x19, 0x1A, 0x30, 0x38

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------------|----|----|----|----|----|----|----|
| | EXT(N)THL[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – EXT(N)THL[7:0] External Diode n THERM limits, where n = 1 to 4.

8.11.19. Internal Diode Therm Limit Register (Address 20h)

Name: INT DIODE THERM LIMIT
Offset: 0x20

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|----|----|----|----|----|----|----|
| | IDTHL[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – IDTHL[7:0] Internal diode THERM limits.

8.11.20. $\overline{\text{Therm}}$ Limit Hysteresis Register (Address 21h)

Name: THRM HYS
Offset: 0x21

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|----|----|----|----|----|----|----|
| | THRMH[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

Bits 7:0 - THRMH[7:0] $\overline{\text{THERM}}$ limit hysteresis.

8.11.21. External Diode Fault Status Register (Address 1Bh)

Name: EXTERNAL DIODE FAULT STATUS
Offset: 0x1B

Note: The External Diode Fault register indicates which of the external diodes caused the FAULT bit in the Status register to be set. This register is cleared when it is read.

| | | | | | | | | |
|--------|---|---|---|-------|-------|-------|-------|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | E4FLT | E3FLT | E2FLT | E1FLT | |
| Access | | | | RC | RC | RC | RC | |
| Reset | | | | 0 | 0 | 0 | 0 | |

Bit 4 – E4FLT This bit is set if the External Diode 4 channel reports a diode fault.

| Value | Description |
|-------|-------------------------------|
| 1 | Diode fault condition present |
| 0 | No diode fault present |

Bit 3 – E3FLT This bit is set if the External Diode 3 channel reports a diode fault.

| Value | Description |
|-------|-------------------------------|
| 1 | Diode fault condition present |
| 0 | No diode fault present |

Bit 2 – E2FLT This bit is set if the External Diode 2 channel reports a diode fault.

| Value | Description |
|-------|-------------------------------|
| 1 | Diode fault condition present |
| 0 | No diode fault present |

Bit 1 – E1FLT This bit is set if the External Diode 1 channel reports a diode fault.

| Value | Description |
|-------|-------------------------------|
| 1 | Diode fault condition present |
| 0 | No diode fault present |

8.11.22. Diode Fault Mask Register (Address 1Fh)

Name: DIODE FAULT MASK
Offset: 0x1F

Note: The Channel Mask register controls individual channel masking. When a channel is masked, the ALERT pin will not be asserted when the masked channel reads a diode fault or out-of-limit error. The channel mask does not mask the THERM pin.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---|---|---|--------|--------|--------|--------|---------|
| | | | | E4MASK | E3MASK | E2MASK | E1MASK | INTMASK |
| Access | | | | RW | RW | RW | RW | RW |
| Reset | | | | 0 | 0 | 0 | 0 | 0 |

Bit 4 – E4MASK Masks the $\overline{\text{ALERT}}$ pin from asserting when the External Diode 4 channel is out-of-limit or reports a diode fault.

| Value | Description |
|-------|---|
| 1 | The External Diode 4 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault |
| 0 | The External Diode 4 channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault |

Bit 3 – E3MASK Masks the $\overline{\text{ALERT}}$ pin from asserting when the External Diode 3 channel is out-of-limit or reports a diode fault.

| Value | Description |
|-------|---|
| 1 | The External Diode 3 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault |
| 0 | The External Diode 3 channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault |

Bit 2 – E2MASK Masks the $\overline{\text{ALERT}}$ pin from asserting when the External Diode 2 channel is out-of-limit or reports a diode fault.

| Value | Description |
|-------|---|
| 1 | The External Diode 2 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault |
| 0 | The External Diode 2 channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault |

Bit 1 – E1MASK Masks the $\overline{\text{ALERT}}$ pin from asserting when the External Diode 1 channel is out-of-limit or reports a diode fault.

| Value | Description |
|-------|---|
| 1 | The External Diode 1 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault |
| 0 | The External Diode 1 channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault |

Bit 0 – INTMASK Masks the $\overline{\text{ALERT}}$ pin from asserting when the internal diode temperature is out-of-limit.

| Value | Description |
|-------|--|
| 1 | The internal diode channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit |
| 0 | The internal diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit |

8.11.23. Consecutive Alert Register (Address 22h)

Name: CONSEC ALERT
Offset: 0x22

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------|------------|----|----|------------|----|----|---|
| | TMOUT | CTHRM[2:0] | | | CALRT[2:0] | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | |
| Reset | 0 | 1 | 1 | 1 | 0 | 0 | 0 | |

Bit 7 – TMOUT Enables the time-out and Idle functionality of the I²C protocol.

| Value | Description |
|-------|---|
| 1 | The I ² C time-out and Idle functionality are enabled. The I ² C interface will time-out if the clock line is held low for longer than 30 ms. Likewise, it will reset if both the data and clock lines are held high for longer than 200 μs. |
| 0 | The I ² C time-out and Idle functionality are disabled. The I ² C interface will not time-out if the clock line is held low for longer than 30 ms. Likewise, it will not reset if both the data and clock lines are held high for longer than 200 μs. This is used for I ² C compliance. |

Bits 6:4 – CTHR[M][2:0] Determines the number of consecutive measurements that must exceed the corresponding therm limit before the $\overline{\text{THERM}}$ pin is asserted.

| Value | Description |
|-------|-------------|
| 000 | 1 |
| 001 | 2 |
| 011 | 3 |
| 111 | 4 |

Bits 3:1 – CALRT[2:0] Determines the number of consecutive measurements that must exceed the corresponding therm limit before the $\overline{\text{ALERT}}$ pin is asserted.

| Value | Description |
|-------|-------------|
| 000 | 1 |
| 001 | 2 |
| 011 | 3 |
| 111 | 4 |

8.11.24. Ext(n) Beta Compensation Configuration Register (Address 25h and 26h)

Name: EXTn BETA CONFIG
Offset: 0x25, 0x26

| | | | | | | | | |
|--------|---|---|---|---------|--------------|----|----|----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | ENBL(N) | BETA(N)[3:0] | | | |
| Access | | | | RW | RO | RO | RO | RO |
| Reset | | | | 0 | 0 | 0 | 0 | 0 |

Bit 4 – ENBL(N) Enables the beta compensation factor auto-detection function; x = 1 or 2, depending on the device.

| Value | Description |
|-------|--|
| 1 | Auto-beta detection for External Diode x is enabled |
| 0 | Auto-beta detection for External Diode x is disabled |

Bits 3:0 – BETA(N)[3:0] These bits always reflect the current beta configuration settings. If auto-detection circuitry is enabled, these bits will be updated automatically and writing to these bits will have no effect. See [Table 7-7](#) for details.

8.11.25. Ext (n) Programmable Ideality Factor Register (Address 27h, 28h, 31h and 39h)

Name: EXTn IDEALITY FACTOR
Offset: 0x27, 0x28, 0x31, 0x39

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---|---|---------------|----|----|----|----|----|
| | | | IDEAL(N)[5:0] | | | | | |
| Access | | | RW | RW | RW | RW | RW | RW |
| Reset | | | 0 | 1 | 0 | 0 | 1 | 0 |

Bits 5:0 – IDEAL(N)[5:0] External Diode n ideality factor, where n = 1 to 4, depending on the device.
See [Table 7-8](#) or [Table 7-9](#) for details.

8.11.26. High Limit Status Register (Address 3Ah)

Name: HIGH LIMIT STATUS
Offset: 0x3A

| | | | | | | | | |
|--------|---|---|---|--------|--------|--------|--------|-------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | E4HIGH | E3HIGH | E2HIGH | E1HIGH | IHIGH |
| Access | | | | RC | RC | RC | RC | RC |
| Reset | | | | 0 | 0 | 0 | 0 | 0 |

Bit 4 – E4HIGH

This bit is set when the External Diode 4 channel exceeds its programmed high limit. Reading this register will also clear the HIGH bit.

| Value | Description |
|-------|-------------------------|
| 1 | High limit exceeded |
| 0 | High limit not exceeded |

Bit 3 – E3HIGH

This bit is set when the External Diode 3 channel exceeds its programmed high limit. Reading this register will also clear the HIGH bit.

| Value | Description |
|-------|-------------------------|
| 1 | High limit exceeded |
| 0 | High limit not exceeded |

Bit 2 – E2HIGH This bit is set when the External Diode 2 channel exceeds its programmed high limit. Reading this register will also clear the HIGH bit.

| Value | Description |
|-------|-------------------------|
| 1 | High limit exceeded |
| 0 | High limit not exceeded |

Bit 1 – E1HIGH This bit is set when the External Diode 1 channel exceeds its programmed high limit. Reading this register will also clear the HIGH bit.

| Value | Description |
|-------|-------------------------|
| 1 | High limit exceeded |
| 0 | High limit not exceeded |

Bit 0 – IHIGH This bit is set when the internal diode exceeds its programmed high limit. Reading this register will also clear the HIGH bit.

| Value | Description |
|-------|-------------------------|
| 1 | High limit exceeded |
| 0 | High limit not exceeded |

8.11.27. Low Limit Status Register (Address 3Bh)

Name: LOW LIMIT STATUS
Offset: 0x3B

| | | | | | | | | |
|--------|---|---|---|-------|-------|-------|-------|------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | E4LOW | E3LOW | E2LOW | E1LOW | ILOW |
| Access | | | | RC | RC | RC | RC | RC |
| Reset | | | | 0 | 0 | 0 | 0 | 0 |

Bit 4 – E4LOW This bit is set when the External Diode 4 channel drops below its programmed low limit. Reading from the register will also clear the LOW status bit in the Status register.

| Value | Description |
|-------|------------------------|
| 1 | Low limit exceeded |
| 0 | Low limit not exceeded |

Bit 3 – E3LOW This bit is set when the External Diode 3 channel drops below its programmed low limit. Reading from the register will also clear the LOW status bit in the Status register.

| Value | Description |
|-------|------------------------|
| 1 | Low limit exceeded |
| 0 | Low limit not exceeded |

Bit 2 – E2LOW This bit is set when the External Diode 2 channel drops below its programmed low limit. Reading this register will also clear the LOW bit.

| Value | Description |
|-------|------------------------|
| 1 | Low limit exceeded |
| 0 | Low limit not exceeded |

Bit 1 – E1LOW This bit is set when the External Diode 1 channel drops below its programmed low limit. Reading this register will also clear the LOW bit.

| Value | Description |
|-------|------------------------|
| 1 | Low limit exceeded |
| 0 | Low limit not exceeded |

Bit 0 – ILOW This bit is set when the internal diode drops below its programmed low limit. Reading this register will also clear the LOW bit.

| Value | Description |
|-------|------------------------|
| 1 | Low limit exceeded |
| 0 | Low limit not exceeded |

8.11.28. Therm High Limit Status Register (Address 3Ch)

Name: THERM LIMIT STATUS
Offset: 0x3C

Note: The Therm Limit Status register contains the status bits that are set when a temperature channel's therm limit is exceeded. If any of these bits are set, the THERM Status bit in the Status register is also set. Reading from the Therm Limit Status register will not clear the status bits. Once the temperature drops below the therm limit minus the therm hysteresis, the corresponding status bits will be automatically cleared. The THERM bit in the Status register will be cleared when all individual channel THERM bits are cleared.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---|---|---|---------|---------|---------|---------|--------|
| | | | | E4THERM | E3THERM | E2THERM | E1THERM | ITHERM |
| Access | | | | RO | RO | RO | RO | RO |
| Reset | | | | 0 | 0 | 0 | 0 | 0 |

Bit 4 – E4THERM

This bit is set when the External Diode 4 channel exceeds its programmed therm limit. When set, this bit will assert the THERM pin.

| Value | Description |
|-------|------------------------|
| 1 | THERM pin asserted |
| 0 | THERM pin not asserted |

Bit 3 – E3THERM

This bit is set when the External Diode 3 channel exceeds its programmed therm limit. When set, this bit will assert the THERM pin.

| Value | Description |
|-------|------------------------|
| 1 | THERM pin asserted |
| 0 | THERM pin not asserted |

Bit 2 – E2THERM

This bit is set when the External Diode 2 channel exceeds its programmed therm limit. When set, this bit will assert the THERM pin.

| Value | Description |
|-------|------------------------|
| 1 | THERM pin asserted |
| 0 | THERM pin not asserted |

Bit 1 – E1THERM

This bit is set when the External Diode 1 channel exceeds its programmed therm limit. When set, this bit will assert the THERM pin.

| Value | Description |
|-------|------------------------|
| 1 | THERM pin asserted |
| 0 | THERM pin not asserted |

Bit 0 – ITHERM

This bit is set when the internal diode channel exceeds its programmed therm limit. When set, this bit will assert the THERM pin.

| Value | Description |
|-------|------------------------|
| 1 | THERM pin asserted |
| 0 | THERM pin not asserted |

8.11.29. Rate of Change Gain Register (Address 3Dh)

Name: ROC GAIN
Offset: 0x3D

| | | | | | | | | |
|--------|-----------|----|----|----|----|----|----|----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | RC1G[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 5:3 – RC2/3G[2:0] This represents the binary gain applied to the difference equation.

| Value | Description |
|-------|-------------|
| 0 | 1 |
| 1 | 2 |
| 2 | 4 |
| 3 | 8 |
| 4 | 16 |
| 5 | 32 |
| 6 | 64 |
| 7 | 128 |

Bits 7:0 – RC1G[7:0] This represents the binary gain applied to the difference equation.

| Value | Description |
|-------|-------------|
| 0 | 1 |
| 1 | 2 |
| 2 | 4 |
| 3 | 8 |
| 4 | 16 |
| 5 | 32 |
| 6 | 64 |
| 7 | 128 |

8.11.30. Rate of Change Configuration Register (Address 3Eh)

Name: ROC CONFIG
Offset: 0x3E

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---|---|--------|---------|-------|-----------|----|----|
| | | | EN_ROC | MASK2/3 | MASK1 | RCHY[2:0] | | |
| Access | | | RW | RW | RW | RW | RW | RW |
| Reset | | | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5 – EN_ROC Enables the Rate of Change calculations.

| Value | Description |
|-------|-------------------------|
| 1 | Rate of Change enabled |
| 0 | Rate of Change disabled |

Bit 4 – MASK2/3

Masks an event from setting the $\overline{\text{ALERT}}$ pin on Channel 2.

| Value | Description |
|-------|---|
| 1 | Event is masked |
| 0 | Event will assert the $\overline{\text{ALERT}}$ pin |

Bit 3 – MASK1

Masks an event from setting the $\overline{\text{ALERT}}$ pin on Channel 1.

| Value | Description |
|-------|---|
| 1 | Event is masked |
| 0 | Event will assert the $\overline{\text{ALERT}}$ pin |

Bits 2:0 – RCHY[2:0] Hysteresis setting for Rate of Change slope reversal. Deviations greater than this setting will result in the bit being set.

| Value | Description |
|-------|-------------|
| 111 | 4.000°C |
| 110 | 3.000°C |
| 101 | 2.000°C |
| 100 | 1.000°C |
| 011 | 0.500°C |
| 010 | 0.250°C |
| 001 | 0.125°C |
| 000 | 0.000°C |

8.11.31. Rate of Change Status Register (Address 3Fh)

Name: ROC STATUS
Offset: 0x3F

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------|-------|---------|-------|---------|-------|---------|-------|
| | SLCG2/3 | SLCG1 | R2/3ODD | R1ODD | RC2/3HI | RC1HI | RC2/3LO | RC1LO |
| Access | RO | RO | RO | RO | RC | RC | RC | RC |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 – SLCG2/3 Reports a change in slope during the Rate of Change calculation for External Channel 2.

| Value | Description |
|-------|-------------------------|
| 1 | Slope changed direction |
| 0 | Monotonic slope |

Bit 6 – SLCG1 Reports a change in slope during the Rate of Change calculation for External Channel 1.

| Value | Description |
|-------|-------------------------|
| 1 | Slope changed direction |
| 0 | Monotonic slope |

Bit 5 – R2/3ODD Indicates whether the number of slope reversals is even or odd.

| Value | Description |
|-------|---|
| 1 | Odd number of slope reversals during the sampling period |
| 0 | Even number of slope reversals during the sampling period |

Bit 4 – R1ODD Indicates whether the number of slope reversals was even or odd.

| Value | Description |
|-------|---|
| 1 | Odd number of slope reversals during the sampling period |
| 0 | Even number of slope reversals during the sampling period |

Bit 3 – RC2/3HI This bit is set when the Rate of Change results for External Diode 2 exceed its programmed limit.

| Value | Description |
|-------|-------------------------|
| 1 | High limit exceeded |
| 0 | High limit not exceeded |

Bit 2 – RC1HI This bit is set when the Rate of Change results for External Diode 1 exceed its programmed limit.

| Value | Description |
|-------|-------------------------|
| 1 | High limit exceeded |
| 0 | High limit not exceeded |

Bit 1 – RC2/3LO This bit is set when the Rate of Change results for External Diode 2 exceed its programmed limit (applies when slope limit is negative).

| Value | Description |
|-------|------------------------|
| 1 | Low limit exceeded |
| 0 | Low limit not exceeded |

Bit 0 – RC1LO This bit is set when the Rate of Change results for External Diode 1 exceed its programmed limit (applies when slope limit is negative).

| Value | Description |
|-------|------------------------|
| 1 | Low limit exceeded |
| 0 | Low limit not exceeded |

8.11.32. Rate of Change Results High Byte Register (n) (Addresses 40h and 44h)

Name: R RESH
Offset: $0x40 + (n-1)*0x04$ [n=1..2]

| | | | | | | | | |
|--------|-------------|----|----|----|----|----|----|----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | R(N)RH[7:0] | | | | | | | |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – R(N)RH[7:0] This is the high byte of the result of the most recent Rate of Change calculations, where n = 1 or 2, corresponding to the remote diode channel.

8.11.33. Rate of Change Results Low Byte Register (Address 45h)

Name: R2/3 RESL
Offset: 0x45

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------|----|----|----|------------|----|----|----|
| | R2/3_RL[3:0] | | | | R1_RL[3:0] | | | |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:4 – R2/3_RL[3:0] This is the low byte of the result of the most recent Rate of Change calculations for remote Diode Channel 2.

Bits 3:0 – R1_RL[3:0] This is the low byte of the result of the most recent Rate of Change calculations for remote Diode Channel 1.

8.11.34. Rate of Change Alert Limit High Byte Register (n) (Addresses 41h and 46h)**Name:** R LIMH**Offset:** $0x41 + (n-1)*0x05$ [n=1..2]

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------|----|----|----|----|----|----|----|
| | R(N)LIMH[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – R(N)LIMH[7:0]

This is the high byte ROC $\overline{\text{ALERT}}$ limit. If the ROC results exceed this value and the MASK bit is not set, the $\overline{\text{ALERT}}$ pin will assert; where n = 1 or 2, corresponding to the remote diode channel.

8.11.35. Rate of Change Alert Limit Low Byte Register (n) (Address 42h and 47h)

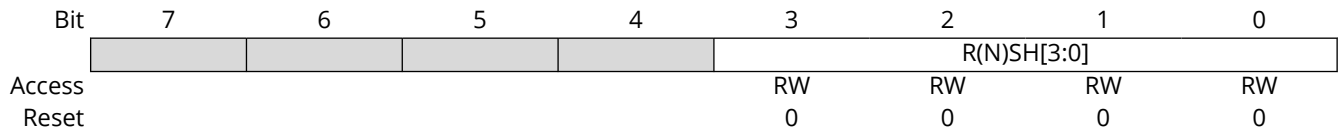
Name: R LIML
Offset: $0x42 + (n-1)*0x05$ [n=1..2]

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------|----|----|----|---|---|---|---|
| | R(N)LIML[3:0] | | | | | | | |
| Access | RW | RW | RW | RW | | | | |
| Reset | 0 | 0 | 0 | 0 | | | | |

Bits 7:4 – R(N)LIML[3:0] This is the low byte ROC $\overline{\text{ALERT}}$ limit, where n = 1 or 2, corresponding to the remote diode channel.

8.11.36. Rate of Change Samples Register (Address 43h and 48h)

Name: R SMPL
Offset: $0x43 + (n-1)*0x05$ [n=1..2]



Bits 3:0 – R(N)SH[3:0] This represents the high byte of the number of samples taken for the Rate of Change calculation, where n = 1 or 2, corresponding to the remote diode channel.

| Value | Description |
|---------|-------------|
| 0x0 | 2 Samples |
| 0x1 | 3 Samples |
| 0x2 | 5 Samples |
| 0x3 | 9 Samples |
| 0x4 | 17 Samples |
| 0x5 | 33 Samples |
| 0x6 | 65 Samples |
| 0x7 | 129 Samples |
| 0x8–0xF | 257 Samples |

8.11.37. Sample Period Max Temperature High Byte Data Register (Address 49h and 4Bh)

Name: PER MAXTH
Offset: 0x49 + (n-1)*0x02 [n=1..2]

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------|----|----|----|----|----|----|----|
| | GM(N)HB[7:0] | | | | | | | |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – GM(N)HB[7:0] Integer value of the internal diode maximum temperature reading within the sample period.

8.11.38. Sample Period Max Temperature Low Byte Data Register (Address 4Ah and 4Ch)

Name: PER MAXTL
Offset: 0x4A + n*0x02 [n=0..1]

| | | | | | | | | |
|--------|-------------|----|----|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | PM(N)L[2:0] | | | | | | | |
| Access | RO | RO | RO | | | | | |
| Reset | 0 | 0 | 0 | | | | | |

Bits 7:5 – PM(N)L[2:0] Fractional portion of the internal diode temperature to be added to the value at register 00h.

| Value | Description |
|-------|-------------|
| 111 | 0.875°C |
| 110 | 0.750°C |
| 101 | 0.625°C |
| 100 | 0.500°C |
| 011 | 0.375°C |
| 010 | 0.250°C |
| 001 | 0.125°C |
| 000 | 0.000°C |

8.11.39. Global Max Temperature High Byte Register (Address 4Dh and 4Fh)

Name: GBL MAXTH
Offset: 0x4D + (n-1)*0x02 [n=1..2]

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------|----|----|----|----|----|----|----|
| | GM(N)HB[7:0] | | | | | | | |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7:0 – GM(N)HB[7:0] Integer value of the External Diode n’s maximum temperature reading within the sample period, where n = 1 or 2, corresponding to External Diode 1 or 2.

8.11.40. Sample Period Max Temperature Low Byte Data Register (Address 4Eh and 50h)

Name: GBL MAXTL
Offset: 0x4E + (n-1)*0x02 [n=1..2]

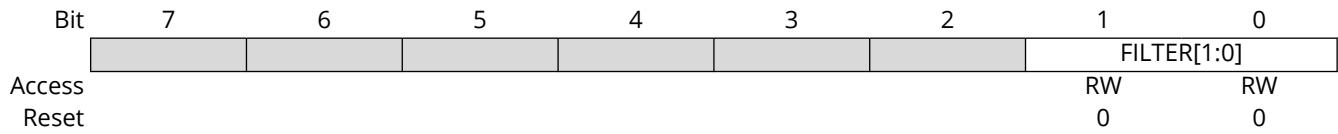
| | | | | | | | | |
|--------|--------------|----|----|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | GM(N)LB[2:0] | | | | | | | |
| Access | RO | RO | RO | | | | | |
| Reset | 0 | 0 | 0 | | | | | |

Bits 7:5 – GM(N)LB[2:0] Fractional portion of the External Diode n’s maximum temperature reading within the sample period, where n = 1 or 2, corresponding to External Diode 1 or 2.

| Value | Description |
|-------|-------------|
| 111 | 0.875°C |
| 110 | 0.750°C |
| 101 | 0.625°C |
| 100 | 0.500°C |
| 011 | 0.375°C |
| 010 | 0.250°C |
| 001 | 0.125°C |
| 000 | 0.000°C |

8.11.41. Filter Selection Register (Address 51h)

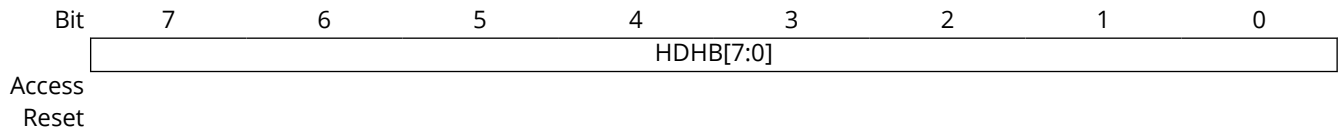
Name: FILTER SEL
Offset: 0x51



Bits 1:0 – FILTER[1:0] Control the level of digital filtering applied to the external diode temperature measurement, as shown in [Table 5-5](#).

8.11.42. Hottest Diode Temperature High Byte Register (Address 6Ah)

Name: HOTTEST DIODE HIGH BYTE
Offset: 0x6A



Bits 7:0 – HDHB[7:0] Integer value of the hottest diode from the most recent samples.

8.11.43. Hottest Diode Temperature Low Byte Register (Address 6Bh)

Name: HOTTEST DIODE LOW BYTE
Offset: 0x6B

| | | | | | | | | |
|--------|-----------|----|----|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | HDLB[2:0] | | | | | | | |
| Access | RO | RO | RO | | | | | |
| Reset | 0 | 0 | 0 | | | | | |

Bits 7:5 – HDLB[2:0] Fractional portion of the hottest diode for the most recent sample period.

| Value | Description |
|-------|-------------|
| 111 | 0.875°C |
| 110 | 0.750°C |
| 101 | 0.625°C |
| 100 | 0.500°C |
| 011 | 0.375°C |
| 010 | 0.250°C |
| 001 | 0.125°C |
| 000 | 0.000°C |

8.11.44. Hottest Diode Status Register (Address 6Ch)

Name: HOTTEST STATUS
Offset: 0x6C

| | | | | | | | | |
|--------|---|---|---|-------|-------|-------|-------|------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | E4HOT | E3HOT | E2HOT | E1HOT | IHOT |
| Access | | | | RO | RO | RO | RO | RO |
| Reset | | | | 0 | 0 | 0 | 0 | 0 |

Bit 4 – E4HOT Indicates External Diode 4 is the hottest.

| Value | Description |
|-------|-------------------------------------|
| 1 | External Diode 4 is hottest |
| 0 | External Diode 4 is not the hottest |

Bit 3 – E3HOT Indicates External Diode 3 is the hottest.

| Value | Description |
|-------|-------------------------------------|
| 1 | External Diode 3 is hottest |
| 0 | External Diode 3 is not the hottest |

Bit 2 – E2HOT Indicates External Diode 2 is the hottest.

| Value | Description |
|-------|-------------------------------------|
| 1 | External Diode 2 is hottest |
| 0 | External Diode 2 is not the hottest |

Bit 1 – E1HOT Indicates External Diode 1 is the hottest.

| Value | Description |
|-------|-------------------------------------|
| 1 | External Diode 1 is hottest |
| 0 | External Diode 1 is not the hottest |

Bit 0 – IHOT Indicates internal diode is the hottest.

| Value | Description |
|-------|-----------------------------------|
| 1 | Internal diode is hottest |
| 0 | Internal diode is not the hottest |

8.11.45. Hottest Diode Configuration Register (Address 6Dh)

Name: HOTTEST CONFIG
Offset: 0x6D

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---|---|--------|-------|-------|-------|-------|------|
| | | | REMHOT | E4ENB | E3ENB | E2ENB | E1ENB | IENB |
| Access | | | RW | RW | RW | RW | RW | RW |
| Reset | | | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5 – REMHOT Enables the Remember Hottest function, so if the hottest diode changes, the $\overline{\text{ALERT}}$ pin is set.

| Value | Description |
|-------|------------------------------------|
| 1 | Remember Hottest function enabled |
| 0 | Remember Hottest function disabled |

Bit 4 – E4ENB Enables External Diode 4 for “Hottest of” comparisons.

| Value | Description |
|-------|---------------------------------|
| 1 | External Diode 4 is enabled |
| 0 | External Diode 4 is not enabled |

Bit 3 – E3ENB Enables External Diode 3 for “Hottest of” comparisons.

| Value | Description |
|-------|---------------------------------|
| 1 | External Diode 3 is enabled |
| 0 | External Diode 3 is not enabled |

Bit 2 – E2ENB Enables External Diode 2 for “Hottest of” comparisons.

| Value | Description |
|-------|---------------------------------|
| 1 | External Diode 2 is enabled |
| 0 | External Diode 2 is not enabled |

Bit 1 – E1ENB Enables External Diode 1 for “Hottest of” comparisons.

| Value | Description |
|-------|---------------------------------|
| 1 | External Diode 1 is enabled |
| 0 | External Diode 1 is not enabled |

Bit 0 – IENB Enables internal diode for “Hottest of” comparisons.

| Value | Description |
|-------|-------------------------------|
| 1 | Internal diode is enabled |
| 0 | Internal diode is not enabled |

8.11.46. Product ID Register (Address FDh)

Name: PRODUCT ID
Offset: 0xFD

| | | | | | | | | |
|--------|-----------------|----|----|----|----|----|----|----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | PRODUCT_ID[7:0] | | | | | | | |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | | | | | | | | |

Bits 7:0 – PRODUCT_ID[7:0] Unique Product ID.

| Value | Description |
|-------------|-------------|
| EMC1822-1/2 | 0x89 |
| EMC1823-1/2 | 0x8F |
| EMC1824-1/2 | 0x8C |
| EMC1825-1/2 | 0x8D |
| EMC1843-1/2 | 0x8B |

8.11.47. Manufacturer ID Register (Address FEh)

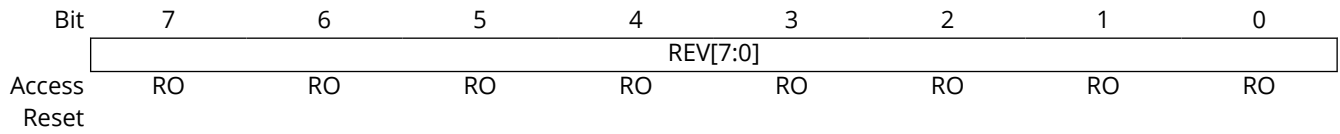
Name: MANUFACTURER ID
Offset: 0xFE

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------|----|----|----|----|----|----|----|
| | MCHP_ID[7:0] | | | | | | | |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |

Bits 7:0 – MCHP_ID[7:0] Unique manufacturer ID for Microchip.

8.11.48. Revision – Revision Register (Address FFh)

Name: REVISION
Offset: 0xFF

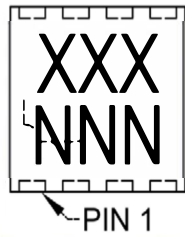


Bits 7:0 – REV[7:0] Die revision number.

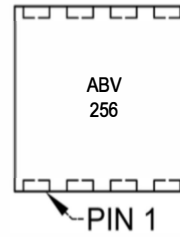
9. Packaging Information

9.1. Package Marking Information

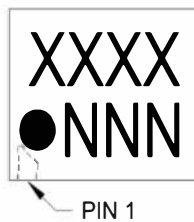
8-Lead WDFN (2 x 2 mm)



| Product Number | Code |
|----------------|------|
| EMC1822T-1E/RW | ABV |
| EMC1822T-2E/RW | ABW |
| EMC1843T-1E/RW | ACB |
| EMC1843T-2E/RW | ACC |

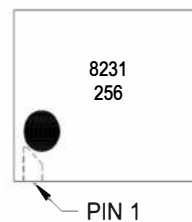


10-Lead VDFN (2.5 x 2.0 mm)



| Product Number | Code |
|----------------|------|
| EMC1823T-1E/9R | 8231 |
| EMC1823T-2E/9R | 8232 |
| EMC1824T-1E/9R | 8241 |
| EMC1824T-2E/9R | 8242 |
| EMC1825T-1E/9R | 8251 |
| EMC1825T-2E/9R | 8252 |

Example



Legend:

- XX...X Customer-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WW Week code (week of January 1 is week '01')
- NNN Alphanumeric traceability code
- Ⓔ³ JEDEC® designator for Matte Tin (Sn)

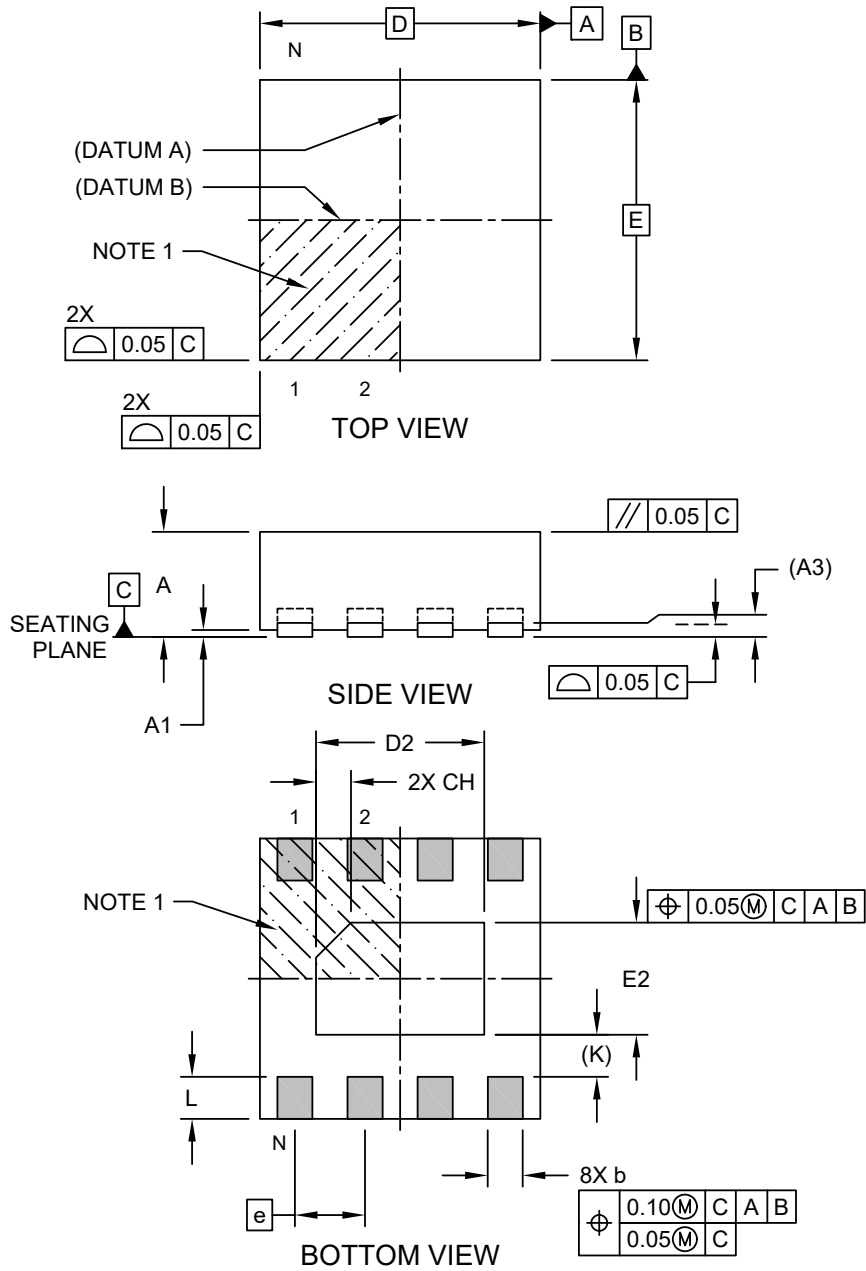
*

This package is RoHS compliant. The JEDEC designator (Ⓔ³) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

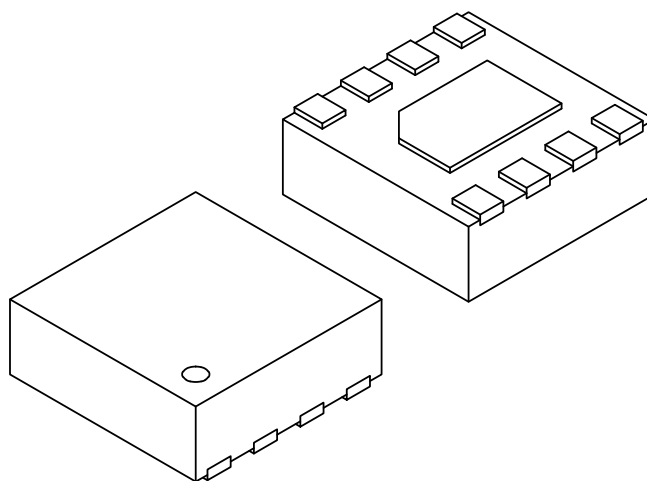
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-261C Sheet 1 of 2

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | MILLIMETERS | | |
|-------------------------|----|-------------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | 8 | | |
| Pitch | e | 0.50 BSC | | |
| Overall Height | A | 0.70 | 0.75 | 0.80 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | 0.10 REF | | |
| Overall Width | E | 2.00 BSC | | |
| Exposed Pad Width | E2 | 0.70 | 0.80 | 0.90 |
| Overall Length | D | 2.00 BSC | | |
| Exposed Pad Length | D2 | 1.10 | 1.20 | 1.30 |
| Exposed Pad Chamfer | CH | - | 0.25 | - |
| Terminal Width | b | 0.20 | 0.25 | 0.30 |
| Terminal Length | L | 0.25 | 0.30 | 0.35 |
| Terminal-to-Exposed-Pad | K | 0.30 REF | | |

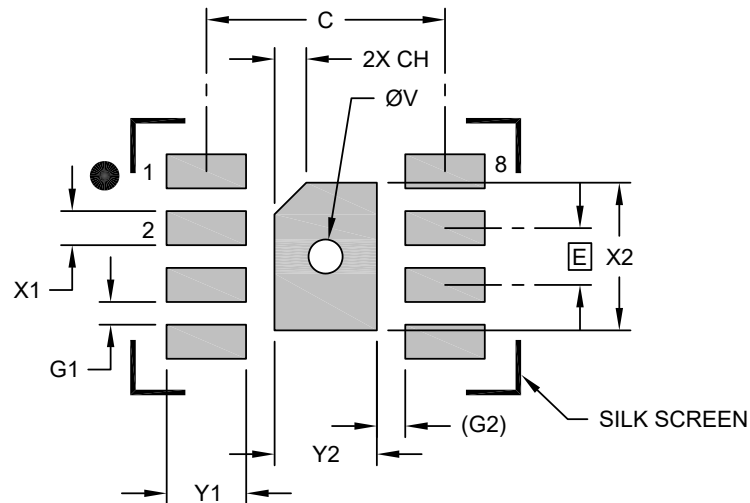
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-261C Sheet 2 of 2

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | | MILLIMETERS | | |
|---------------------------------|----|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Optional Center Pad Width | Y2 | | | 0.90 |
| Optional Center Pad Length | X2 | | | 1.30 |
| Contact Pad Spacing | C | 2.10 | | |
| Center Pad Chamfer | CH | 0.28 | | |
| Contact Pad Width (X8) | X1 | | | 0.30 |
| Contact Pad Length (X8) | Y1 | | | 0.70 |
| Contact Pad to Contact Pad (X6) | G1 | 0.20 | | |
| Contact Pad to Center Pad (X8) | G2 | 0.25 REF | | |
| Thermal Via Diameter | V | | 0.30 | |

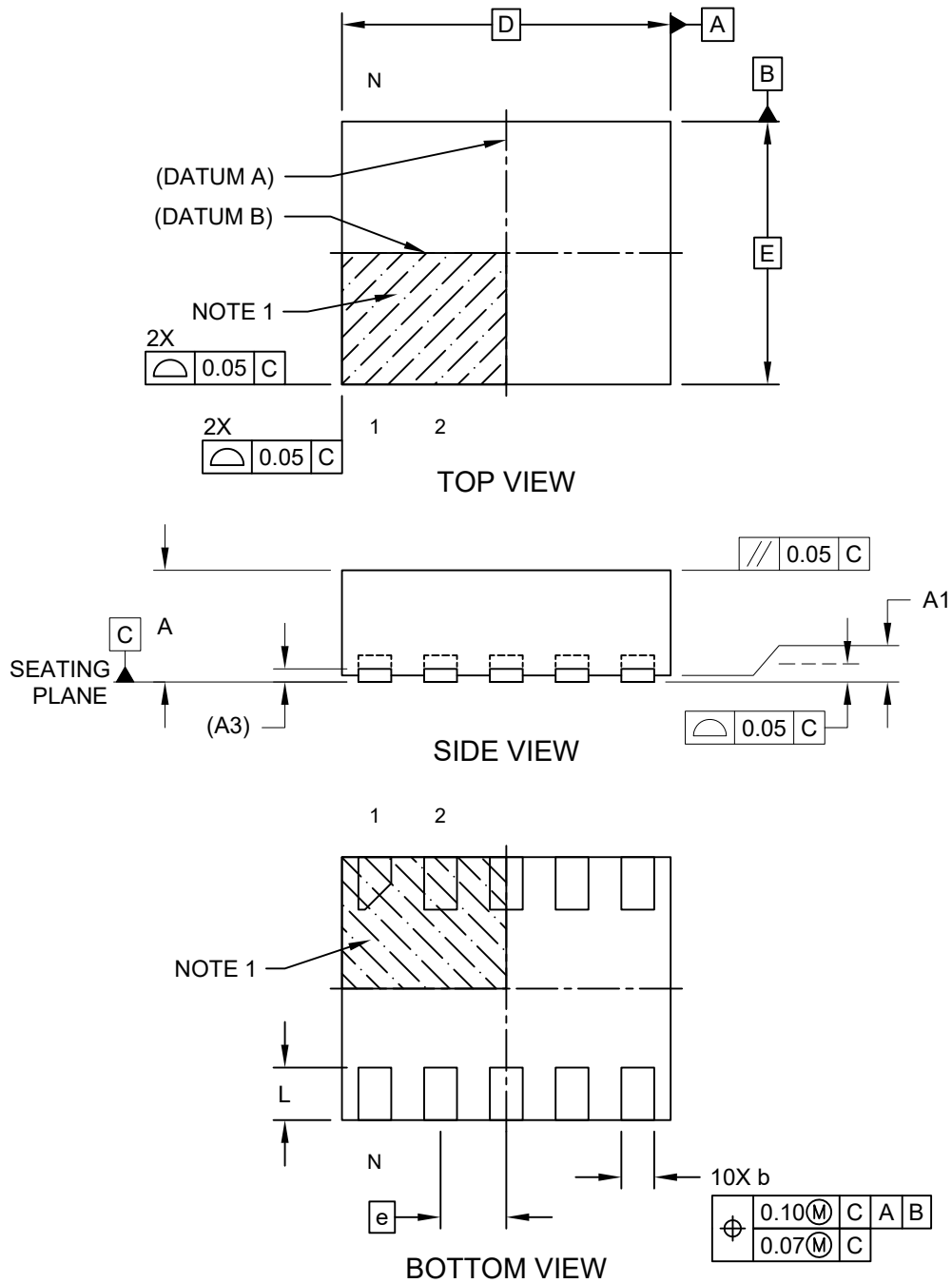
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2261C

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9R) - 2.5x2.0 mm Body [VDFN]

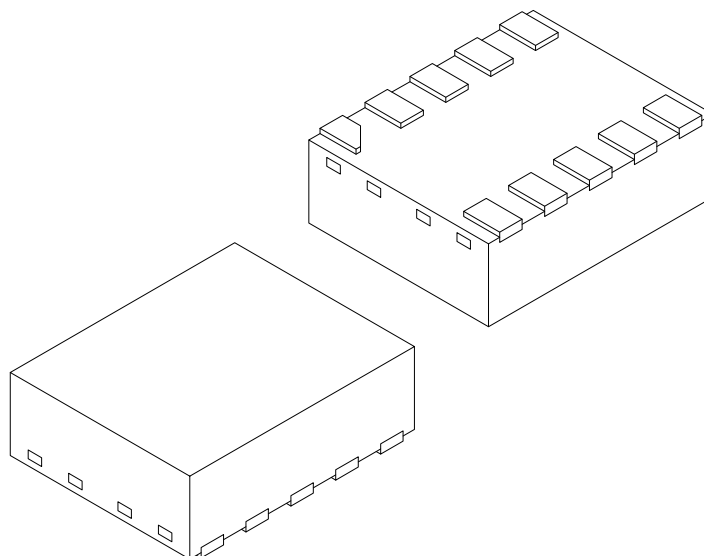
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-332B Sheet 1 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9R) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 10 | | |
| Pitch | e | 0.50 BSC | | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | (A3) | 0.10 REF | | |
| Overall Length | D | 2.50 BSC | | |
| Overall Width | E | 2.00 BSC | | |
| Terminal Width | b | 0.20 | 0.25 | 0.30 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

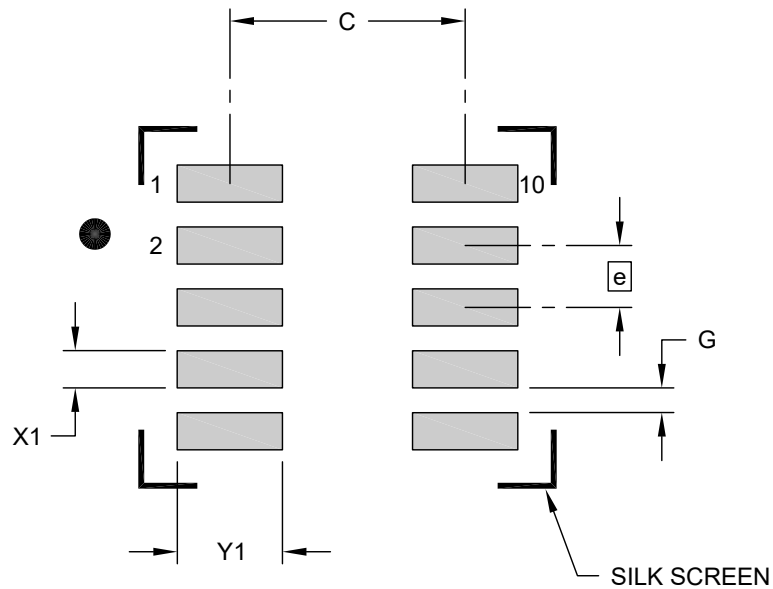
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-332B Sheet 2 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9R) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|---------------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Contact Pad Spacing | C | | 1.90 | |
| Contact Pad Width (X10) | X1 | | | 0.30 |
| Contact Pad Length (X10) | Y1 | | | 0.85 |
| Contact Pad to Center Pad (X10) | G1 | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2332A

10. Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. **[X]⁽¹⁾** **-X** **X** **/XX**
 Device Tape SMBUS Temp. Package
 and Reel Address Range
 Range

| | | |
|-----------------------|---|--|
| Device: | EMC1822: High-Accuracy, Low-Cost, Two-Wire Temperature Sensor EMC1823: High-Accuracy, Low-Cost, Two-Wire Temperature Sensor EMC1824: High-Accuracy, Low-Cost, Two-Wire Temperature Sensor EMC1825: High-Accuracy, Low-Cost, Two-Wire Temperature Sensor EMC1843: High-Accuracy, Low-Cost, Two-Wire Temperature Sensor | |
| Tape and Reel Option: | T | = Tape and Reel |
| SMBus Address: | 1 | = 1001_100(r/w) |
| | 2 | = 1000_101(r/w) |
| Temperature Range: | E | = -40°C to +125°C (Extended) |
| Package: | RW | = 8-Lead Very, Very Thin Plastic Dual Flat, No Lead - 2 x 2 mm Body (WDFN) |
| | 9R | = 10-Lead Very Thin Plastic Dual Flat, No Lead - 2.5 x 2.0 mm Body (VDFN) |

Examples:

- EMC1822T-1E/RW:Tape and Reel, 1001_100(r/w), Extended Temperature, 8L-WDFN package
- EMC1843T-2E/RW:Tape and Reel 1000_101(r/w), Extended Temperature, 8L-WDFN package
- EMC1823T-1E/9R:Tape and Reel, 1001_100(r/w), Extended Temperature, 10L-VDFN package
- EMC1824T-1E/9R:Tape and Reel, 1001_100(r/w), Extended Temperature, 10L-VDFN package
- EMC1825T-2E/9R:Tape and Reel, 1000_101(r/w), Extended Temperature, 10L-VDFN package

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

11. Revision History

Revision C (May 2025)

The following is the list of modifications:

- Updated [Table 7-2](#).
- Updated [Figure 8-1](#).
- Updated Section [Package Marking Information](#).

Revision B (July 2020)

The following is the list of modifications:

- Corrected Section [PRODUCT ID](#).
- Corrected Section [Package Marking Information](#).

Revision A (November 2018)

Original release of the document.

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