KSZ8441HLI and KSZ8441FHLI Errata

Device Revision: Production
Document Revision: 0.3

1	Writing to PMCTRL Register Power Management Bits Requires Change to Host Interface Write Timing

Description:
The Write Sample Time bit in the RX Frame Data Pointer Register (0x186 – 0x187) bit [12] determines when write data is sampled on the host interface. When this bit is 1 (default), the sample time is earlier, and writes to the Power Management Mode bits in PMCTRL (0x032 – 0x033) bits [1:0] may not occur properly. For example, it may be impossible to put the device into Global Soft Power Down mode.

Workaround:
Clear the Write Sample Time bit in the RX Frame Data Pointer Register (0x186 – 0x187) bit [12]. This causes the write sample time to occur later, and eliminates the problem described above.

This bit is cleared by the driver.

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2	Transmit Memory Available Value may Read Incorrect

Description:
The TXQ Memory Information Register (TXMIR) (0x178 – 0x179) is a read-only register that indicates the amount of unused memory space in the transmit queue. Sometimes this register returns an incorrect value of zero. Reading it again will return a correct value.

Workaround:
The software workaround is to read the register a second time whenever a zero value is read.

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3	Received PAUSE Frames

Description:
The KSZ8441 not respond to received PAUSE control frames, meaning that it will not suspend transmission of data frames on that port when requested to do so by its link partner sending PAUSE frames. PAUSE frames are received and are counted in the MIB RxPausePkts counter (offset 0xA), but they are not acted upon.

This issue does not affect the generation (transmission) of PAUSE frames in response to congestion within the KSZ8441.

Workaround:
There is no direct workaround for this issue.

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4	Disabling Auto-Negotiation

Description:

Unusual link behavior may occur if the Auto-Negotiation Enable bit (in the P1MBCR or P1CR4 register) is cleared (to disable AN) while link is already established and Energy Efficient Ethernet (EEE) is enabled. Note that by default, EEE is enabled.

The problem does not occur if link is down when AN Enable is cleared, or if link is to a non-EEE device.

Workaround:

To disable auto-negotiation, follow these steps:

1. Disable EEE by clearing the Next Page Enable bit in the PCSEEEC Register (0x0F3).
2. Set the Restart Auto-Negotiation bit(s) in the P1MBCR or P1CR4 registers (0x04C, 0x07E) for the desired port(s).
3. The Auto-Negotiation Enable bit(s) may now be cleared.

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