

Clock System Configuration and Usage on SAM C2x (Cortex M0+) Devices

TB3227



Introduction

The SAM C2x family of microcontrollers (MCUs) contains a sophisticated clock distribution system designed to give maximum flexibility to the user application. The clock system allows the tuning of the performance and power consumption of the device in a dynamic manner. This achieves the best trade-off between the two for an application.

The following figure illustrates the clock management diagram for the SAMC21N MCU.

Figure 1. SAMC21N Clock Distribution

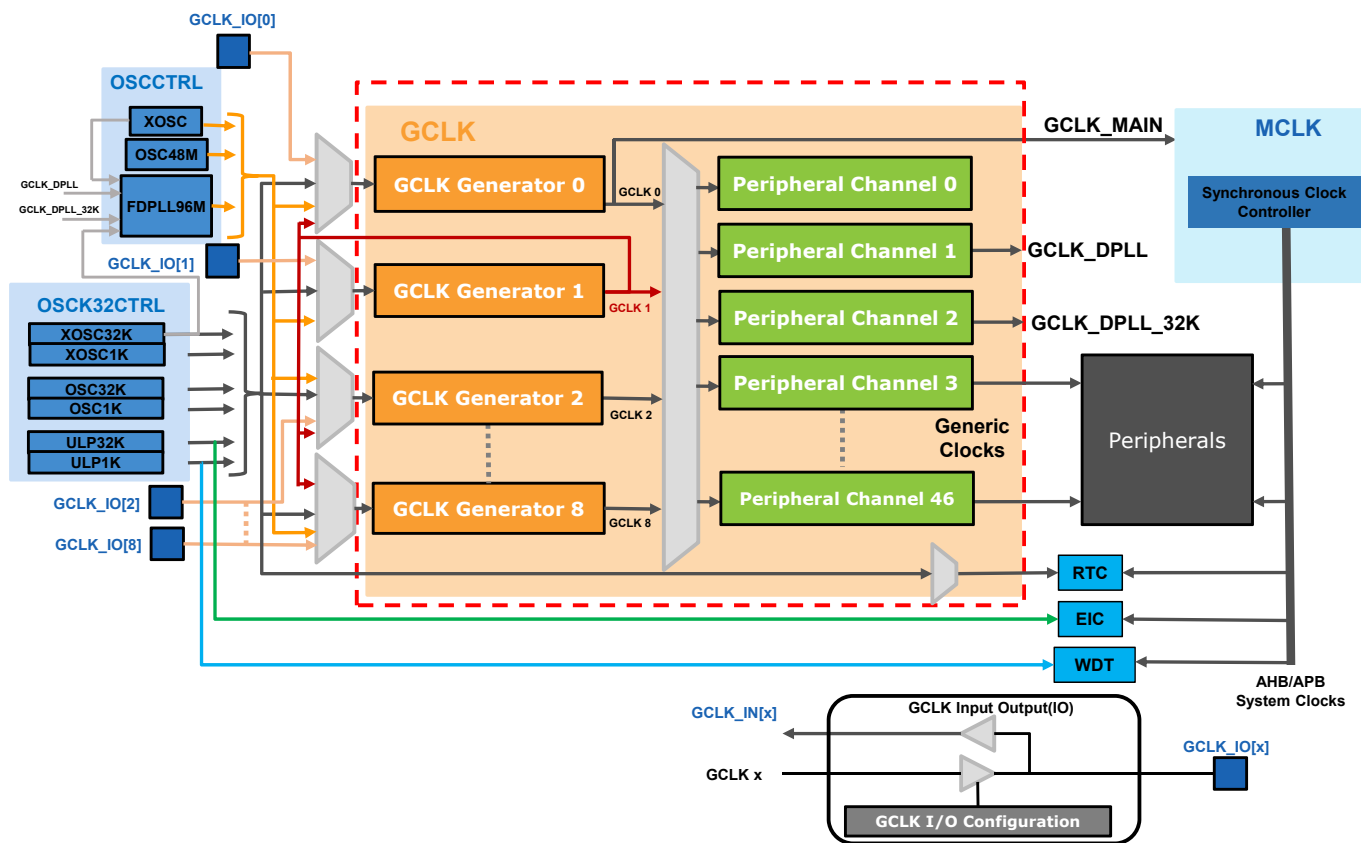


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1. Description

The clock system of the SAMC21N MCU consists of the following blocks:

Clock Sources

The SAMC21N MCU has several clock sources. The supported clock source modules are as follows:

OSCTRL: High-frequency clock sources.

- XOSC – 0.4 MHz to 32 MHz External Oscillator
- OSC48M – 48 MHz Internal Oscillator
- FDPLL96M – 48 MHz to 96 MHz Fractional Digital Phase-Locked Loop Oscillator

OSCK32CTRL: Low-frequency clock sources.

- XOSC32K – 32 kHz External Crystal Oscillator, provides both 32 kHz and 1 kHz output
- OSC32K – 32 kHz Internal Oscillator, provides both 32 kHz and 1 kHz output
- OSCULP32K – 32 kHz Internal Ultra-Low Power Oscillator, provides both 32 kHz and 1 kHz output

Generic Clock Controller (GCLK)

The GCLK provides Generic Clocks to various peripheral clock domains. The GCLK consists of nine GCLK Generators and 46 Peripheral channels. The Generic Clock Controller Input/Output (GCLK_IO) blocks act as a clock source to the GCLK generators.

Note: GCLK_IO[x] – Generic Input/Output External Clock Signal.

GCLK1 is the output of the GCLK generator 1, and is one of the clock sources for all the GCLK generators except the GCLK generator 1. GCLK Generators consist of a programmable prescaler. The programmable prescaler scales down the input frequency (from one of the Clock Sources discussed above) to a slower rate for use in a peripheral.

The peripheral channels multiplex and gate various generator outputs to one or more peripherals within the device. This setup allows a single common generator to feed one or more peripheral channels, which can then be enabled or disabled individually as required.

Main Clock Controller (MCLK)

The MCLK, also known as the Synchronous Clock Controller, provides the synchronous clocks (CPU, bus (AHB, APB) clocks) to the system. The main clock GCLK_MAIN to the MCLK is fed from the GCLK Generator 0 through Peripheral Channel 0. The MCLK contains clock masks that can turn on or off the user interface of peripheral clocks and bus clocks, and contain prescalers to derive low-frequency CPU clocks.

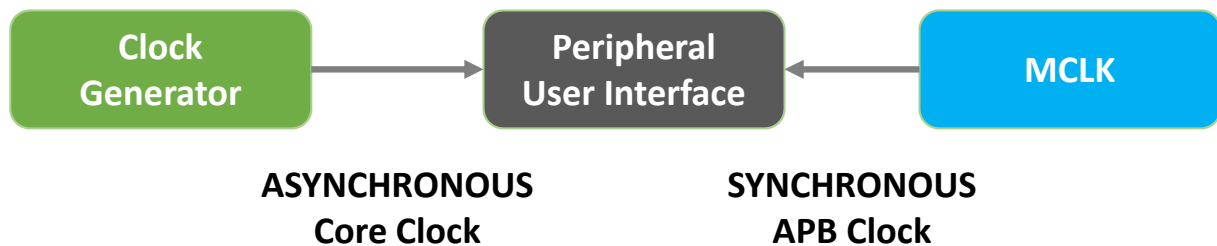
2. Clock Synchronization

The peripherals on the SAM C21N MCU consists of the following two clock domain interfaces:

- Synchronous interface: It is connected to the AHB/APB bus running from the synchronous clock in the Main Clock (MCLK) domain. The CPU accesses the peripheral registers through the synchronous interface.
- Asynchronous interface: It is connected to the core peripheral running from the asynchronous peripheral Generic Clock (GCLK) domain. The core peripheral runs at the asynchronous peripheral generic clock.

Communication between these clock domains must be synchronized. This mechanism is implemented in the hardware through the SYNCBUSY peripheral status register. The synchronization process takes place even if the peripheral generic clock is running from the same clock source and on the same frequency as the bus interface.

Figure 2-1. Clock Synchronization



3. Power and Performance Considerations

In an application, the system and peripheral clock frequencies are configured based on the power and performance requirements of the application. The power consumption of a device is directly proportional to the frequency of operation. A device running at high speed consumes more power versus a device running at low speed.

For the SAM C21n MCU, refer to the chapter “Electrical Characteristics” of the device data sheet for power and performance values.

Each GCLK generator operates independently, enabling the GCLK generators to drive different clock frequencies for different peripherals, and to drive different clock frequencies for different instances of the same peripheral. This capability of GCLK generators enables power saving, hence only the necessary clocks are generated. In Power-Saving mode of the MCU, when a peripheral is not utilizing the peripheral clock, the GCLK generator will not source from the oscillator until the peripheral requests the clock.

As noted above, the peripherals on the SAM C2x devices run on the asynchronous clock domain. These asynchronous peripheral clocks are synchronized to the system clocks (CPU, AHB/APB) when the CPU accesses the peripheral registers. The synchronization time is an important factor in the overall response time of the system.

For example, running a peripheral with a low speed has lower active power consumption. However, at the same time, the synchronization to the synchronous clock domain is dependent on the peripheral clock speed. The slower peripheral clock can give a lower response time, and more time waiting for the synchronization to complete.

4. Configuring Clocks with MPLAB Harmony v3

MPLAB[®] Harmony is a modular framework that provides interoperable firmware libraries for application development on 32-bit microcontrollers and microprocessors. It includes an easy to use Graphical User Interface (MPLAB Code Configurator) for selecting, configuring, and generating starter codes, peripheral libraries and middlewares (USB, TCP/IP, graphics and so on). The MCC provides an easy to use UI window, and a Clock Easy View window to configure the system and peripheral clocks.

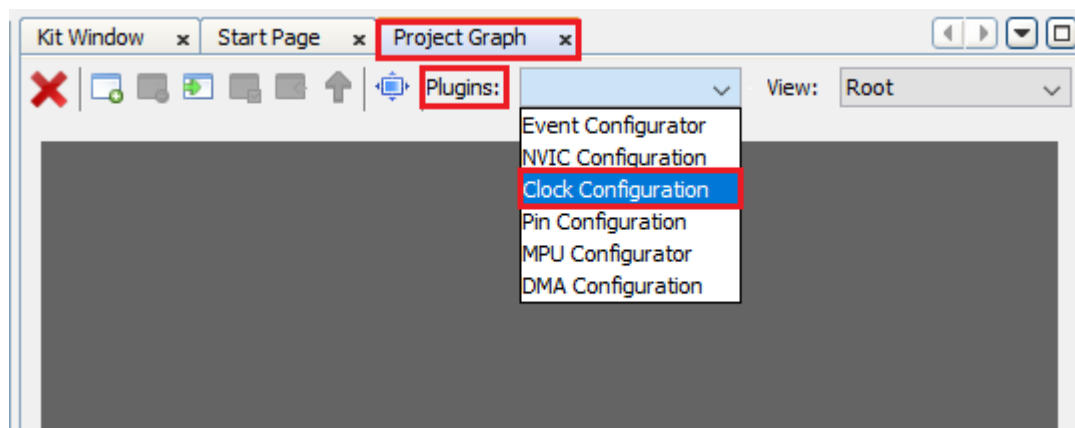
For additional information on MPLAB Harmony v3, refer to: www.microchip.com/en-us/tools-resources/configure/mplab-harmony.

4.1 Use Case Scenarios

The following use case scenarios demonstrate how to use MCC Clock Configuration window to configure the clocks.

1. To launch Clock Easy View in MPLAB X IDE, click on the **Project Graph** tab.
2. From the Plugins drop-down item list, select **Clock Configuration**.

Figure 4-1. Selecting Clock Configuration



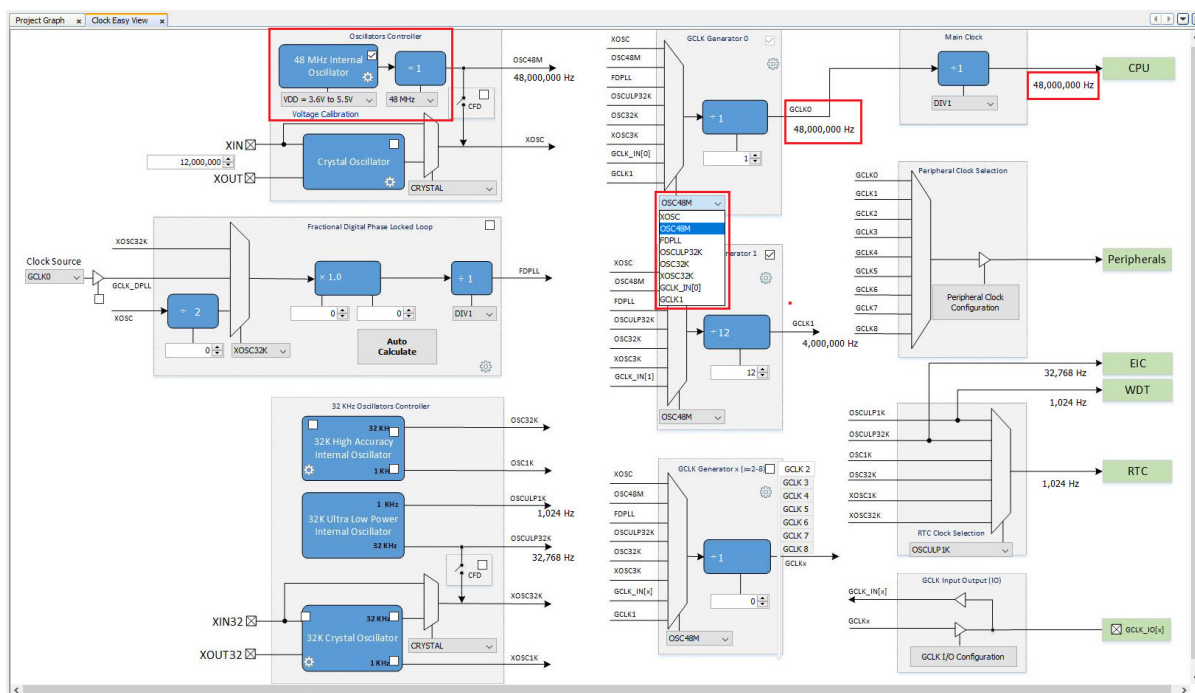
3. Click on the **Clock Easy View** tab. The Clock Easy View will be displayed within the MCC window.

Use Case Scenario 1

Configure the device to run at the maximum possible speed. Measure the frequency of the configured clock by routing the prescaled clock signal to a GPIO pin.

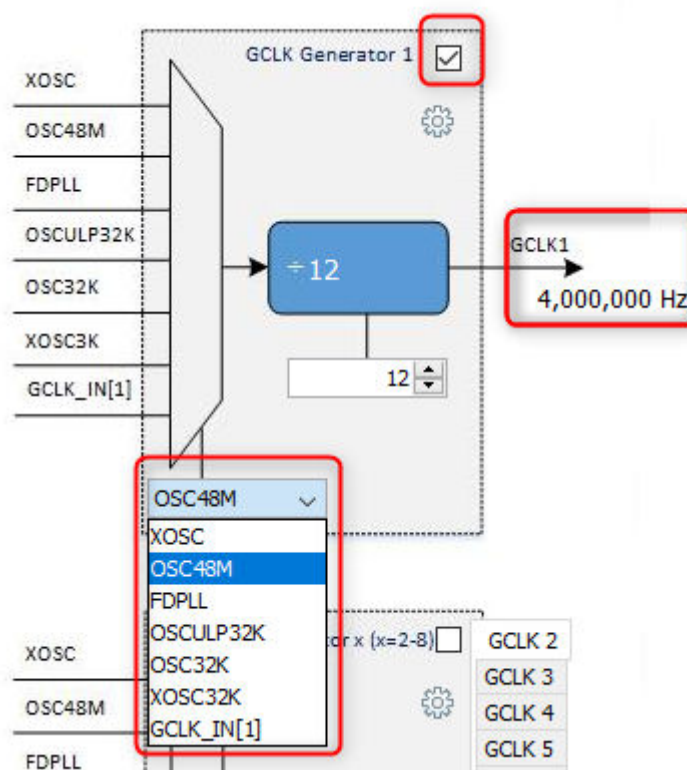
1. SAMC21N operates at 48 MHz maximum frequency. The OSC48M oscillator is configured and enabled to run the main clock at maximum frequency. The configured oscillator (OSC48M) is fed as input to the GCLK generator '0', and a suitable clock divider and masker must be selected to achieve a maximum frequency of 48 MHz. Refer to the following figure to configure the main clock.

Figure 4-2. SAMC21N Clock Easy View and Main Clock Configuration

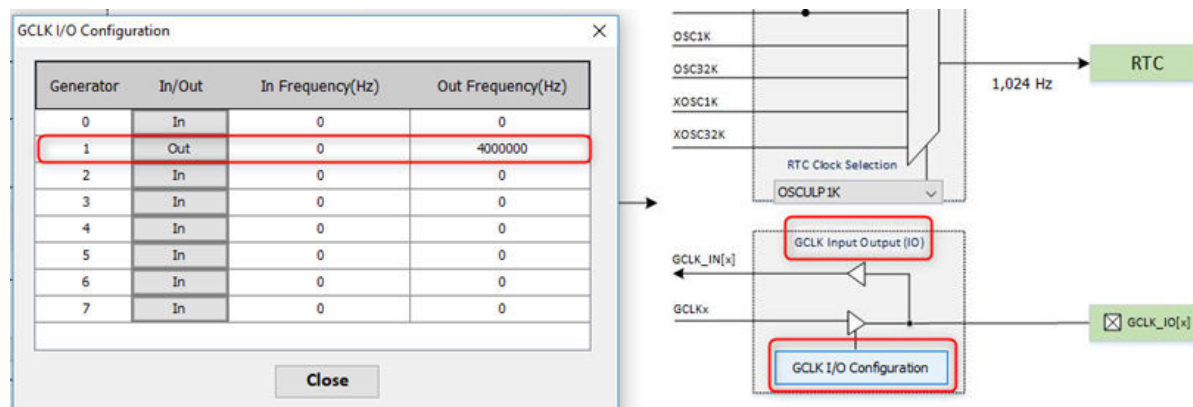


Tip: Double-click on the **Clock Easy View** tab to maximize the window.

2. Enable the GCLK generator 1 and select the oscillator OSC48M as the generator input. The divider value of a generator will be used to derive the low-frequency clocks from the GCLK generator sourced clocks. Configure the divider value as 12 to achieve a 4 MHz clock frequency at the GCLK generator 1 output. Refer to the following figure to configure GCLK IO1. Refer to the data sheet for maximum clock frequency an I/O pin can operate at.

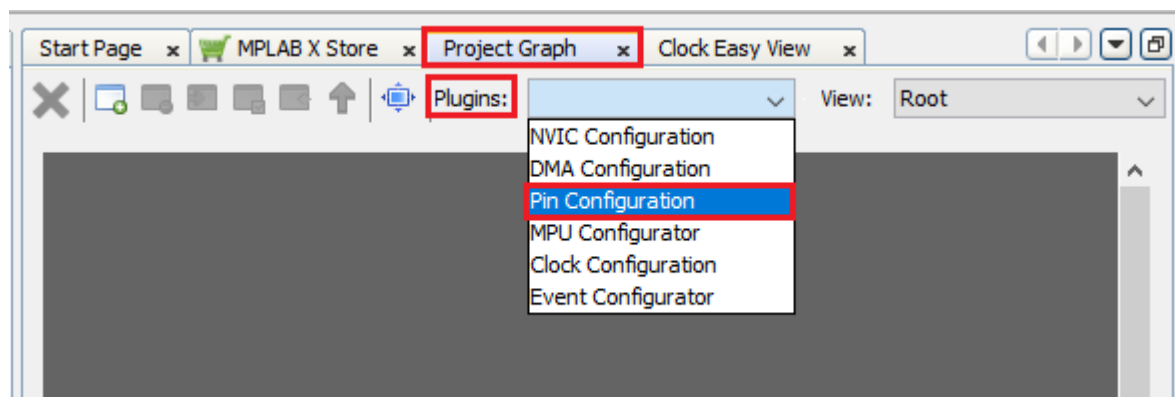
Figure 4-3. GCLK Generator 1 Configuration

- The output of the GCLK Generator 1 is used to measure the frequency and accuracy of the main clock. Click on the **GCLK I/O Configuration** to check the configured GCLK I/O [1] clock frequency as shown below.

Figure 4-4. GCLK I/O [1] Configuration

- Configure the pin which maps to GCLK1 on the device. To configure clock signal GCLK1 to a pin, in MPLAB X IDE click **Project Graph** and from the Plugins drop-down item list, select **Pin Configuration**.

Figure 4-5. Pin Configuration

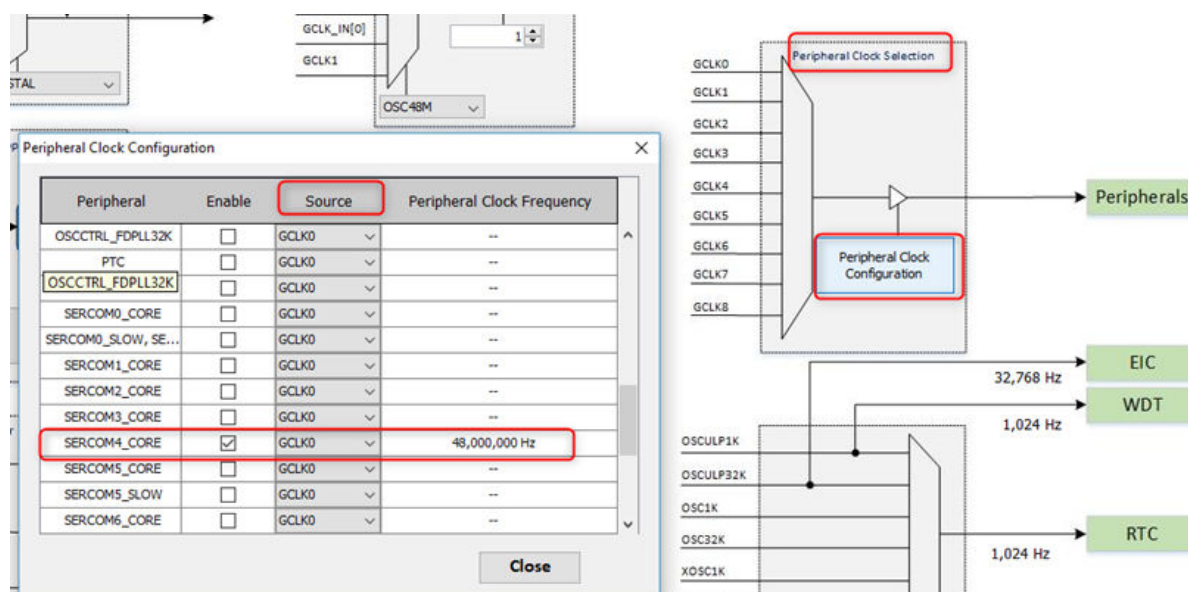


Use Case Scenario 2

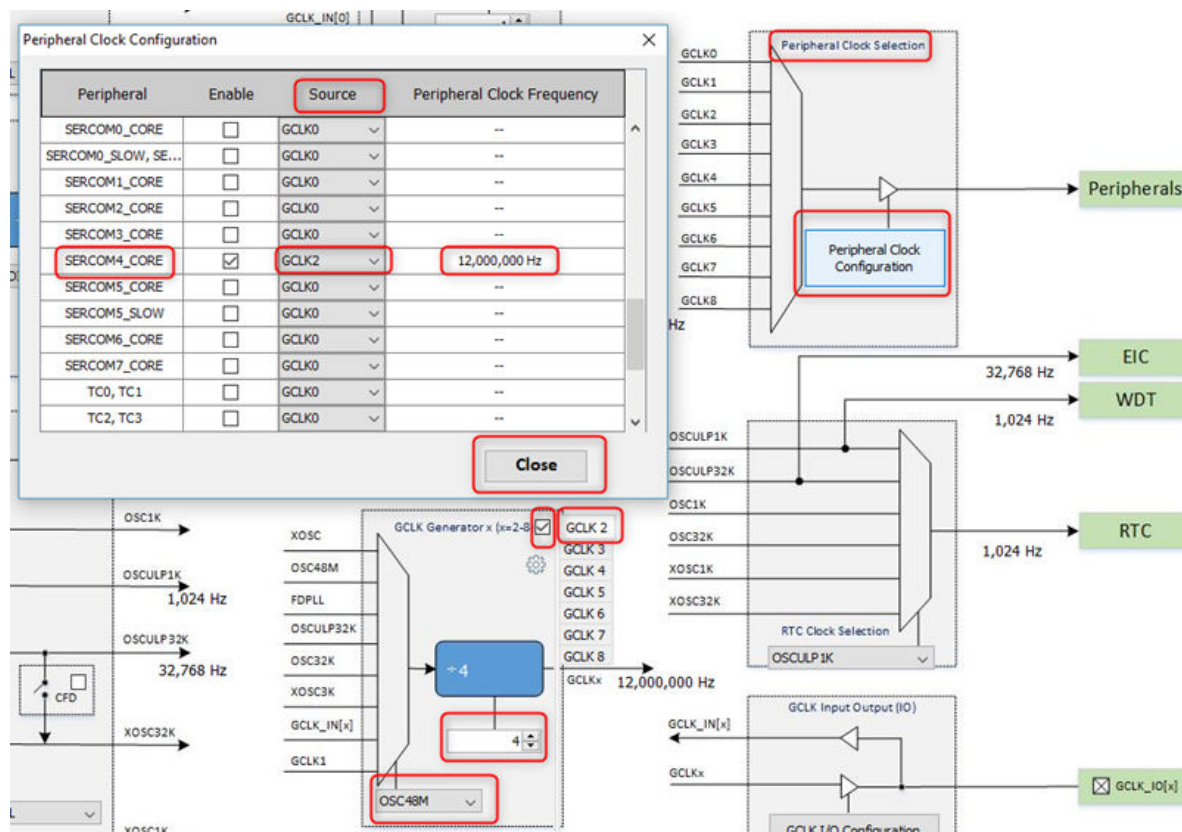
To configure the SERCOM Peripheral Clock to run the SERCOM (as USART) peripheral, follow these steps:

1. Configure the main clock, as shown in "Step 1" of the 4.1. Use Case Scenario 1.
2. By default, MCC automatically enables the peripheral clock when a peripheral is added to the Project Graph. Click on the **Peripheral Clock Configuration** button to check the specific peripheral (SERCOM) clock. The SERCOM4 clock source is selected as GCLK0, which is set to 48 MHz, see figure below.

Figure 4-6. SERCOM Peripheral Default Clock Configuration



3. The Peripheral Clock Configuration window can be used to configure the peripheral to run at a frequency different from the default frequency of 48 MHz. A different clock source can be selected. Refer to the following figure to configure the SERCOM4 peripheral clock with a 12 MHz frequency by using the GCLK2 as the source.

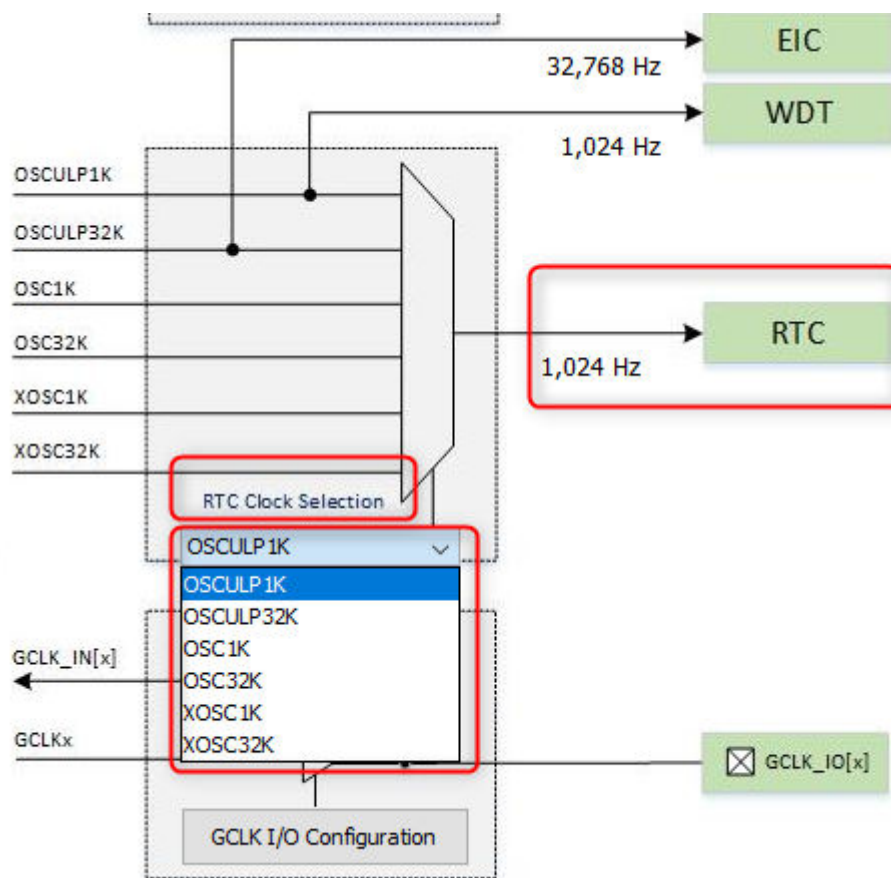
Figure 4-7. SERCOM Peripheral Clock Configuration with 12 MHz Clock Source

4. Configure the SERCOM (as USART) pins on the device. To configure the SERCOM pins, use the Pin Configuration option in the Project Graph.
5. To launch the Pin Configuration in MPLAB X IDE, click **Project Graph**, and from the Plugins drop-down item list, select **Pin Configuration**.

Use Case Scenario 3

Follow these steps to configure the RTC peripheral clock in Harmony v3 to run the RTC peripheral at low power.

1. Configure the main clock, as shown in "Step 1" of the [4.1. Use Case Scenario 1](#).
2. On SAMC21N, some of the peripherals, such as the RTC, WDT, and EIC will run directly with the 32 kHz oscillator controller outputs (OSC32K, OSC1K, OSCULP32K, OSCULP1K⁽³⁾, XOSC32K, XOSC1K).
3. From the drop-down list, select the **OSCULP1K** oscillator as the RTC peripheral clock input to run the RTC at low power. The OSCULP1K oscillator will provide 1 KHz clock frequency as the oscillator output by running at low power. Refer to the following figure to configure the RTC peripheral clock.

Figure 4-8. RTC Peripheral Clock Configuration

4. The RTC peripheral can be used for different applications, for example, the RTC used as a calendar requires an accurate clock source. When the RTC is used as a calendar, it uses an external accurate clock source. The external clock sources (XOSC1K or XOSC32K) can be configured through MCC.

Notes:

1. Advanced clock configuration options, such as RUN in STANDBY, ONDEMAND clock, DPLL COARSE, FINE and so on can be configured in the Clock Tree View window (Refer to the MCC *Project graph > System > Clock*).
2. In these use case scenarios above, the MCC UI screen shots are captured using MPLAB Code Configurator version 5.3.7 and repository Chip Support Package (CSP) version 3.18.0.
3. OSCULP1K is an Oscillator name used in MPLAB Code Configurator for 1.024 kHz output from 32 kHz internal Oscillator.

5. Resources

- The Low-Power Training Module for SAMC21 Low-Power Application on SAMC2x (Arm® Cortex® M0+) MCUs Using MPLAB® Harmony v3 Peripheral Libraries: microchipdeveloper.com/xwiki/bin/view/software-tools/harmony/low-power-application-on-samc21/

For additional information on the clock system and low-power features, refer to the following documents:

- TB3183: What is Sleep Walking? How it Helps to Reduce Power Consumption: <http://ww1.microchip.com/downloads/en/DeviceDoc/90003183A.pdf>
- AT13486: SAM C System Clock Management (SYSTEM CLOCK) Driver: ww1.microchip.com/downloads/en/DeviceDoc/Atmel-42647-SAM-System-Clock-Management-SYSTEM-CLOCK-Driver_ApplicationNote_AT13486.pdf

For additional information about 32-bit Microcontroller Collaterals and Solutions, refer to:

- DS70005534: 32-bit Microcontroller Collateral and Solutions Reference Guide ww1.microchip.com/downloads/aemDocuments/documents/MCU32/ProductDocuments/ReferenceManuals/32-bit-Microcontroller-Collateral-and-Solutions-Reference-Guide-DS70005534.pdf

For other relevant information, refer to the Microchip web site.

- www.microchip.com/

6. Revision History

Revision B - January 2024

The following updates were incorporated for this revision:

Document	Minor changes of format. Changed <i>MPLAB Harmony Configurator</i> by <i>MPLAB Code Configurator</i> . Changed <i>MHC</i> by <i>MCC</i> .
4. Configuring Clocks with MPLAB Harmony v3	Updated some paragraphs in 4.1. Use Case Scenarios . Updated Figure 4-1 and Figure 4-2 . Added Figure 4-5 .
5. Resources	Added new references.

Revision A - August 2019

This is the initial released version of this document.

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ISBN: 978-1-6683-3848-3

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