TB3184

NAND Flash Interface with EBI on Cortex-M Based MCUs

Introduction

The External Bus Interface (EBI) is used to transfer data to and from the external memory. The EBI of the MCU transfers data between the internal AHB bus and the external memories.

The EBI is mapped to the external RAM region of the Cortex®-M core. The external RAM region (0x60000000–0x9FFFFFFF) of the Cortex-M7 memory system is intended for either on-chip or off-chip memory.

This document focuses on the interfacing of the NAND Flash with EBI using a Static Memory Controller (SMC). A part of the EBI which can handle several external memory and peripheral devices are as follows::

- SRAM
- PSRAM
- PROM
- EEPROM
- LCD Module
- NOR Flash
- NAND Flash

The SMC is accessed through the AHB bus matrix from the CPU core. The SMC can be connected to an external static memory, such as a NAND Flash through the multiplexed /IO pins.

Figure 1. NAND Interface with SMC
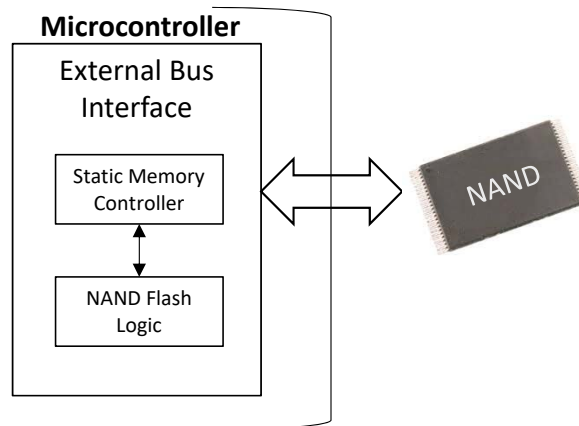
Applicable MCUs:

Microchip's Cortex-M7 and M4 based MCUs with EBI-SMC, that is, ATSAMV71, ATSAME70, ATSAM4E.

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1. Interfacing With SMC

The SMC supports NAND Flash devices with 8-bit and 16-bit data buses.

The SMC embeds the NAND Flash logic which handles all the commands, addresses and data sequences of the NAND low-level protocol. The SMC features dedicated address space for each NAND Flash Chip Select (NCSx) that is used for command, address and data transfer to and from the NAND Flash, minimizing CPU overhead. A maximum of 4 NAND Flash memories can be connected to the SMC using the NAND Chip Select signal.

The Address Latch Enable (ALE) and Command Latch Enable (CLE) signals on the NAND Flash device are driven by the address bits, A22 and A21, of the address bus.

The address space allocated for the command, address, and data going to and from the NAND Flash for each NAND chip select (NCSx) is listed in the following table. Whenever a command or an address byte is written to the respective address space, the NAND control signals, ALE or CLE, will be enabled.

Table 1-1. NAND Chip Select and Corresponding Address Space

NAND Chip Select (NCSx)	Address Space		Address for Transferring Data Bytes to the NAND Flash	Address for Transferring Address Bytes to the NAND Flash	Address for Transferring Command Bytes to the NAND Flash
NCS0	0x6000_0000	0x60FF_FFFF	0x6000_0000	0x6020_0000	0x6040_0000
NCS1	0x6100_0000	0x61FF_FFFF	0x6100_0000	0x6120_0000	0x6140_0000
NCS2	0x6200_0000	0x62FF_FFFF	0x6200_0000	0x6220_0000	0x6240_0000
NCS3	0x6300_0000	0x6FFF_FFFF	0x6300_0000	0x6320_0000	0x6340_0000

Writing the READ ID command (0x90) to the memory location 0x60400000 triggers the CLE and places the data 0x90 on the data bus D0-D7 for the 8-bit NAND Flash.

Similarly, writing the 0x00 column address to the memory location 0x60200000 triggers the ALE and places the data 0x00 on the data bus D0-D7 for the 8-bit NAND Flash.

Code Example:

```
/* Assign NCS0 specific memory address to the variables */
static uint32_t data_addr     = 0x60000000;
static uint32_t address_addr  = 0x60200000;
static uint32_t command_addr  = 0x60400000;


/* Send command to the NAND Flash. */
*((volatile uint8_t *)command_addr) = (uint8_t)command;

/* Send address to the NAND Flash. */
*((volatile uint8_t *)address_addr) = (uint8_t)address;

/* Write 8-bit data to the NAND Flash. */
*((volatile uint8_t *)data_addr) = (uint8_t)data;
```
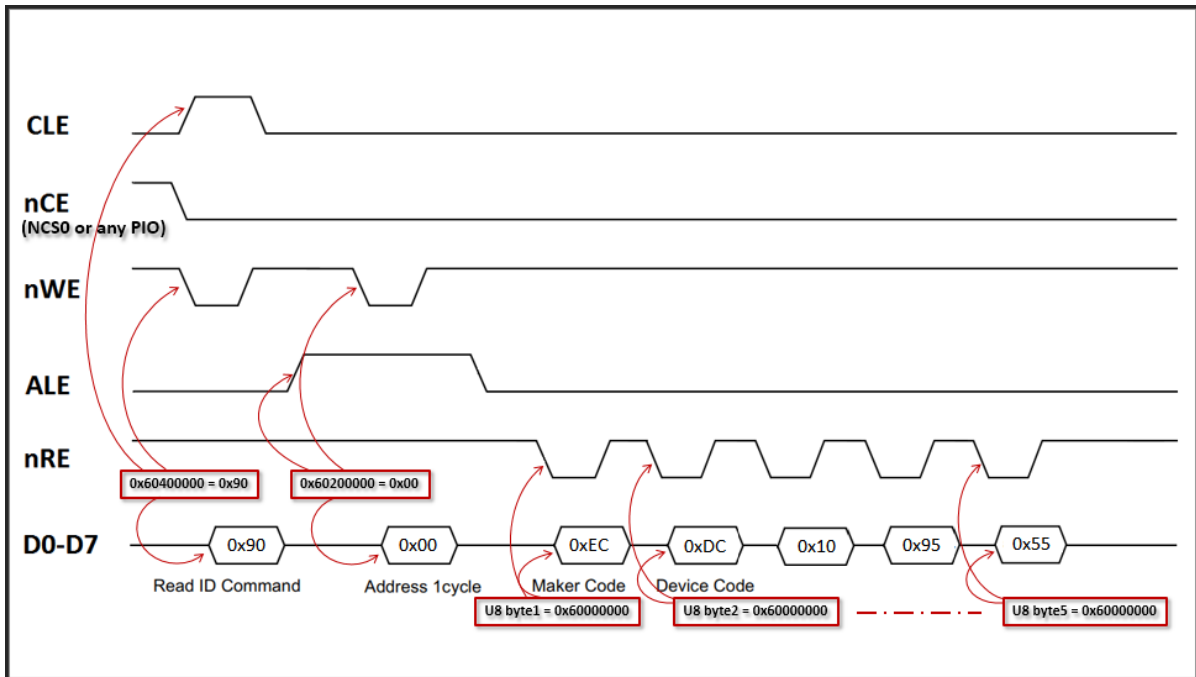
The following figure shows the Read ID command and the response from the NAND Flash memory part number K9F4G08U0E.

Figure 1-1. Read ID Command Operation

2.   Hardware Interface Initialization

The following hardware connections and register initialization steps are described for the ATSAMV71Q21 144-pin package.

Note: The initialization is shown for the reference purpose only, and for other MCUs, refer to the *Package and Pinout* chapter of the respective data sheet.

The I/O pin initialization for the 8-bit NAND is connected to the NCS0:

- To initialize the 8-bit D0-D7 data bus, configure the Port C, PC0 to PC7 in Peripheral-A mode
- To initialize the NANDOE, configure the Port C, PC9 in Peripheral-A mode
- To initialize the NANDWE, configure the Port C, PC10 in Peripheral-A mode
- To initialize the NANDCLE, configure the Port C, PC17 in Peripheral-A mode
- To initialize the NANDALE, configure the Port C, PC16 in Peripheral-A mode
- To initialize the R/nB, configure any PIO as an input pin with pull-up enabled
- To initialize the nCE, configure any PIO as an output pin (refer to Tips and Tricks for the supported nCE connection types)

Figure 2-1. MCU-8-Bit NAND Hardware Connection
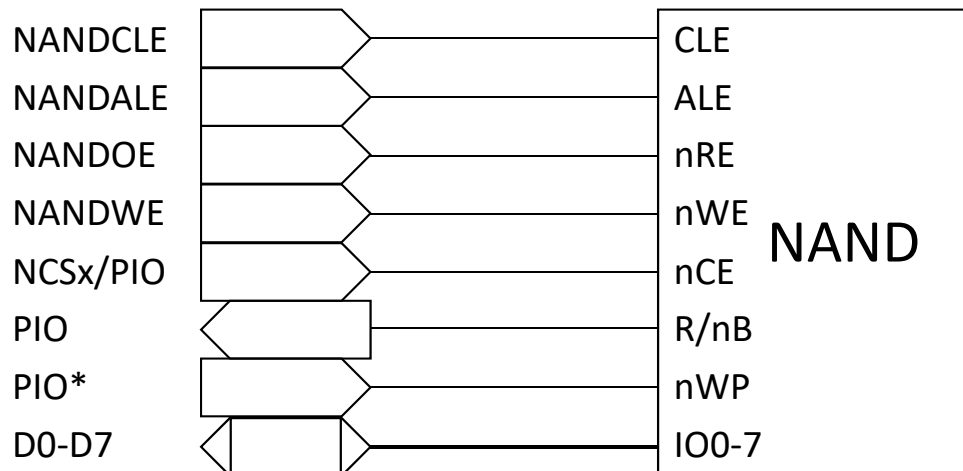
* For the application requiring the Write Protect feature, nWP shall be assigned to a PIO. Otherwise, nWP shall be pulled-up permanently.

Follow these register settings for the initialization:

- Enable the SMC peripheral clock.
- Enable the Port C clock.
- Depending on the nCE and R/nB pin selected, enable the corresponding port.
- Set the SMC_NFCS0 bit in the SMC NAND Flash Chip Select Configuration Register to assign the NCS0 to the connected NAND Flash.
- Set the SMC setup, pulse, and cycle timing based on the timing parameters recommended by the NAND Flash manufacturer. Refer to the AC Characteristics in the NAND Flash specification.
- Set the required bits in the SMC_MODE0 register, that is, set the READ_MODE, WRITE_MODE and DBW = 0

3.   Tips and Tricks

The MPU region setting for EBI

To ensure that the processor preserves the transaction order and correct NAND Flash behavior, and the NAND Flash address space must be declared in the Memory Protection Unit (MPU) as *Device* or *Strongly-ordered* memory.
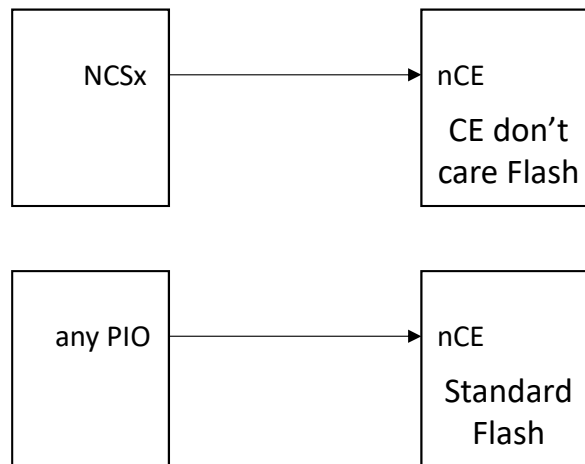
Error Correction Code (ECC)

The SMC does not support the hardware ECC. The software has to handle the generation and verification of ECC bytes for the spare area of the NAND Flash page. The Advanced Software Framework (ASF) from Microchip provides the software API for generating 3-byte hamming code for a data block with the size as a multiple of 256 bytes, that is, 22 bits per 256 bytes. The ECC verification API of the ASF is capable of detection and correction of a 1-bit error per 256 bytes and a multi-bit error detection per 256 bytes.

Chip Enable (nCE)

If the Chip Enable (nCE) signal of the NAND Flash is connected to a PIO line, then it remains asserted even when NCSx is not selected, preventing the NAND Flash from returning to Standby mode. The connection of nCE to either NCSx (x=0, 1, 2, 3) or any PIO depends on the NAND Flash specification. For example, if NAND Flash is of the *CE don't care* type, then the nCE signal must be connected to NCSx.

Figure 3-1. The nCE Connectivity Options

```
┌──────────┐              ┌──────────┐
│          │              │  nCE     │
│  NCSx    │─────────────▶│          │
│          │              │ CE don't │
│          │              │care Flash│
└──────────┘              └──────────┘

┌──────────┐              ┌──────────┐
│          │              │  nCE     │
│ any PIO  │─────────────▶│          │
│          │              │ Standard │
│          │              │  Flash   │
└──────────┘              └──────────┘
```

Ready/Busy (R/nB)

The ready/busy (R/nB) signal of the NAND Flash must be connected to a PIO input.

SMC Timing

The read and write timing cycles required to access the NAND Flash are built on the SMC core clock cycle, which can be enabled or disabled through the Power Management Controller (PMC). The SMC Core clock is derived from the Master Clock (MCK) and therefore, MCK = SMC Clock.

The read and write timings are defined separately for each Chip Select (NCSx) as an integer multiple of the Master Clock cycles.

- Read Timing:
  - The read from the Flash is either controlled by the NRD (also referred to as NANDOE or nRE) or the NCS (also referred to as NCSx. Where, x = 0,1,2,3). The SMC needs to know when the read data is available on the data bus. This is achieved through the READ_MODE bit in the SMC_MODE register.

Figure 3-2. Read Waveform
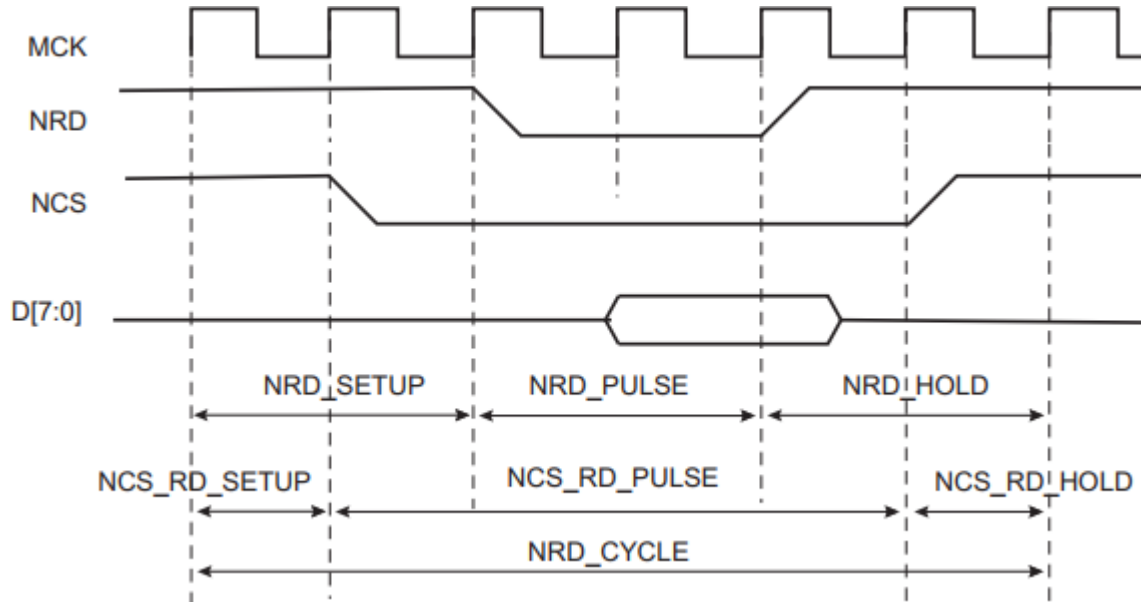
READ_MODE:

0: The read operation is controlled by the NCS signal.

1: The read operation is controlled by the NRD signal.

When `READ_MODE = 1`,

```
NRD_CYCLE = NRD_SETUP + NRD_PULSE + NRD_HOLD
```

When `READ_MODE = 0`,

```
NRD_CYCLE = NCS_RD_SETUP + NCS_RD_PULSE + NCS_RD_HOLD
```

The data from the NAND Flash is available during the falling edge of the nRE.

- Write Timing
  - Writing to the Flash is controlled by the NWE (also referred as NANDWE or nWE) or the NCS (also referred as NCSx. Where, x = 0,1,2,3). This is achieved through the WRITE_MODE bit in the SMC_MODE register.

Figure 3-3. Write Waveform
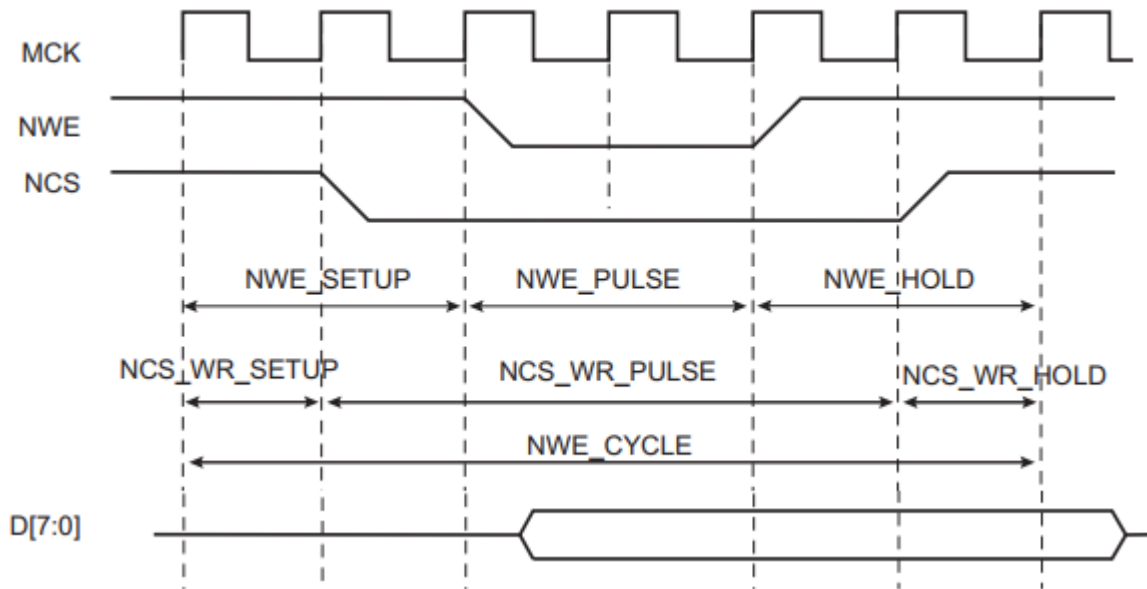
WRITE_MODE

0: The write operation is controlled by the NCS signal.

1: The write operation is controlled by the NWE signal.

When `WRITE_MODE = 1`,

```
NWE_CYCLE = NWE_SETUP + NWE_PULSE + NWE_HOLD
```

When `WRITE_MODE = 0`,

```
NWE_CYCLE = NCS_WR_SETUP + NCS_WR_PULSE + NCS_WR_HOLD
```

The data to the NAND Flash is latched during the rising edge of the nWE.

- Sample calculation of the SMC timing:
  As mentioned previously, the SMC timing parameters are highly dependent on the NAND Flash characteristics.

  The following example shows how to calculate the read-timing value.

  Given input parameters:

  MCK = 150 MHz

  `READ_MODE = 1`

  RE Pulse Width (tRP) = min. 12 ns (from NAND Flash AC characteristics specification)

A tRp of 12 ns can be achieved by selecting the proper value in the NRD_PULSE register.

NRD_PULSE should be >= 12 ns

SMC Clock period = 1/MCK = 1/150 MHz = 6.7 ns = approx. 7 ns

Therefore, NRD_PULSE = X * 7 ns >= 12 ns

X >= 2

Therefore, the value to be loaded in the NRD_PULSE register should be >=2

The value selection for the SMC timing register must be done with care. A bigger value might have impact over the performance, where a smaller value might have impact over the normal functionality. Therefore, an optimum value must be chosen.

Note: Programming either the read and write PULSE timing to zero is not permitted.

Note: The SMC NAND Flash Controller on the Cortex-M3 based MCU (i.e., ATSAM3U) is more advanced than what is available on the Cortex-M7 or Cortex-M4 based MCUs.
The following are some of the key features available on the ATSAM3U MCUS; however, these are not applicable on the ATSAM4E or the STSAMV71:

1. Various page size configurations, such as 512+16 bytes (main area + spare area), 1024+32 bytes, 2048+64 bytes and 4096+128 bytes.
2. Hardware ECC support for all page size configurations.
3. Dedicated NFC (NAND Flash controller) SRAM for data transfer.
4. Dedicated interrupt support for data transfer status.

For additional information, refer to the respective product data sheet which are available for download form the Microchip web site.

4. References

For additioanl information, refer to these documents:

- SAM V71 SMART ARM-Based Flash MCU Data Sheet:
  http://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-44003-32-bit-Cortex-M7-Microcontroller-SAM-V71Q-SAM-V71N-SAM-V71J_Datasheet.pdf
- SAM4E Series SMART ARM-Based Flash MCU Data Sheet:
  http://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-11157-32-bit-Cortex-M4-Microcontroller-SAM4E16-SAM4E8_Datasheet.pdf
- SAM3U Series SMART ARM-Based Flash MCU Data Sheet:
  http://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-6430-32-bit-Cortex-M3-Microcontroller-SAM3U4-SAM3U2-SAM3U1_Datasheet.pdf
- For ARM reference:
    - http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0646a/CHDBIJJE.html
    - http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0553a/CHDBIJJE.html

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