AN4320

BM78 and RN4678 Firmware Upgrade using Host Microcontroller Unit

Introduction

The BM78 and the RN4678 modules are fully certified, embedded 2.4 GHz Bluetooth® Low Energy wireless module with Basic Rate (BR) and Enhanced Data Rate (EDR) features. The BM78 and the RN4678 modules include an on-board Bluetooth stack, power management subsystem, 2.4 GHz transceiver and Radio Frequency (RF) power amplifier. The users can embed Bluetooth functionality into any application using the BM78 and the RN4678 modules.

This application note describes the procedures and data formats used to conduct the Device Firmware Upgrade (DFU) using the external host MCU.

Table of Contents

1. Quick References

1.1 Reference Documentation

For further details, refer to the following:

- *BM78 Evaluation Board (EVB) User's Guide* (DS70005246)
- *BM78 Bluetooth® Dual-Mode Module Data Sheet* (DS60001380)
- *RN4678 PICtail™/PICtail Plus Daughter Board User's Guide* (DS50002566).
- *RN4678 Bluetooth® Dual Mode Module Data Sheet* (DS50002519)

1.2 Hardware Requirements

- SAM G55 Xplained Pro Evaluation Kit (ATSAMG55-XPRO)
- BM78 PICTAIL Plus (BM-78-PICTAIL)
- BM78 Bluetooth Dual Mode Module (BM78)

1.3 Software Requirements

- Tera Term software tool. For more details on the software tools and firmware files, refer to the www.microchip.com/BM78 and www.microchip.com/RN4678.

1.4 Acronyms and Abbreviations

Table 1-1. Acronyms and Abbreviations

Acronyms and Abbreviations	Description
ACK	Acknowledgment
BR	Basic Rate
CSEQ	Command Sequence
DFU	Device Firmware Update
EDR	Enhanced Data Rate
MCU	Microcontroller Unit
NAK	Non Acknowledgment

2. Overview of the BM78 and the RN4678 Modules

The IS1678 chip in the BM78 module or the RN4678 module has a code memory (Flash) and a configuration memory (EEPROM). The code memory stores the firmware of the BM78 module or the RN4678 module. There are 5 banks composing the Flash, and the size of each bank is 64 Kbytes.

Note: In this application note, all the data is aligned in the big endian.

2.1 BM78 and RN4678 Flash Memory Programming

To perform any memory programming operation, the user needs to follow the process shown in the following figure with respect to the command protocols. The following are the steps to perform the Flash memory programming process:

1. Enter Flash Memory Programming Mode – Set the BM78 module or the RN4678 module into the write Flash mode using the pins P2_0/P2_4/EAN. Set the pins P2_0/P2_4/EAN to the ON state, and, then, initiate a hardware reset using the RST_N pin; see the following table for details. For more details, refer to the *BM78 Evaluation Board (EVB) User's Guide* (DS70005246) and the *RN4678 PICtail™/PICtail Plus Daughter Board User's Guide* (DS50002566).
2. Connect to the Flash – Use the CSEQ Get Flash ID command to get the Flash ID for verification to connect to the Flash in the BM78 module or the RN4678 module.
3. Use the following Flash operations commands to implement the DFU:
   - CSEQ Flash Erase command
   - CSEQ Bank Switch command
   - CSEQ Write Flash command
4. Disconnect from Flash – After the DFU, the host MCU sets the BM78 module or the RN4678 module into Application mode using the pins P2_0/P2_4/EAN. Set the pins P2_0/P2_4/EAN to the OFF state, and, then, initiate a hardware reset using the RST_N pin; see the following table. For more details, refer to the *BM78 Evaluation Board (EVB) User's Guide* (DS70005246) and the *RN4678 PICtail™/PICtail Plus Daughter Board User's Guide* (DS50002566).

Figure 2-1. Overview of Flash Memory Programming Process

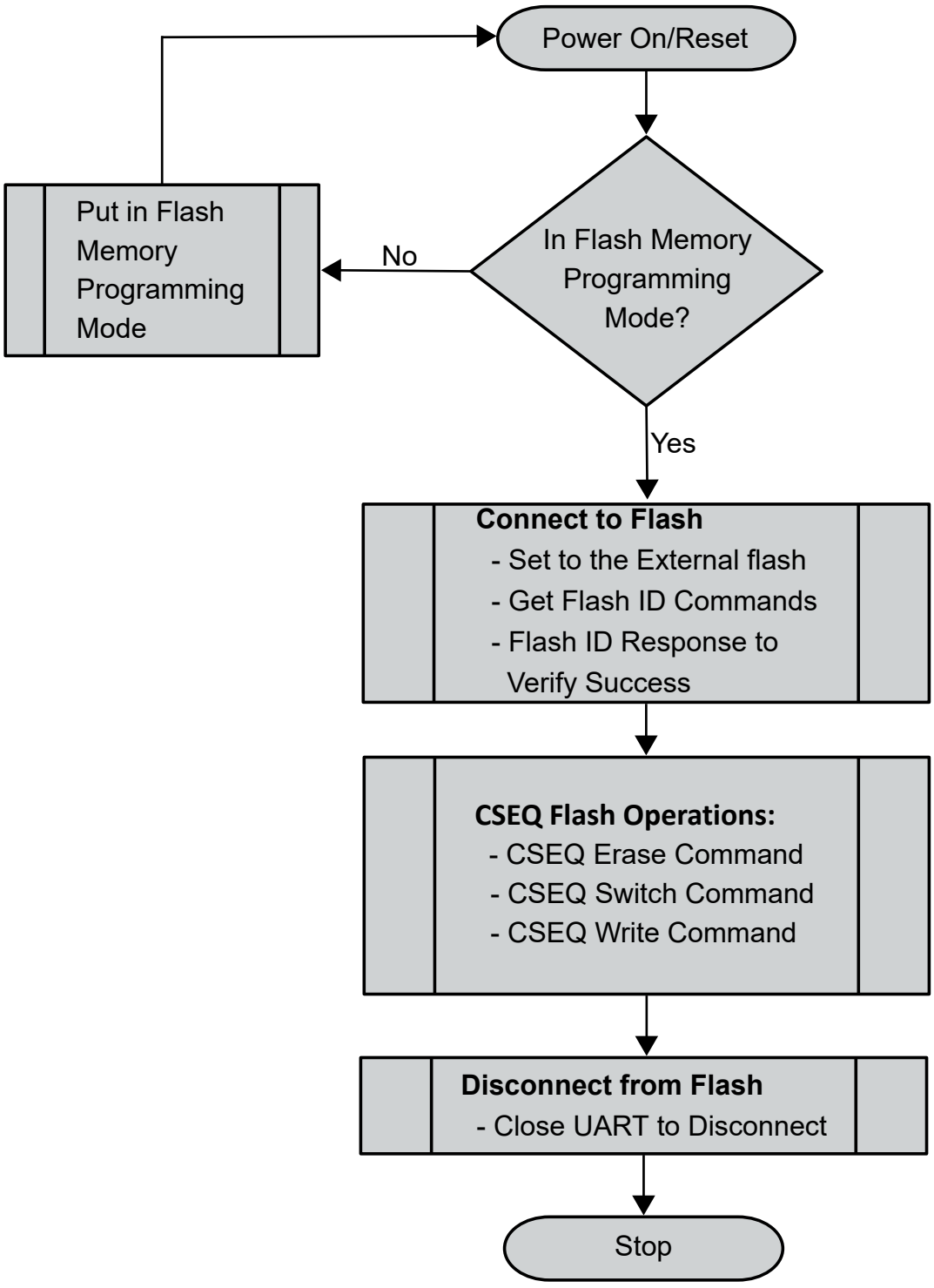
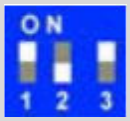


Table 2-1. BM78 and RN4678 EVB Mode Switch Positions

Mode		Switch Positions	Pin Definition		
			1/P2_0	2/P2_4	3/EAN
Flash	Write Flash		ON	ON	ON
ROM	Test (Write EEPROM)		ON	OFF	ON
	Application (default)		OFF	OFF	ON
Flash	Test (Write EEPROM)		ON	OFF	OFF
	Application (default)		OFF	OFF	OFF

Device Firmware Upgrade (DFU) Process

The following are the steps in the DFU process:

1. Entering Flash Programming Mode – Set the pins P2_0, P2_4 and EAN into the write Flash mode; see the preceding table. For more details, refer to the *BM78 Bluetooth® Dual-Mode Module Data Sheet* (DS60001380) and the *RN4678 Bluetooth® Dual Mode Module Data Sheet* (DS50002519). The following table provides the system configuration settings for the BM78 module and the RN4678 module.

Table 2-2. System Configuration Settings

Module	P2_0	P2_4	EAN	Operational Mode
BM78SPPx5NC2 (ROM variant)	Low	High	High	Test mode (write EEPROM)
	High	High	High	Application mode (APP mode) (normal operation)
BM78SPPx5MC2 (Flash variant)	Low	Low	High	Write Flash
	Low	High	Low	Test mode (write EEPROM)
	High	High	Low	APP mode (normal operation)

2. Connect to the Flash – Use the following Command Sequence (CSEQ) commands 0x70 and 0x50 to connect to the Flash via UART in the Flash memory programming process:

- CSEQ Set Flash (Opcode: 0x70) – Use the CSEQ Set Flash command to set the Flash as the external Flash. During the DFU, the BM78 module or the RN4678 module receives the CSEQ Set Flash command as the first Flash operation command.
- CSEQ Get Flash ID (Opcode: 0x50) – Use the CSEQ Get Flash ID command to read the Flash ID from the BM78 module or the RN4678 module. The CSEQ Get Flash ID command returns the Flash ID. For confirmation, after sending the CSEQ Set Flash command, the host MCU performing the DFU must check the Flash ID.

3. CSEQ Flash Operations – After connecting to the Flash, the host MCU carries the following CSEQ Flash operations:
   - CSEQ Flash Erase command (Opcode: 0x51) – Erases the entire external Flash of the BM78 module or the RN4678 module.
   - CSEQ Switch Bank command (Opcode: 0x63) – Before the write Flash command, use the CSEQ Switch Bank command to switch to the target bank.
   - CSEQ write Flash command (Opcode: 0x45) – To write the current bank of Flash with data specified in the CSEQ write Flash command. The maximum data limit is 240 bytes.
4. Disconnect from Flash – After the completion of the DFU, perform a hardware reset after setting the pins P2_0, P2_4 and EAN to APP mode.

3. Firmware Image Manipulation

There are five banks of image files composing the entire firmware. Inside each image file, there are many records indicating which type of hex record the records in the image file represent.

The following are the three types of hex records:

- Bank start record
- Data record or Firmware record
- Bank end record
  Note: The firmware data resides in the data type record.

The file size of each bank of image files in the firmware is 64 Kbytes. Align the data record or the firmware record from the offset 0x0000 of the each bank in ascending order. There is no hole between the records.

Table 3-1. Hex Record Format

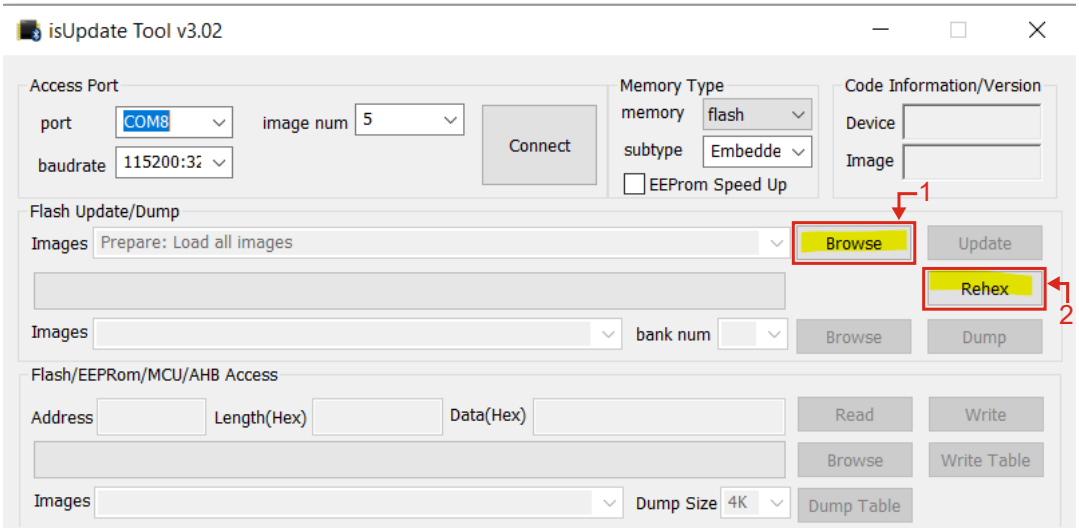
	Start	Data Length	Starting Address	Category	Data	Checksum	End
Nibble#	0	1-2	3-6	7-8	9-N	N+1	N+2
Value	:	0xNN	0x0000 – 0xFFE0	0x04 – Start of bank 0x00 – Data 0x01 – End of bank	Data – up to 32 bytes	0xXX	'\n'

In some exceptional cases, the offset does not always start from 0x0000, and there can be an empty hole between the data/firmware records. The following are the steps to generate one large `.hex` file where each data record or firmware record is placed in sequence using the isUpdate tool; see the following figure:

1. Click **Browse** to select five bank files.
2. Click **Rehex** to initiate the reHex process.
3. The isUpdate tool converts five bank files into one large `.hex` file.

Fill each empty hole and each non-zero offset with an empty record of 0xFF so that the host MCU can download the firmware data in sequence from 0x0000 of bank0 to the end of bank4. At the same time, generate a binary file. In the 6. BM78 Module DFU Demo with SAMG55 Xplained Pro Evaluation Kit, turn the binary file into a large constant C array, which is inside the Flash memory of the host MCU.

Figure 3-1. reHex Operation with isUpdate Tool



4. Data Format of CSEQ Request, CSEQ Response and CSEQ Event

The host MCU sends the CSEQ Requests and expects the corresponding responses from the BM78 module or the RN4678 module. There can be CSEQ Events from the BM78 module or the RN4678 module, and the expected responses are from the host MCU.

Note: All data fields in the following sections are aligned in the big endian.

4.1 Format of CSEQ Request (Host –> BM78)

The host MCU sends the CSEQ Request. The CSEQ payload includes the OPCODE, parameter and Cyclic Redundancy Check (CRC) fields. Any 0x3C byte in the payload must escape with a 0x3C byte, so that the 0x3C 0x3C sequence replaces the original 0x3C. Calculate the CRC against the raw data of the OPCODE and CSEQ parameter without escaping with 0x3C.

Table 4-1. CSEQ Request Format

	CSEQ_DEL (Delimiter)	CSEQ_BEGIN	CSEQ_ OPCODE	CSEQ Parameter	CRC	CSEQ_DEL (Delimiter)	CSEQ_END
	Packet Indicator		**CSEQ Payload**			**Packet End**	
Byte Number	0	1	2	3-N	(N+1) to (N+2)	N+3	N+4
Size (bytes)	1	1	1	3-N	2	1	1
Value	0x3C	0x66	0xXX	0xXXXXXX	0xXXXX	0x3C	0x5A

4.2 Format of CSEQ Event (BM78 –> Host)

On receiving a CSEQ Request, a CSEQ Event returns from the BM78 module or the RN4678 module. The CSEQ Event packet shares the same format of the CSEQ Request. As it does to the CSEQ Request, send a CSEQ Response on receiving the CSEQ Event.

4.3 Format of CSEQ Response (BM78 <–> Host)

A CSEQ Response must be given to the peer on receiving a CSEQ Request or CSEQ Event. The following are the two types of responses:

- Acknowledgment (ACK)
- Non Acknowledgment (NAK)

Note: There is no CRC in the CSEQ Response packet.

The following table provides details about the CSEQ Response format.

Table 4-2. CSEQ Response Format

	CSEQ_DEL (Delimiter)	CSEQ_RESPONSE_CODE
	Packet Indicator	
Byte Number	0	1
Size (bytes)	1	1

.....continued		
	CSEQ_DEL (Delimiter)	CSEQ_RESPONSE_CODE
	Packet Indicator	
Value	0x3C	0x33 (ACK) or 0x55 (NAK)

5. Command Sequence (CSEQ) Flash Request Overview

This chapter provides details about the procedure to perform the DFU with the CSEQ Flash Request. There are five CSEQ Requests to manipulate the Flash as shown in the following table.

After setting P2_0 to ON and P2_4/EAN pins into write Flash mode, the CSEQ Flash Requests are sent in sequence:

1. Set Flash Request
2. Get Flash ID Request
3. Erase Flash Request
4. Switch Bank Request
5. Write Flash Request
6. Repeat steps 4 and 5 until all the banks are written

Table 5-1. CSEQ Flash Request OPCOCE

OPCODE	Parameter Description
0x45 – Write Flash	Write to program space
0x50 – Get Flash ID	Read Flash ID
0x51 – Erase Flash	Erases the entire Flash
0x63 – Switch Bank	Switches the Flash bank
0x70 – Set Flash	Set Flash ID

5.1 CSEQ Set Flash Request

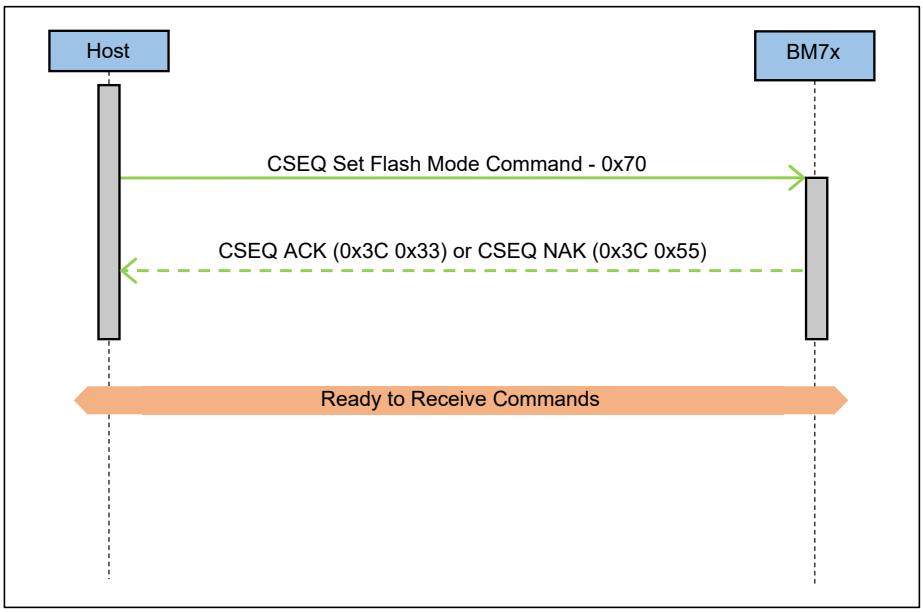
Fix the CSEQ Parameter to 0x01 in the CSEQ Set Flash Request command.

Table 5-2. Set Flash Request Format

	CSEQ_DEL	CSEQ_BEGIN	CSEQ OPCODE	CSEQ Parameter	CSEQ CRC	CSEQ_DEL	CSEQ_END
Byte Number	0	1	2	3	4-5	6	7
Size (bytes)	1	1	1	1	2	1	1
Value	0x3C	0x66	0x70	0x01	0xXXXX	0x3C	0x5A

On receiving the CSEQ Set Flash Request command, the user can get ACK or NAK as one of the responses from the BM78 or the RN4678 module.

Figure 5-1. CSEQ Set Flash Request Sequence



The following figure illustrates the CSEQ Set Flash Request Sequence example data.

Figure 5-2. CSEQ Set Flash Request Sequence Example Data

5.2 CSEQ Get Flash ID Request

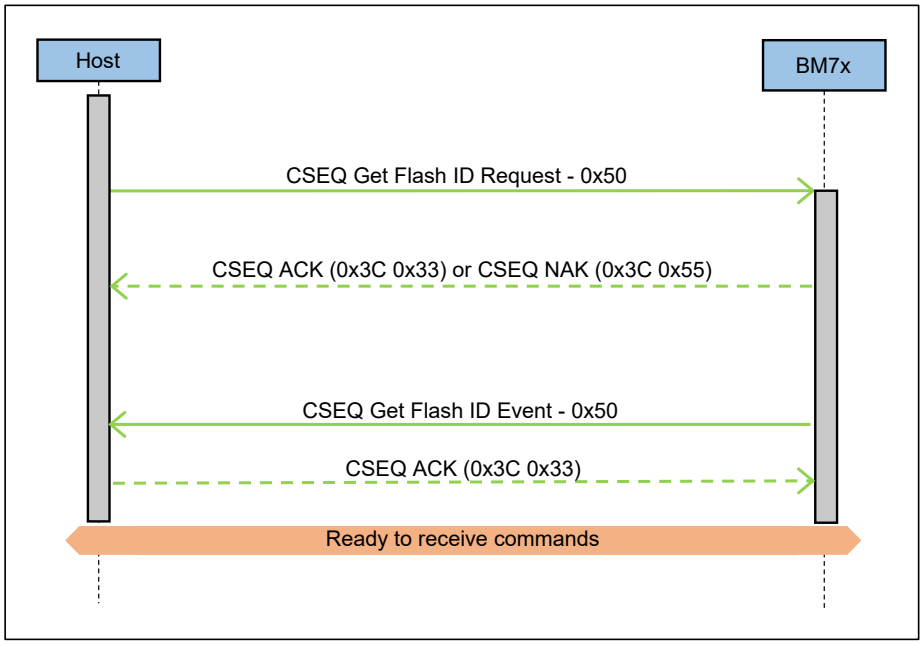
There is no CSEQ Parameter in the CSEQ Get Flash ID Request command.

Table 5-3. Get Flash ID Request Format

	CSEQ_DEL	CSEQ_BEGIN	CSEQ OPCODE	CSEQ CRC	CSEQ_DEL	CSEQ_END
Byte Number	0	1	2	3-4	5	6
Size (Bytes)	1	1	1	2	1	1
Value	0x3C	0x66	0x50	0xXXXX	0x3C	0x5A

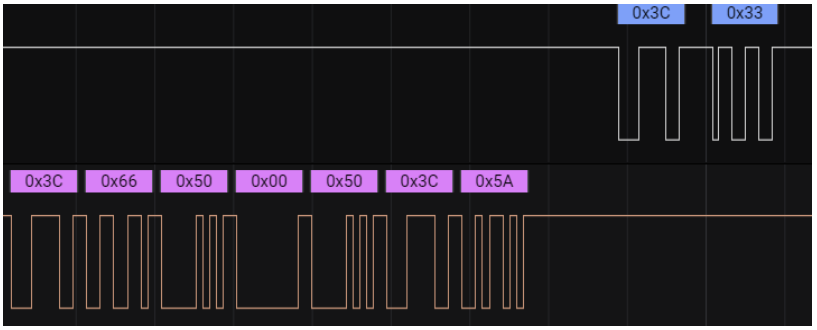
The CSEQ Event returns the Flash ID. The following figure illustrates the CSEQ Get Flash ID Request Sequence.

Figure 5-3. CSEQ Get Flash ID Request Sequence



The following figure illustrates the CSEQ Get Flash ID Request Sequence example data.

Figure 5-4. Get Flash ID Request Sequence Example Data



The CSEQ Event returns the 0x1CBA Flash ID. The following figure illustrates the CSEQ Get Flash ID Request Event example data.

Figure 5-5. CSEQ Get Flash ID Request Event Example Data

5.3 CSEQ Erase Flash Request

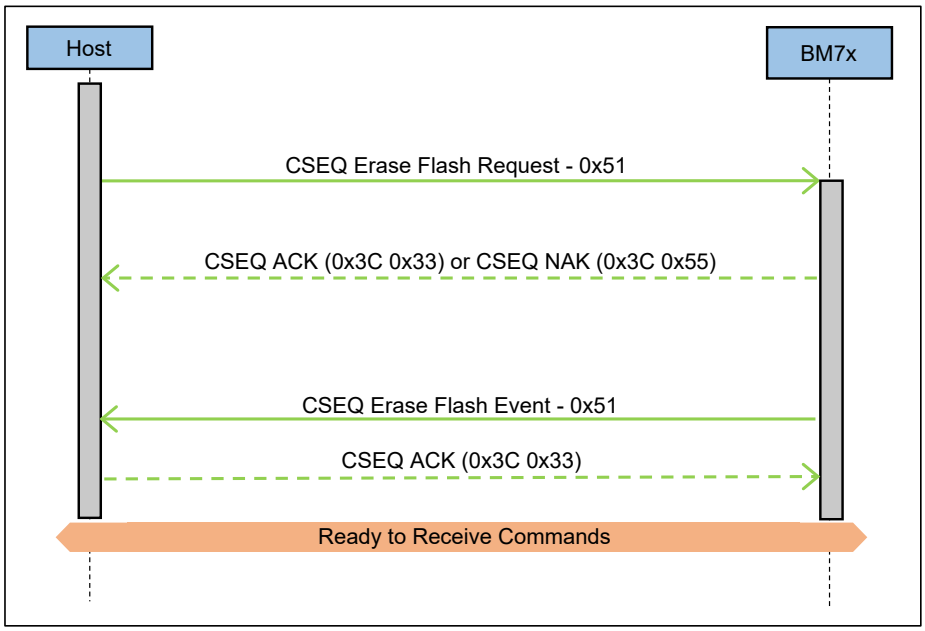
There is no CSEQ Parameter in the CSEQ Erase Flash Request command.

Table 5-4. Erase Flash Request Format

	CSEQ_DEL	CSEQ_BEGIN	CSEQ OPCODE	CSEQ CRC	CSEQ_DEL	CSEQ_END
Byte Number	0	1	2	3-4	5	6
Size (bytes)	1	1	1	2	1	1
Value	0x3C	0x66	0x51	0xXXXX	0x3C	0x5A

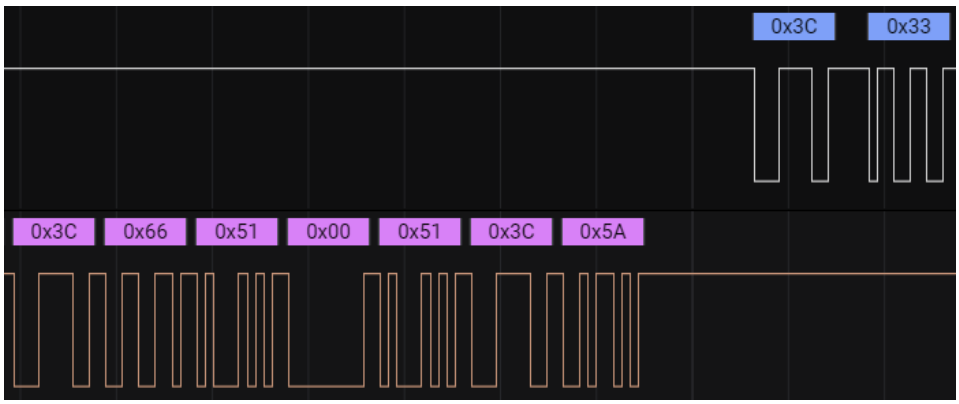
On receiving the CSEQ Erase Flash Request command, the user can get ACK or NAK as one of the responses from the BM78 or the RN4678 module. The CSEQ Erase Request command can take time to send the status to the host MCU.

Figure 5-6. CSEQ Erase Flash Request Sequence



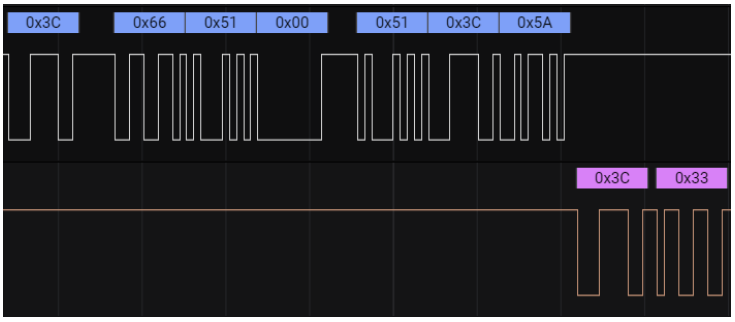
The following figure illustrates the CSEQ Erase Flash Request Sequence example data.

Figure 5-7. CSEQ Erase Flash Request Sequence Example Data



The following figure illustrates the CSEQ Erase Flash Request Event example data.

Figure 5-8. CSEQ Erase Flash Request Event Example Data



5.4 CSEQ Switch Bank Request

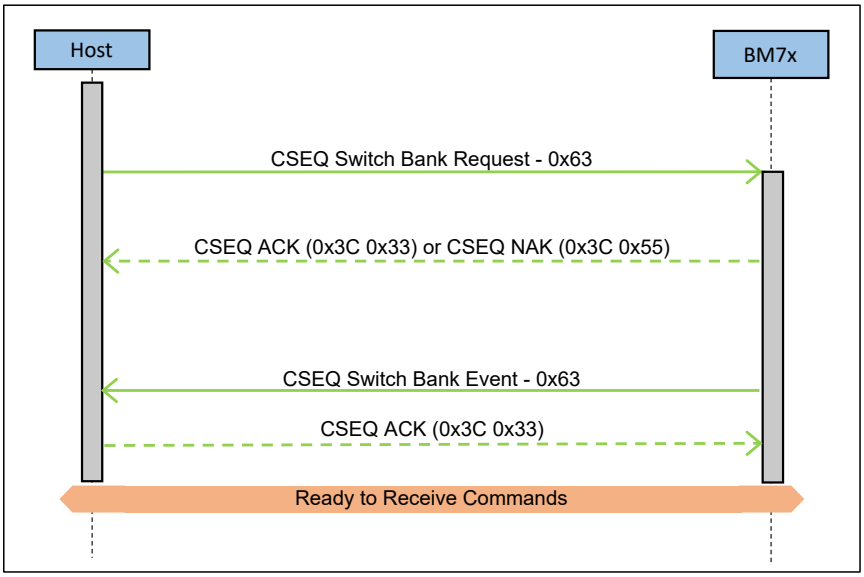
Before the write Flash operation, send the CSEQ Switch Bank command to set the target bank. The bank number is set in the CSEQ Parameter field.

Table 5-5. Switch Bank Request Format

	CSEQ_DEL	CSEQ_BEGIN	CSEQ OPCODE	CSEQ Parameter	CSEQ CRC	CSEQ_DEL	CSEQ_END
Byte Number	0	1	2	3	4-5	6	7
Size (bytes)	1	1	1	1	2	1	1
Value	0x3C	0x66	0x63	Bank number	0xXXXX	0x3C	0x5A

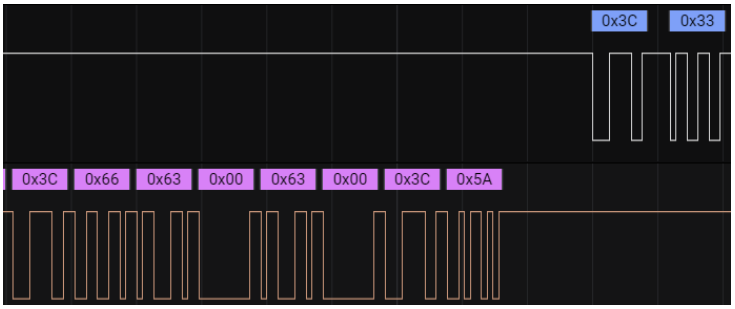
On receiving the CSEQ Switch Bank Request command, the user can get ACK or NAK as one of the responses from the BM78 module or RN4678 module. After receiving the CSEQ Response, send the CSEQ Switch Bank Event from the BM78 or the RN4678 module with the same format as the CSEQ Switch Bank Request.

Figure 5-9. CSEQ Switch Bank Request Sequence



The following figure illustrates the CSEQ Switch Bank Request Sequence example data.

Figure 5-10. CSEQ Switch Bank Request Sequence Example Data



The following figure illustrates the CSEQ Switch Bank Request Event example data.

Figure 5-11. CSEQ Switch Bank Request Event Example Data

5.5 CSEQ Write Flash Request

The following are the two parameters to consider for the CSEQ write Flash Request:

- Offset of the firmware data to send
- Firmware data

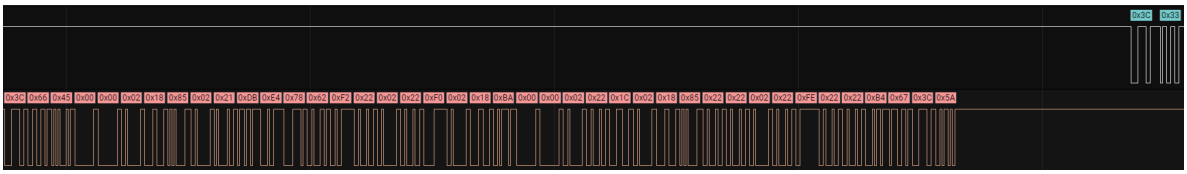
The maximum limit for the firmware data is 240 bytes. After Flashing the firmware by the BM78 or the RN4678 module, the BM78 or the RN4678 module returns an CSEQ Event. The CSEQ Event consists of the firmware offset and the firmware data length.

Table 5-6. Write Flash Request Format

	CSEQ_DEL	CSEQ_BEGIN	CSEQ_ OPCODE	CSEQ_ OFFSET	CSEQ_DATA	CSEQ_CRC	CSEQ_DEL	CSEQ_END
Byte Number	0	1	2	3 - 4	5-n	n+1-n+2	n+3	n+4
Size (bytes)	1	1	1	2	n	2	1	1
Value	0x3C	0x66	0x45	0xXXXX	0xXXXX…	0xXXXX	0x3C	0x5A

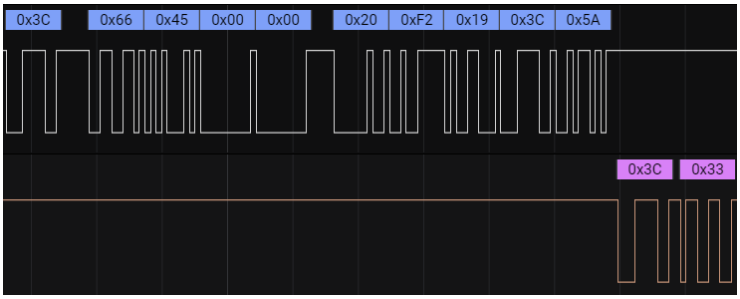
The following figure illustrates the Write Flash Request Sequence example data. In 6. BM78 Module DFU Demo with SAMG55 Xplained Pro Evaluation Kit, the firmware data length is set to 32.

Figure 5-12. Write Flash Request Sequence Example Data



The following figure illustrates the Write Flash Request Event example data and the CSEQ Response. In the CSEQ event, the 0x0000 is the previous firmware data offset and 0x20 is the data length of the firmware chunk; see the following figure.

Figure 5-13. Write Flash Request Event Example Data



5.6 Cyclic Redundancy Check (CRC) Calculation

Calculate the CRC against the raw payload without escaping with 0x3C. The algorithm is available in the `BM78_DU.c` file. For more details, refer to 6.2. SAMG55 Xplained Pro Evaluation Board Firmware Setup. If the result of the CRC calculation contains 0x3C, then it escapes with the new 0x3C 0x3C.

6. BM78 Module DFU Demo with SAMG55 Xplained Pro Evaluation Kit

The DFU demo of the BM78 module uses the SAMG55 Xplained Pro Evaluation board (SAMG55 XPRO board) and BM78-PICtail™ board. The SAMG55 XPRO board controls the whole DFU process of the BM78 module using the UART.

Note: As an example, the demo is only shown for the BM78 module.

6.1 DFU Hardware Setup of the BM78 Module

This chapter describes the DFU hardware setup of the BM78 module. The following are the steps involved in the DFU of the BM78 module:

1. To power the SAMG55 XPRO board, connect the EDEBUG USB of the SAMG55 XPRO board to the PC.
2. Open the Tera Term tool on the PC.
3. Connect the pin13 UART_RX on EXT1 of the SAMG55 XPRO board to pin9 BT_UART_TX on J1 of the BM78-PICtail™ board; see the following table.
4. Connect the pin 14 UART_TX on EXT1 of SAMG55 XPRO board to the pin 11 BT_UART_RX on J1 of the BM78-PICtail™ board; see the following table.
5. To power the BM78-PICtail™ board, connect the pin 4 3v3 on J100 of the SAMG55 XPRO board to the pin 26 EXT_3v3 on J1 of the BM78-PICtail™ board; see Table 6-2.
6. Connect the pin2 GND on J100 of the SAMG55 XPRO board to the pin 28 GND on J1 of the BM78-PICtail™ board; see Table 6-2.
7. The BM78-PICtail™ board controls the P2_0, P2_4, EAN and RESET pin and to ease the connection setup P2_0, P2_4, EAN and RESET pin are not connected to the SAMG55 XPRO board.
8. Use the SW4 switch to set the BM78-PICtail™ board in write Flash mode with all pins set to ON, then, perform a hardware reset by pressing the SW3 Reset button.
   Note: The blue D1 LED starts blinking on the BM78-PICtail™ board indicating the BM78-PICtail™ board is set to write Flash mode.

Figure 6-1. DFU Hardware Setup of the BM78 Module

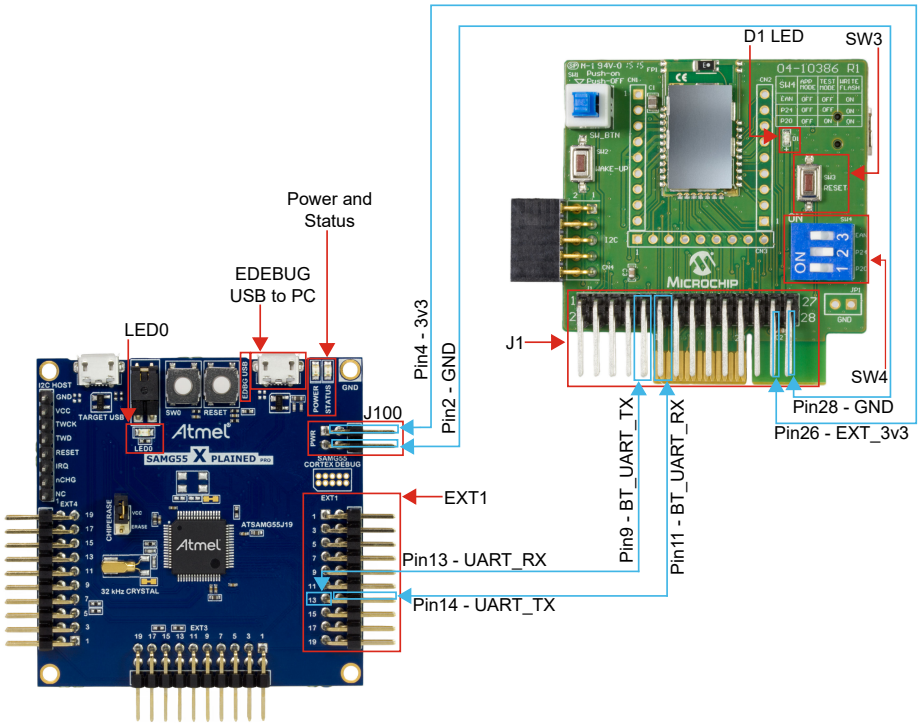


Table 6-1. UART Connection between the SAMG55 XPRO Board and the BM78 PICtail™ Board

	SAMG55 XPRO Board Pins	BM78-PICtail™ Board Pins
UART Connection	Pin13 – UART_RX	Pin9 – BT_UART_TX
	Pin14 – UART_TX	Pin11 – BT_UART_RX

Table 6-2. Power Connection between the SAMG55 XPRO Board and the BM78 PICtail™ Board

	SAMG55 XPRO Board Pins	BM78-PICtail™ Board Pins
Power Connection	Pin4 – 3v3	Pin26 – EXT_3v3
	Pin2 – GND	Pin28 – GND

6.2 SAMG55 Xplained Pro Evaluation Board Firmware Setup

This section provides an overview of the SAMG55 Xplained Pro Evaluation board (SAMG55 XPRO board) firmware setup. Go to github.com/MicrochipTech/BM78_DFU_with_SAMG55 for the code and documentation related to the SAMG55 XPRO board firmware setup. The following sections provide details about the SAMG55 XPRO board firmware setup:

Open the MPLAB®-X Project

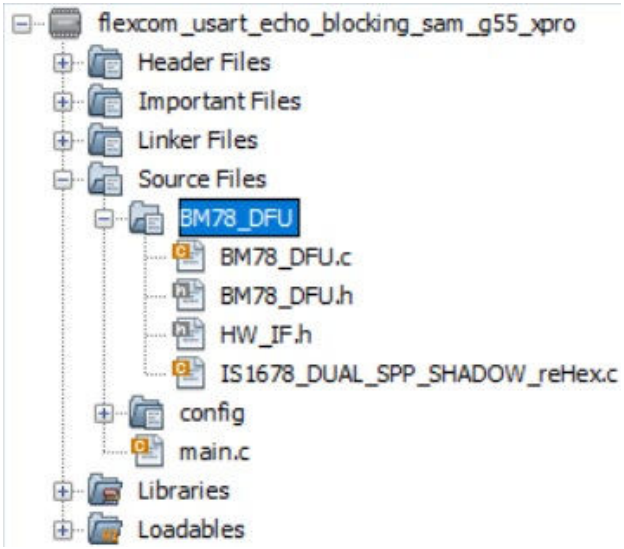
The SAMG55 firmware is designed with the latest revision of the MPLAB®-X and MPLAB® Harmony. Open the MPLAB®-X project and the user can see the BM78_DFU folder.

Note: The user only uses the `BM78_DFU()` function at the application level.

The BM78_DFU folder contains the following files:

- `BM78_DFU.c` – DFU code
- `BM78_DFU.h` – DFU header file
- `HW_IF.h` – Contains the hardware relevant API
- `IS1678_DUAL_SPP_SHADOW_reHex.c` – BM78 1v38 reHex image

Figure 6-2. MPLAB-X Project Organization

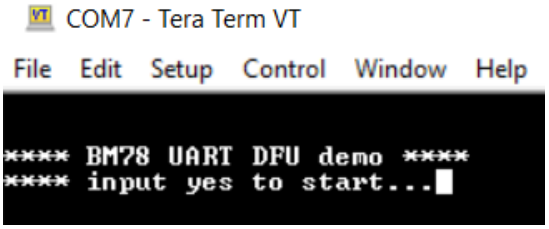


Run the SAMG55 Firmware

The following are the steps to run the SAMG55 firmware:

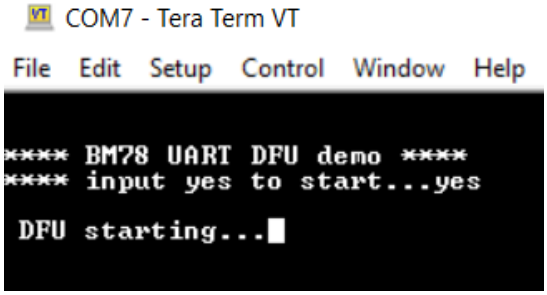
1. Put the BM78 module in write Flash mode manually. For more details, refer to 2.1. BM78 and RN4678 Flash Memory Programming.
2. Open the Tera Term software tool on the PC.
3. Compile and download the SAMG55 firmware from the MPLAB®-X IDE.
4. The following figure illustrates the opening window of the Tera Term tool, which displays the *input yes to start* message to start the BM78 module UART DFU process.

   Figure 6-3. DFU Initialization Screen



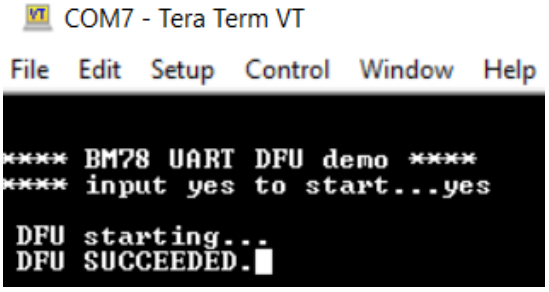
5. Enter the input *yes* to start the BM78 module UART DFU process; see the following figure.

   Figure 6-4. Input *yes* Screen – DFU Starting



6. After the successful completion of the BM78 module UART DFU process, the LED0 on the SAMG55 XPRO board turns ON. The Tera Term software tool also displays the *DFU SUCCEEDED* message; see the following figure.

   Figure 6-5. DFU Succeeded



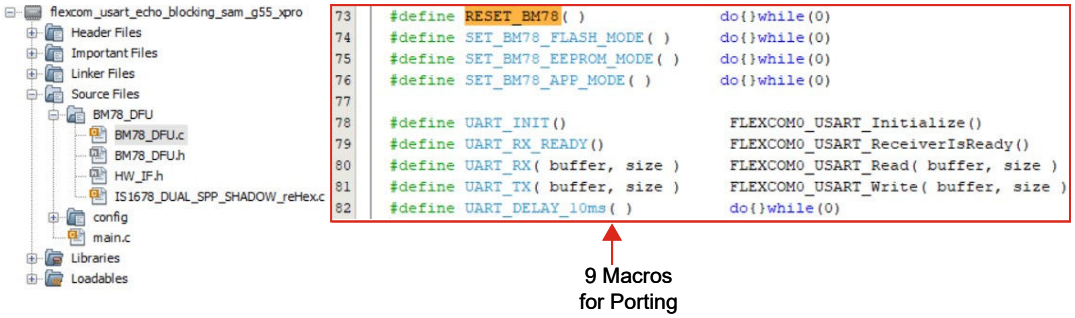
7. Port DFU Demo Code

The reference code is designed for easy porting to other MCU and its framework, if the user is not using SAMG55 XPRO board and MPLAB® Harmony framework.

The hardware relevant API is declared in the HW_IF header file. If there is any need for modification, the user needs to modify these nine macros; see the following figure. The nine API are categorized into three types:

- GPIO control
- UART interface
- Delay API (optional for more responsiveness)

Figure 7-1. Macros for Porting



Note: The `BM78-1V38-DFU-log-32Byte.sal` UART log file in saleae Logic2 format is only given for reference. Go to github.com/MicrochipTech/BM78_DFU_with_SAMG55 for the UART log file in saleae Logic2 format related to the port DFU demo code.

8. Document Revision History

Revision	Date	Section	Description
A	12/2021	Document	Initial Revision

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