TB3175

What is SSC? How to Configure SSC for Audio Applications

Introduction

The Synchronous Serial Controller (SSC) is a serial synchronous communication module available on Microchip's 32-bit ARM Cortex™-M3, Cortex™-M4 and Cortex™-M7 series of microcontrollers (MCUs). The SSC supports multiple synchronous communication protocols generally used in audio and telecom applications, such as I^2S (Inter-IC Sound), Short Frame Sync, and Long Frame Sync. The SSC has independent transmitter and receiver modules, and a common clock divider module. The SSC interface uses data, clock, and frame sync signals for transmission and reception.

The SSC used in conjunction with DMA, enables continuous high data rate transfers without processor intervention, typically used in Audio applications connecting over the I^2S interface.

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1. Description

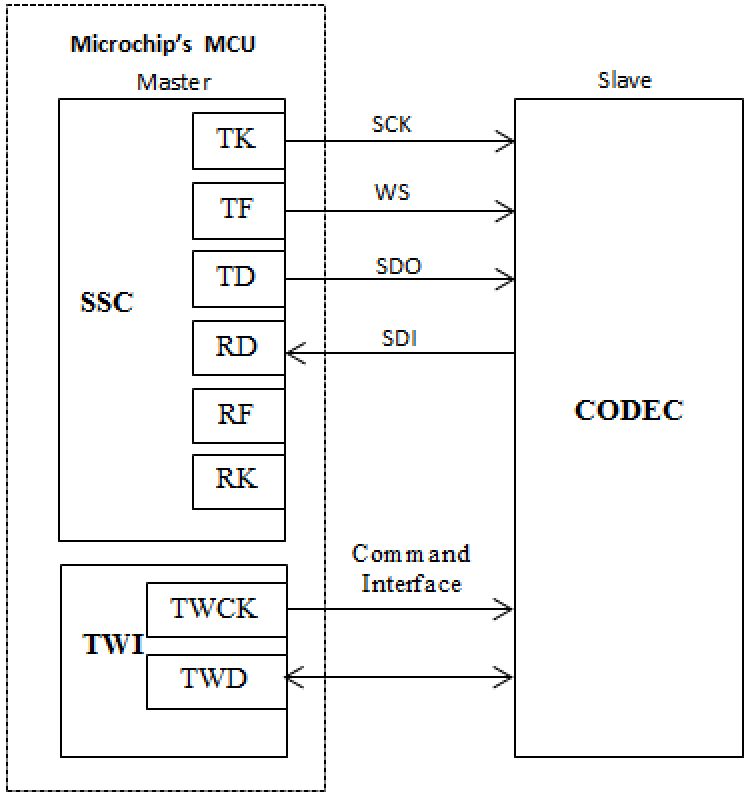
The SSC is placed on the peripheral bridge of the microcontroller. The peripheral bus provides the clock to the SSC, which is configured and enabled through the Power Management Control (PMC) module. The SSC interfaces with the general-purpose extended Direct Memory Access controller (XDMAC) to enhance operational performance. It has three interface signals, TD/RD, TF/RF and TK/RK, for data transmission and reception routed through the Peripheral Input Output (PIO) controller. The following table represents the description of the SSC signals.

Table 1-1. SSC Signals

Pin Name	Pin Description	Type
RF	Receive Frame Synchronization	Input/Output
RK	Receive Clock	Input/Output
RD	Receive Data	Input
TF	Transmit Frame Synchronization	Input/Output
TK	Transmit Clock	Input/Output
TD	Transmit Data	Output

Interfacing an MCU to an audio CODEC module provides a typical example of using the SSC to interface over the I^2S protocol. The CODEC has two interfaces: an audio data interface over I^2S protocol, and a command interface, typically over the I^2C protocol. Microchip's 32-bit ARM Cortex MCUs have a Two Wired Interface (TWI). TWI is Microchip's serial interface compatible with I^2C. The following figure represents the typical connection of the SSC (on a Cortex MCU) to a CODEC device for stereo output and mono input. The MCU acts as the I^2S master and therefore, provides clock to the slave (CODEC).

Figure 1-1. SSC-I²S Interface



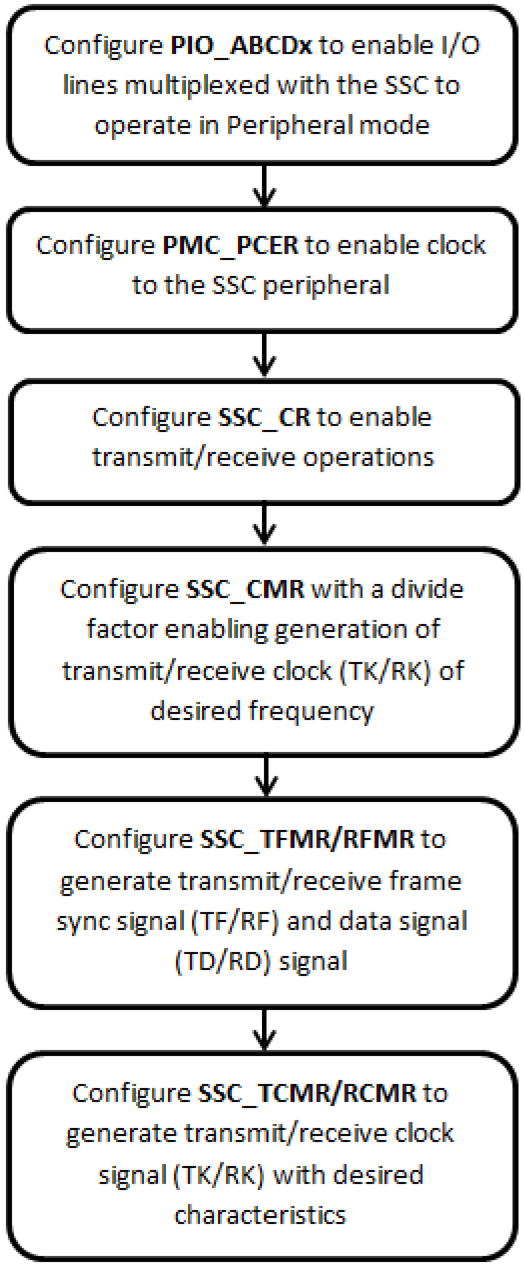
The command interface (TWI) signals from the MCU to the CODEC, and the correspondence of SSC signals to I²S protocol signals.

Note: The configuration registers discussed in the following sections are applicable to Cortex-M7 devices. For details of registers on Cortex-M3 and Cortex-M4 devices, refer to the specific device data sheet.

2. Configuring the SSC and XDMAC

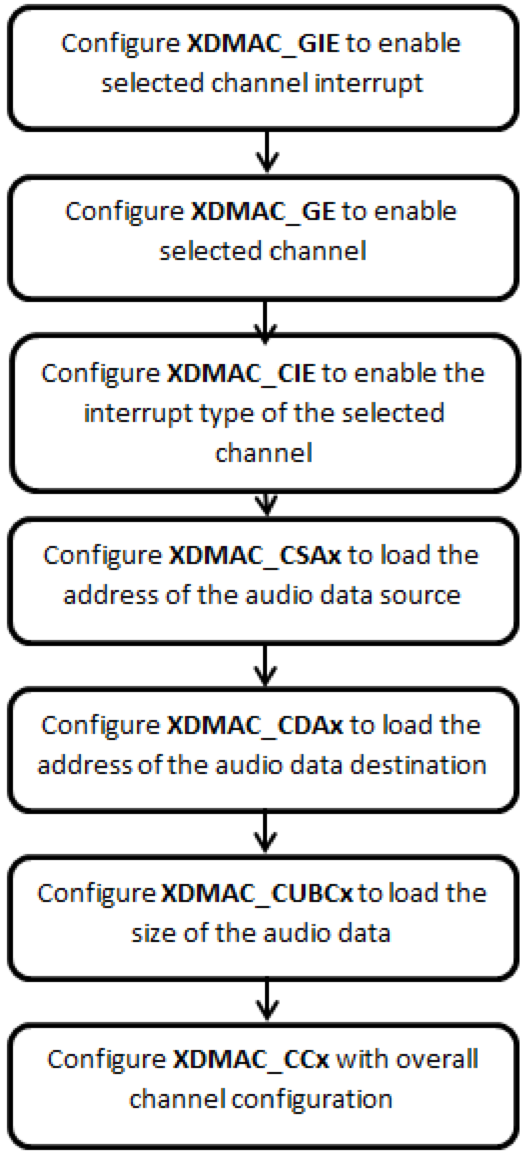
The following figure shows the flow sequence of registers to configure when interfacing SSC to an audio CODEC.

Figure 2-1. SSC Configuration Sequence



The following figure shows the flow sequence of registers to configure the XDMAC, when the XDMAC is used to optimize operational performance of the SSC.

Figure 2-2. XDMAC Configuration Sequence



3. Tips

1. The SSC provides three clock source options to generate the TK/RK.
   For the transmitter, the supported clock sources are:
   - MCK: Divided internal peripheral clock
   - Receive Clock (RK): Receiver clock acts as an input to generate the transmitter clock
   - Transmit Clock (TK): Externally generated clock is available as input on the TK pin

   For the receiver, the supported clock sources are:
   - MCK: Divided internal peripheral clock
   - Receive Clock (RK): Externally generated clock is available as input on the RK pin
   - Transmit Clock (TK): Transmitter clock acts as an input to generate the receiver clock

   Note:
   1. The CKS field in the SSC_TCMR/SCC_RCMR registers provides options to specify the clock source.
   2. When the clock source is MCK, the divisor value for the internal peripheral clock is specified in the SSC_CMR register.
2. To configure the SSC registers to transfer audio data with 16-bit width, use two channels and a 48000 Hz sampling rate when the MCU is acting as an I^2S master.

   2.1. The following divide factor should be programmed in SSC_CMR to enable generation of TK from the internal peripheral clock (MCK).
   When interfaced with an I^2S device, the Transmit Clock (TK) signal corresponds to the bitrate for the desired audio data.

   I^2S bitrate = Number of bits per Channel * Number of Channels * Sampling Frequency

   I^2S bitrate =16 * 2 * 48000 = 1536000 Hz

   Therefore, the SSC needs to produce a TK of **1536000 Hz.** To generate the required TK, the SSC peripheral provides an option to divide its internal peripheral clock by an integer factor.

   For a MCK of 150 MHz, Integer Factor Divisor => MCK/TK => 150 MHz/1536000 => 97.65 => 98

   By default the SSC divides the internal clock by two, therefore the factor to be programmed in the SSC clock mode register **SSC_CMR** = 49.

   2.2. What settings are to be programmed in the SSC_TFMR register to generate a transmit frame sync (TF)?

Table 3-1. Programmable Settings in SSC_TFMR

Field	Value	Description
DATLEN	15	DATLEN+1 corresponds to the data word length
DATDEF	0	Default data value 0
MSBF	1	MSB is sent first
DATNB	1	DATNB+1 words per frame
FSLEN	15	FSLEN+1 clock cycles length of each frame sync pulse
FSOS	1	Frame sync output enabled on negative TK pulse

Field	Value	Description
FSDEN	0	Frame sync data is driven with default data value (DATDEF)
FSEDGE	0	Frame sync edge detection enabled for positive pulse
FSLEN_EXT	0	Extended pulse length disabled

2.3. What settings are to be programmed in the SSC_TCMR register to generate the TK?

Table 3-2. Programmed Settings to Generate the TK

Field	Value	Description
CKS	0	Divided MCK clock is the source to generate TK
CKO	1	Continuous TK clock so as to toggle
CKI	0	Data is shifted out on TK falling edge
CKG	0	No gating for TK, it is always enabled
START	7	Start data transmission on the detection of an edge
STTDLY	1	1 clock cycle delay before transmission could start (Corresponding to I^2S protocol)
PERIOD	15	Bit Width (16)-1, hence that frame length (left and right channels) of 32 bit width is achieved

4. Relevant Resources

- Synchronous Serial Controller (SSC) of SAMV71 Devices to Output an Audio Stream Through the On-board WM8904 CODEC
  http://asf.atmel.com/docs/latest/sam.components.audio.codec.wm8904.example.samv71_xplained_ultra/html/index.html
- Synchronous Serial Controller (SSC) of SAM3S Devices to Output an Audio Stream Through the On-board WM8731 CODEC
  http://asf.atmel.com/docs/latest/sam.components.audio.codec.wm8731.example.sam3x_ek/html/index.html
- ASF SSC in I^2S Mode Example – EVK 1100
  http://asf.atmel.com/docs/latest/avr32.drivers.ssc_i2s.example.evk1100/html/index.html
- ASF SSC in I^2S Mode Example – EVK 1101
  http://asf.atmel.com/docs/latest/avr32.drivers.ssc_i2s.example.evk1101/html/index.html
- Connecting the Atmel ARM-based Serial Synchronous Controller (SSC) to an I^2S-compatible Serial Bus
  http://www.atmel.com/Images/doc6020.pdf
- How to use the SSC in I^2S mode
  http://www.atmel.com/Images/doc32127.pdf
- Usage of XDMAC on SAM S/SAM E/SAM V
  http://www.atmel.com/Images/Atmel-42761-Usage-of-XDMAC-on-SAMS-SAME-SAMV_ApplicationNote_AT17417.pdf

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