Application Note

Using Two KSZ8795CLX Family Switches for a Non-blocking Max 8 ports Fast Ethernet Switch

Introduction

The KSZ8795CLX is a highly integrated Layer 2 managed 5-port switch, Port 5 GMAC5 supports RGMII/GMII/MII/RMII interface, apply port 5 RGMII Gigabit interface that can be used for a non-blocking 8-port switch, two KSZ8795CLX switches need a back to back connection through their port 5 Gigabit RGMII interfaces, KSZ8795CLX has a small 80-pin LQFP package and low power consumption. In this app note, we describe RGMII interface connections for this 8-port fast Ethernet switch.

RGMII Connections for KSZ8795CLX

Strap-in Pin for Port 5 GMAC5 Interface

- Port 5 GMAC5 interface modes

LED3[1,0]	Port 5 GMAC5 Interface Mode
0,0	MII for SW5-MII
0,1	RMII for SW5-RMII
1,0	GMII for SW5-GMII
1,1	RGMII for SW5-RGMII (Default)

- Keep strap-in pins LED3[1,0]='11' (default with internal pull-up) for using RGMII Gigabit interface.

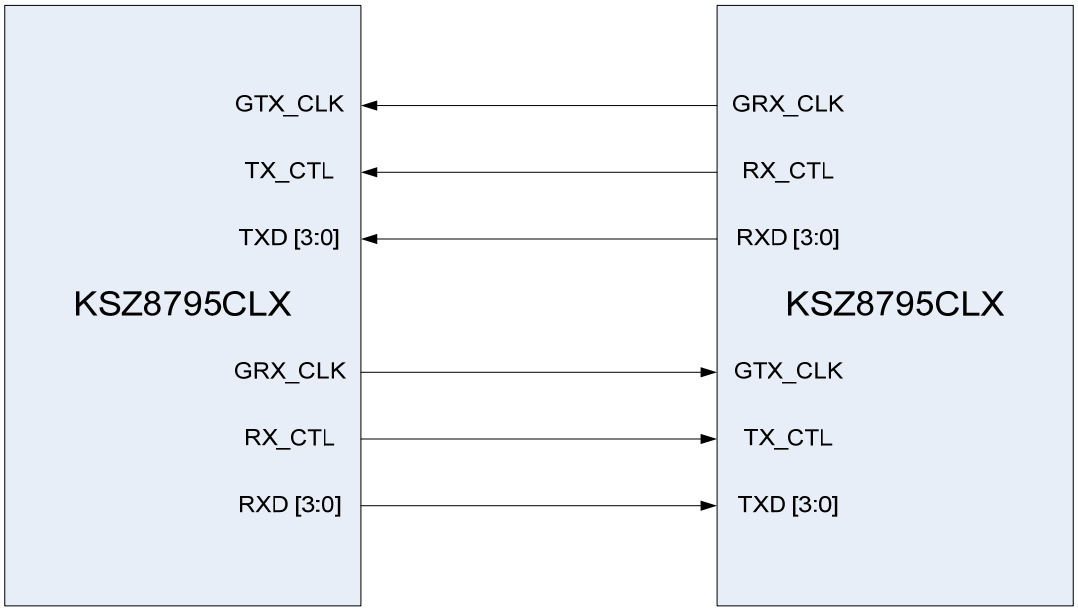
Connection Signals for Port 5 MAC 5 SW5-RGMII Interface

The Table below shows the RGMII reduced connections when connecting with back to back:

Two KSZ8795CLX Switches with Back to Back Gigabit Connection			
KSZ8795CLX Switch #1 SW5-RGMII Signals	**Type**	**KSZ8795CLX Switch #2 SW5-RGMII Signals**	**Type**
RXD5_CTL	Output	TXD5_CTL	Input
RXD5[3:0]	Output	TXD5[3:0]	Input
GRX5_CLK	Output	GTX5_CLK	Input
TXD5_CTL	Input	RXD5_CTL	Output
TXD5[3:0]	Input	RXD5[3:0]	Output
GTXC5	Input	GRXC5	Output

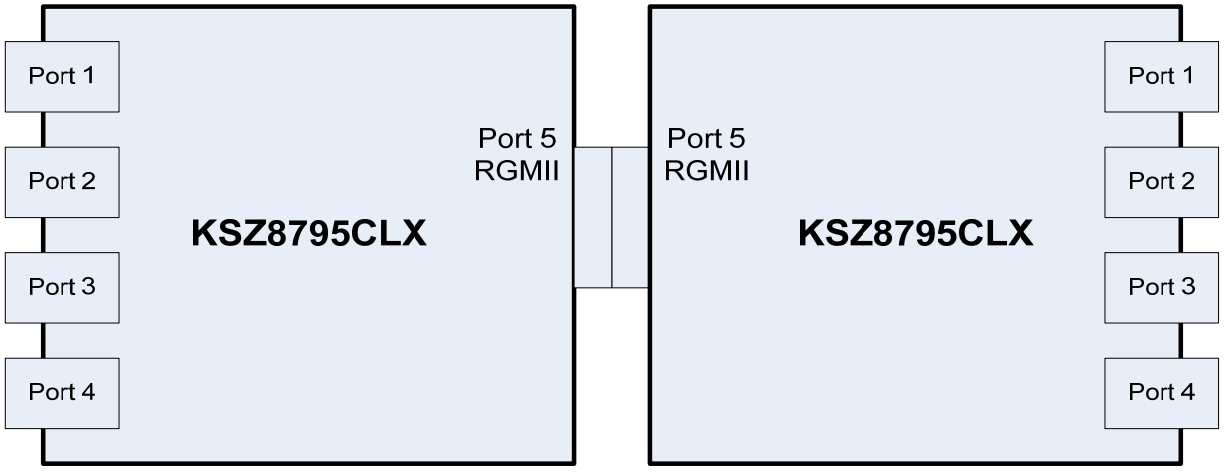
The RGMII interface operates at up to a 1000Mbps speed rate. The transmit signals and receive signals should be equal length and as short as possible for both transmit signals group and receiving signals group in design. The port 5 interface control 6 Register 86 can keep its default value for RGMII interface.

RGMII Signals Connection:



Unmanaged standalone Non-blocking 8-port Fast Ethernet Switch

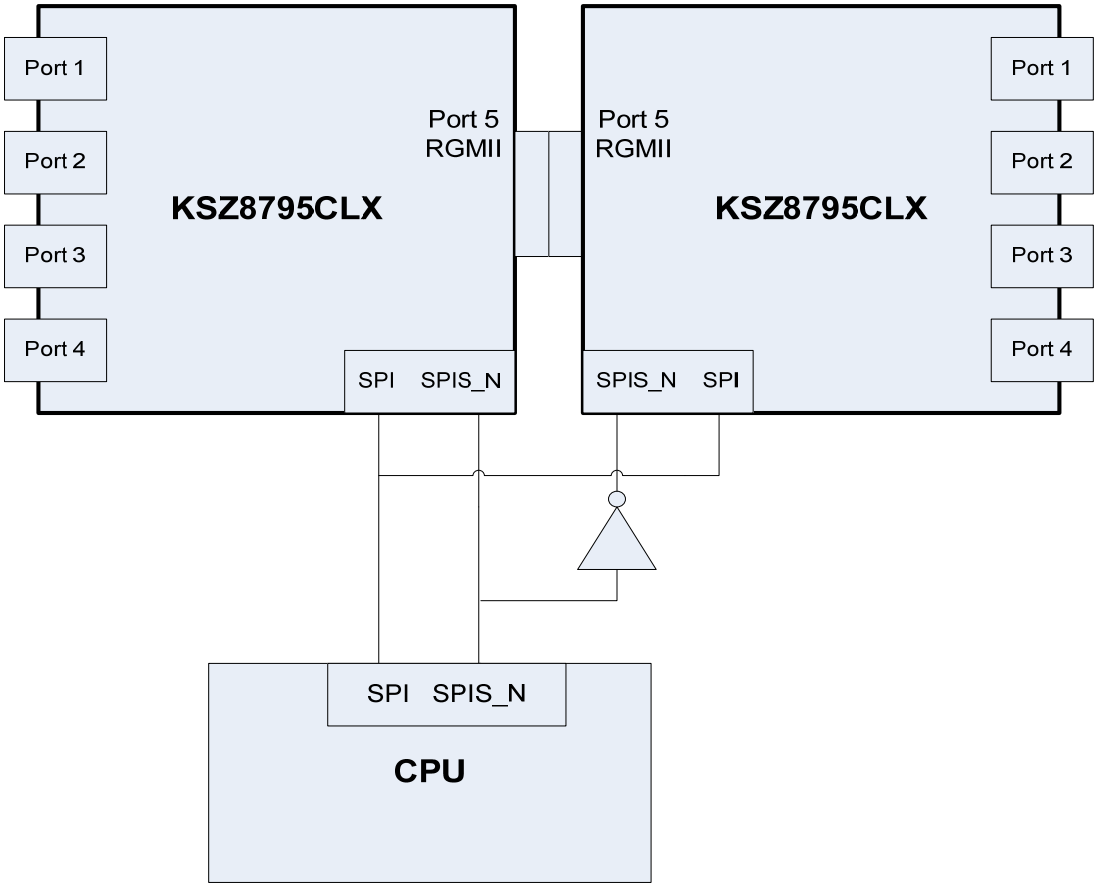
Block Diagram



All registers can keep their default values.

Managed Non-blocking 8-port Fast Ethernet Switch

Block Diagram

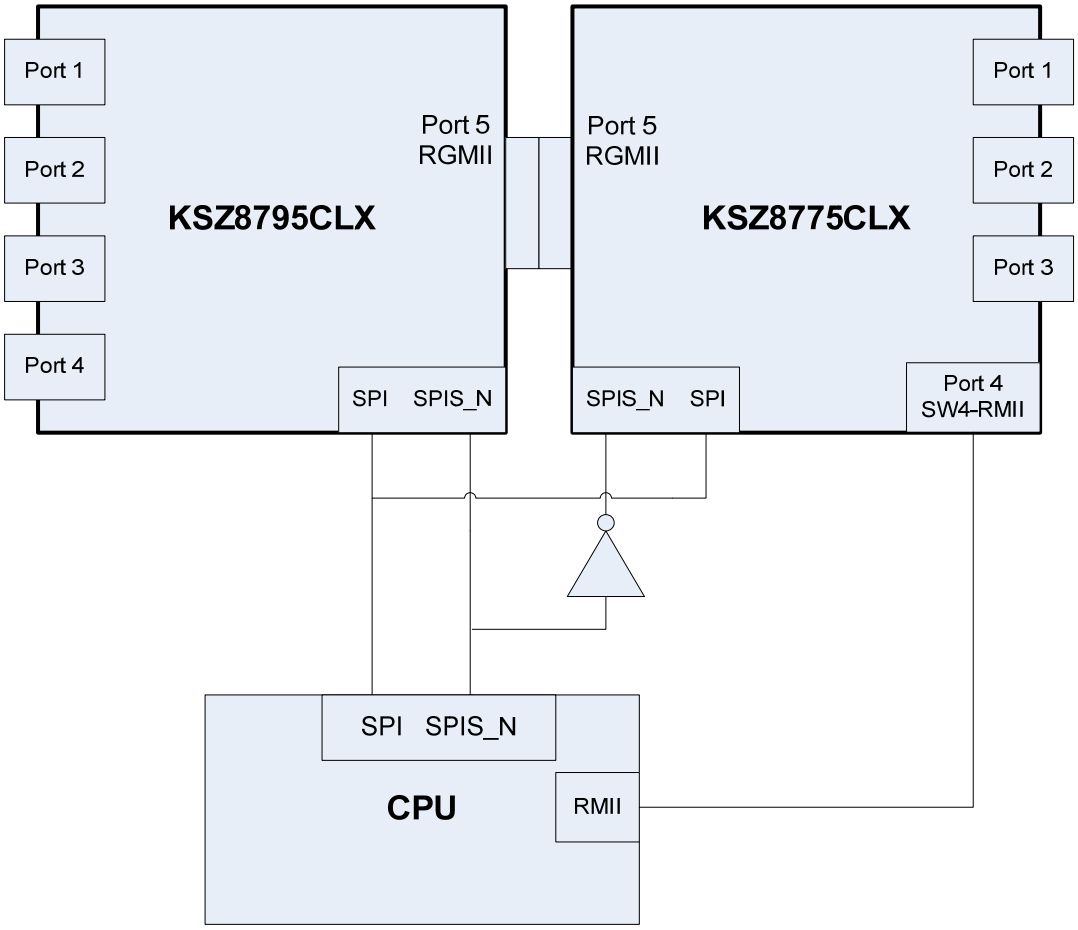


In managed 8-port switch diagram above, the SPIS_N pin can be controled by CPU to access registers between two KSZ8795CLX switches through SPI interface. CPU can set both switches's registers based on real application.

KSZ8795CLX Signal Name	Signal Description
SPIS_N	SPI Interface Select (Select device #1 or device #2 registers access)
SCL	SPI Clock (parallel connection)
SDA	Input (parallel connection)
SPIQ	Output (parallel connection)

Managed Non-blocking 7-port Fast Ethernet Switch

Block Diagram



In managed 7-port switch diagram above, the SPIS_N pin can be controled by CPU to access registers between one KSZ8795CLX and one KSZ8775CLX switches through SPI interface. CPU can set both switches's registers based on real application and can transfer Ethernet packets between CPU and this 7-port swith through RMII interface.

KSZ8795CLX KSZ8775CLX Signal Name	Signal Description
SPIS_N	SPI Interface Select (Select device #1 or device #2 registers access)
SCL	SPI Clock (parallel connection)
SDA	Input (parallel connection)
SPIQ	Output (parallel connection)

Conclusion

There is an option to build a non-blocking 8-port switch by using two KSZ8795CLX switches. For the detail device information, please see their datasheets in www.micrel.com