AVR503: Replacing AT90S/LS2323 or AT90S/LS2343 with ATtiny25

Features

- · General Porting Considerations
- Memories
- System Clock and Clock Options
- System Control and Reset
- Registers
- Interrupt Vectors
- I/O Ports
- Memory Programming
- · Electrical Characteristics

1 Introduction

This application note is a guide to assist users of AT90S/LS2323 and, AT90S/LS2343 converting existing designs to ATtiny25.

In addition to the differences described in this document, the electrical characteristics of the devices are different. Some of the electrical differences are outlined in this document and some are not. Please check the latest data sheets for detailed information.

Improvements or added features in ATtiny25 that are not in conflict with those in AT90S/LS2323 or AT90S/LS2343 are not listed in this document.



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Application Note

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2 General Porting considerations

The information in this document applies to AT90S/LS2323 and AT90S/LS2343, except where otherwise noted. For the remainder of the document, the term "AT90S/LS23x3" will be used for referring to all four parts in general.

Between the ATtiny25 and AT90S/LS23x3, some registers and register bits have changed name but note that they preserve the same functionality. They are all listed later in this document.

In relation to code porting, it is an advantage if register names and bit definitions has been used as substitution of these names and definitions can be performed rather painlessly. If absolute register addresses and bit values have been used in the code that is to be ported, the effort to port it is slightly higher – but never the less possible to overcome.

Examples using register and bit definitions are shown below.

Some of the reserved bits of AT90S/LS23x3 are in use on ATtiny25. To avoid conflicts with added features and register functionality, please ensure that reserved bits and registers are not written. Reserved bits should always be written to zero if accessed. Using register and bit definitions will in general ensure that reserved bits are not accessed incorrectly and will thus ensure forward compatibility.

2.1 Summary of Parts

Table 2-1 summarizes the device specific features of AT90S/LS2323 and AT90S/LS2343.

Table 2-1. Summary of Device Specifics.

	AT90S2323	AT90LS2323	AT90S2343	AT90LS2343	ATtiny25
Internal RC Oscillator	-	-	X	Х	X
Oscillator Amplifier	Х	Х	-	-	X
PB3 as General I/O	-	-	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾
PB4 as General I/O	-	•	X	X	X ⁽²⁾
Start-up Time	1 ms 16 ms	1 ms 16 ms	16 µs	16 µs	14 CK 14 CK + 4 ms 14 CK + 64 ms
Supply Voltage, Min	4.0 V	2.7 V	4.0 V	2.7 V	1.8 V
Supply Voltage, Max	6.0 V	6.0 V	6.0 V	6.0 V	5.5 V

Notes:

- 1. When using internal oscillator.
- 2. When using internal oscillator or external clock source.

3 Memories

EEPROM write access times of AT90S/LS23x3 depend on the supply voltage of the device, while in ATtiny25 the access times are constant. This means that at high supply voltages the EEPROM of ATtiny25 may take more time to program than AT90S/LS23x3, while at lower supply voltages the ATtiny25 operation is faster. Write access times for the devices are listed in Table 3-1.

Table 3-1. EEPROM Programming Times.

Condition	Programming Times, Typical		
Condition	AT90S/LS23x3	ATtiny25	
Vcc = 5.0 V	2.5 ms	3.4 ms (Atomic Operation: Erase & Write)	
VCC = 5.0 V	2.5 1115	1.8 ms (Write, Only)	
Vcc = 2.7 V 4.0 ms		3.4 ms (Atomic Operation: Erase & Write)	
VCC = 2.7 V	4.0 1115	1.8 ms (Write, Only)	

In ATtiny25 it is possible to split the EEPROM program operation into atomic operations of erase and write. The default is to perform erase and write in the same operation. Alternatively, the EEPROM locations of ATtiny25 may be erased during initialization and a fast write operation can be performed at time critical instances. See EEPROM Control Register of ATtiny25 for more details.

4 System Clock and Clock Options

ATtiny25 has a more advanced clock system than AT90S/LS23x3 devices. AT90S/LS2323 can use external crystals, external resonators and external clock signals. In addition, AT90S/LS2343 can use its internal RC oscillator running at 1 MHz. ATtiny25 provides the same features but also a wider range of clock sources, frequencies and options.

Table 4-1shows how to configure ATtiny25 to match the clock source and settings of AT90S/LS23x3 devices. Additional information regarding the clock system settings is found in Table 5-1 on page 4.

Table 4-1. Clock System Migration.

AT90S/LS23x3 Clock System		ATtiny25 F	use Bits
Source Setting		CKSEL31	CKDIV8
Ceramic Resonator	f < 0.9 MHz	100	
	f < 3 MHz	101	
Crystal or Resonator	f = 38 MHz	110	1
	f > 8 MHz	111	
External Clock Signal	Any	000	
Internal RC Oscillator	f = 1 MHz	001	0





5 System Control and Reset

Start-up times are not the same for ATtiny25 and AT90S/LS23x3 devices.

5.1 Start-up Times

Table 5-1 shows how to program fuses CKSEL0 and SUT to get the closest match between the start-up time of ATtiny25 and AT90S/LS23x3.

Table 5-1. Configuring ATtinv25 for Similar Start-up Times (SUT) as AT90S/LS2323.

AT90S/LS23x3 Settings			ATtiny25 Closest Match(es)				
Device	FSTRT	WDT Cycles	Vcc	SUT	CKSEL0	SUT10	SUT
			F 0 \/	1 ma	1	01	14 CK
	0 (1)	1024	5.0 V	1 ms	1	10	14 CK + 4.1 ms
AT000// 00000		3.0 V	3 ms	1	10	14 CK + 4.1 ms	
AT90S/LS2323			5.0 V	5.0 V 16 ms	1	10	14 CK + 4.1 ms
	1	16384			1	11	14 CK + 65 ms
		3.0 V	47 ms	1	11	14 CK + 65 ms	
AT90S/LS2343	N/a (2)	1	Any	16 µs	1	01	14 CK

Notes:

5.2 Power-On Reset

The threshold levels of power-on reset are not identical for AT90S/LS23x3 and ATtiny25.

Please see device data sheets for more detailed information.

5.3 External Reset

Reset characteristics of AT90S/LS23x3 and ATtiny25 differ slightly. The minimum pulse width required on the reset pin to trigger a device reset is typically longer on the ATtiny25. This means a very narrow pulse (spike) on the reset input pin may trigger a device reset on AT90S/LS23x3 but not necessarily on the ATtiny25.

Please see device data sheets for more detailed information.

5.4 Watchdog Reset

In the MCU Status Register (MCUSR) of AT90S/LS23x3 there is no flag to signal a Watchdog reset and this event is hence typically identified by means of exclusion; a Watchdog reset is assumed if all other reset flags are low. In ATtiny25 this does not necessarily work, since an additional source of reset is present; the Brown-Out Reset. The Watchdog Reset Flag (WDRF) of the MCU Status Register (MCUSR) in ATtiny25 should be used to properly identify a Watchdog Reset event.

^{1. &}quot;0" means programmed, "1" is unprogrammed.

^{2.} Fuse not available in AT90S/LS2343.

5.5 Watchdog Timer

In AT90S/LS23x3 the watchdog timer is clocked from a 1 MHz oscillator, which has a frequency that strongly depends on supply voltage. In ATtiny25 the oscillator runs at 128 kHz and has a more stable frequency characteristic.

For a given set of WDP2...0 bits and at 5.0 V supply voltage both devices will have nearly equal time-out periods. At lower supply voltages the time-out period will have to be adjusted.

Please see data sheet for characteristic data on watchdog oscillator.

6 Register Names and Bit Definitions

There are some minor changes in register and bit naming conventions between AT90S/LS23x3 and ATtiny25.

6.1 Renamed Registers

Table 6-1 lists the registers, which have been renamed, but still exist at the same physical address and have maintained their functionality. It is only required to update the register name in the application.

Table 6-1. Changes to Register Names.

Address [hex]	Name in AT90S/LS23x3	Name in ATtiny25
\$33	TCCR0	TCCR0B
\$1E	EEAR	EEARL

6.2 Renamed Bits

Table 6-2 lists the bits that have been renamed, but still exist in the same register and in the same register location.

Table 6-2. Changes to Bit Names.

TUBIO O EL CI	idingoo to Bit it	amoon		
AT90S/LS23	к3		ATtiny25	
Bit Name	Register	Address	Bit Name	
SM	MCUCR	\$35	SM1	
WDTOE	WDTCR	\$21	WDCE	
EEMWE	EECR	\$1C	EEMPE	
EEWE	EECR	\$1C	EEPE	

7 Interrupt Vectors

ATtiny25 has more interrupt vectors than AT90S/LS23x3, but all AT90S/LS23x3 vectors are present in ATtiny25. Note however that the vector address for the timer/counter (T/C0) interrupt has been moved. Please refer to Table 7-1.

Table 7-1. Changes to Interrupt Vectors.

Vector Number	AT90S/LS23x3	ATtiny25		
vector Number	Vector Name	Address	Vector Name	Address
3	TIMER0_OVF	0x0002	TIM0_OVF	0x0005





Programs using only the RESET and INTO vectors can still use the end of AT90S/LS23x3 interrupt vector table as a starting address on ATtiny25, provided that ATtiny25 specific interrupts are not enabled. The starting address of the program may have to be changed if timer/counter overflow vector is used, since this resides in a different location in ATtiny25.

8 Pin Compatibility

AT90S/LS23x3 and ATtiny25 are fully pin compatible, but note that INT0 on pin 6 in AT90S/LS23x3 is moved to pin 7 in ATtiny25. The external interrupt connected to pin 6 on ATtiny25 is called PCINT1 and can be used as a replacement for INT0 on AT90S/LS23x3. Refer to datasheet for details.

9 I/O Ports

Port drivers of AT90S/LS23x3 have a higher current sink rating but a lower current source rating than those of ATtiny25. This means that applications where high current is sunk via I/O pins may exceed ATtiny25 device limits. Applications where I/O pins are used for sourcing current are not affected.

Port driver characteristics are outlined in Table 9-1.

Table 9-1. Changes to Interrupt Vectors.

Condition	Port Pin	Pin Rating [mA]		
Condition	FOICEIII	AT90S/LS23x3	ATtiny25	
Current Sink	PB0:2 + PB3:4 ⁽¹⁾	20	10	
Current Source	PB0:2 + PB3:4 ⁽¹⁾	3	10	

Notes:

1. PB3:4 available as I/O in AT90S2343 and AT90LS2343, only.

10 Memory Programming

Both the In System and High Voltage programming interface and algorithms have changed. Refer to the datasheets for details. The most recent version of AVR Studio automatically supports any updates in memory programming algorithms in all programming tools provided by Atmel.

10.1 Fuse Bits

The number of fuse bits has been increased to three bytes in ATtiny25. Read and write algorithms must be updated for proper fuse programming. If using Atmel programming tools, these are automatically updated when installing a new version of AVR Studio.

10.2 Signature Bytes

Signature bytes reside in a separate address space and can only be read external to the device. Therefore, this notion only applies to programming tools used, and not to the actual program being migrated.

Signature bytes have been updated as listed in Table 10-1.

Table 10-1. Summary of Signature Bytes.

Byte	AT90S/LS2323	AT90S/LS2343	ATtiny25
\$000	\$1E	\$1E	\$1E
\$001	\$91	\$91	\$91
\$002	\$02	\$03	\$08

10.3 Low-Voltage Serial Programming

In AT90S/LS23x3 the low-voltage serial programming algorithm writes Flash and EEPROM one byte at a time. In ATtiny25 the low-voltage serial programming algorithm programs Flash memory one page at a time. Please see the data sheet for more details.

The minimum wait delay after a chip erase or before the next EEPROM or Flash location can be written is approximately equal between ATtiny25 and AT90S/LS23x3, when supply voltage Vcc = 5.0 V. The delay is typically shorter on ATtiny25 for supply voltages below 5 V.

All algorithm updates (above and below) are included in AVR Studio, but customized programming software may have to be modified.

10.3.1 Data Polling of EEPROM

Data polling can be used to detect when the device is ready to program the next byte. In AT90S/LS23x3 polling the EEPROM will first return 0x00, then 0xFF (when autoerase is complete) and then the programmed data (when programming of the byte is complete). In ATtiny25 the EEPROM will always return 0xFF, until programming of the byte is complete.

10.3.2 Data Polling of Flash

In AT90S/LS23x3 data is programmed byte-wise, while in ATtiny25 data is programmed one page at a time. Data polling in ATtiny25 can be performed on any byte within the page being programmed.

10.4 High-Voltage Serial Programming

The recommended algorithm for high-voltage serial programming has been updated. There are also minor changes to timing requirements.

Please data sheet for more details.

11 Electrical Characteristics

ATtiny25 is manufactured using a different process then AT90S/LS23x3 and electrical characteristics will therefore differ between these devices. Major differences are listed below.

- Maximum operating voltage (absolute maximum rating) is lower on ATtiny25.
- Input low voltage is typically lower on ATtiny25.
- Input leakage current of I/O pins is lower on ATtiny25.
- Reset pull-up resistor has higher impedance on ATtiny25.
- I/O pin pull-up resistor typically has lower impedance on ATtiny25.

Please consult data sheets for details on electrical characteristics.





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