

PIC16(L)F1768/1769 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1768/1769 family devices that you have received conform functionally to the current Device Data Sheet (DS40001775C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC16(L)F1768/1769 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select Programmer > Reconnect.
 - b) For MPLAB X IDE, select Window > Dashboard and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Revision ID values for the various PIC16(L)F1768/1769 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾	
		A2	A3
PIC16F1768	3084h	2002h	
PIC16LF1768	3086h	2002h	
PIC16F1769	3085h	2002h	2003h
PIC16LF1769	3087h	2002h	2003h

Note 1: The Device and Revision IDs are located at the respective addresses 8006h and 8005h of configuration memory space.

2: Refer to the “*PIC16(L)F176X Memory Programming Specification*” (DS40001754) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A2	A3
16-Bit Pulse-Width Modulation (PWM)	Continuous Slave mode	1.1	Anomalous behavior.	X	X
Programmable Ramp Generator (PRG)	Ramp Capacitor	2.1	Shorting switch fails to stay closed.	X	
Programmable Ramp Generator (PRG)	Low Range	2.2	Low range missing.	X	
ECCP	Compare mode	3.2	Compare Toggle mode yields unexpected results.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A2).

1. Module: 16-Bit Pulse-Width Modulation (PWM)

1.1 Continuous Slave Mode Anomaly

The 16-bit PWM in continuous Slave mode (PWMxOFCON<6:5> = 11) may get stuck in anomalous behavior. The behavior is that the slave PWM output will toggle when the master PWM matches the master PWM offset value, then toggle again on the next master offset match event. The slave PWM output will then remain steady for the number of master periods equal to the slave PWM period value after which the sequence repeats. The slave PWM may occasionally start to operate as described by either writing the slave PWMxOFCON register or enabling the slave PWM from an Idle state.

Work around

None.

Affected Silicon Revisions

A2	A3						
X	X						

2. Module: Programmable Ramp Generator (PRG)

2.1 Ramp Capacitor Shorting Switch Fails to Stay Closed

When the PRG GO bit is zero or when the rising or falling ramp is in the Reset state for an extended period of time, then the ramp capacitor shorting switch will improperly open, causing the PRG output to drift from the reference voltage input level.

Work around

None.

Affected Silicon Revisions

A2	A3						
X							

2.2 Low Range Missing

The LR bit is missing from the PRGxCON2 register, and the extended low slope capability is not available.

Work around

None.

Affected Silicon Revisions

A2	A3						
X							

3. Module: ECCP

3.2 Compare Mode

The ECCP Compare Toggle modes (CCPxCON<3:0> bits = 0010 or 0001) work properly as long as the Timer1 prescaler value is configured to 1:1. When the Timer1 prescaler value is configured to any other value, the ECCP Compare output yields unexpected results.

Work around

Method 1:

Only use the Compare Toggle mode when the Timer1 prescaler value is set to 1:1.

Method 2:

Use CCP Compare mode with pulse output (CCPxCON<3:0> bits = 1011) to clock a CLC configured as a J-K flip-flop in Toggle mode.

Affected Silicon Revisions

A2	A3						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001775C):

Note: Corrections are shown in bold . Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2015)

Initial release of this document; issued for revision A2. Includes silicon issues 1.1 (EUSART), 2.1 to 2.3 (MSSP) and 3.1 (16-Bit PWM).

Rev B Document (01/2016)

Removed Modules 1 and 2; Added new Module 2, Programmable Ramp Generator and Module 3, ECCP; Other minor corrections.

Rev C Document (01/2018)

Added new Module 2.2: Low Range Missing (on PRG).

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