Single-Edge Nibble Transmission (SENT) Module

HIGHLIGHTS

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1.0 INTRODUCTION

SENT is a unidirectional, single-wire communications protocol that is based on SAE J2716, *"SENT – Single-Edge Nibble Transmission for Automotive Applications"*. The protocol is designed for point-to-point transmission of signal values, using a signal system based on successive falling edges. It allows for high-resolution data transmission with a lower system cost than available serial data solutions, and is intended for use in applications where data needs to be communicated from a sensor to a central controller, such as an Engine Control Unit (ECU).

The 16-bit SENT module is a dedicated hardware implementation of SAE J2716. The module can be configured for three main modes of operation:

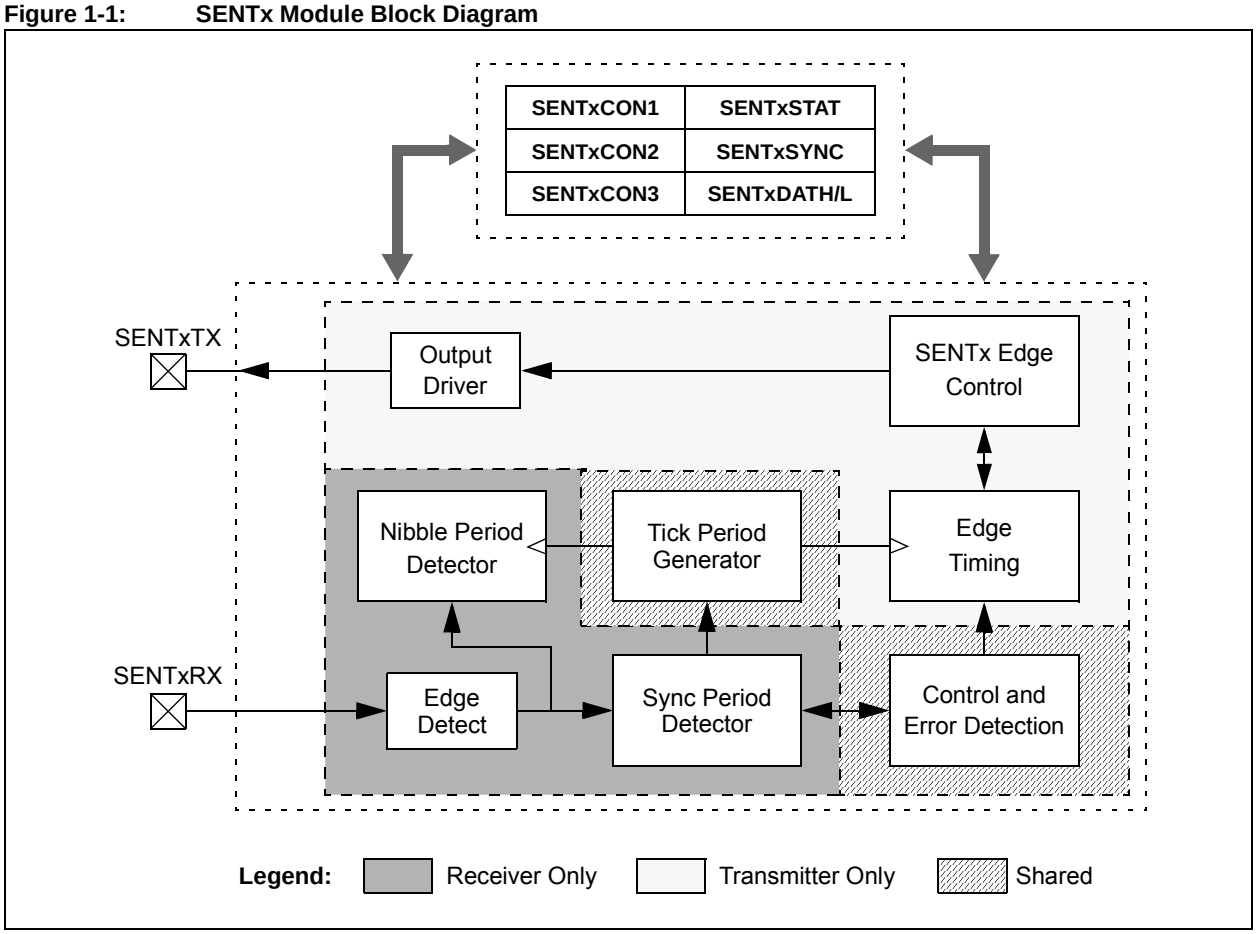
- Asynchronous transmitter (default)
- Synchronous transmitter
- Receiver

The module also includes these features:

- Automatic data rate synchronization
- Optional automatic detection of CRC errors in Receive mode
- Optional hardware calculation of CRC in Transmit mode
- Support for optional Pause Pulse period
- Data buffering for one message frame
- Selectable data length for transmit/receive from 3 to 6 nibbles
- Automatic detection of framing errors
- Separately mappable input and output functions on devices with Peripheral Pin Select (PPS)

An overview of the SENT module is shown in Figure 1-1.

Figure 1-1: SENTx Module Block Diagram



2.0 REGISTERS

Each implementation of the SENT module has the following registers, where 'x' denotes the number of the module:

- SENTxCON1: Configuration and Setup Control
- SENTxCON2: Contains TICKTIME<15:0> bits in Transmit mode or SYNCMAX<15:0> bits in Receive mode
- SENTxCON3: Contains FRAMETIME<15:0> bits in Transmit mode or SYNCMIN<15:0> bits in Receive mode
- SENTxSTAT: Status Information
- SENTxSYNC: Captured Sync Time when in Receive mode
- SENTxDATH/L: Message Frame Nibble Data

2.1 Control Registers

The SENTxCON1 register (Register 2-1) controls most functions of the module, including Transmit/Receive mode selection, data length, transmit polarity and CRC checksum calculation. The module is enabled by setting the SNTEN bit (SENTxCON1<15>).

The SENTxSTAT register (Register 2-2) shows the status of operations in both Transmit and Receive modes. All bits are read-only, with the exception of SYNCTXEN (SENTxSTAT<0>), which may be used in Synchronous Transmit mode to trigger a data transmission.

2.2 Control Registers (Data Values Only)

Two registers are used to store data values that are central to the module's operation. They do not contain individual control bits. Their use is more completely described in **Section 4.0 "Transmit Mode"** and **Section 5.0 "Receive Mode"**.

The SENTxCON2 register is a 16-bit readable and writable register. It stores the 16-bit value for TICKTIME<15:0>, the period of the Tick Clock Generator in Transmit modes. In Receive mode, it stores the 16-bit value for SYNCMAX<15:0>, the maximum time interval for a valid Sync period.

The SENTxCON3 register is also a 16-bit readable and writable register. In Transmit modes, it stores the 16-bit value of FRAMETIME<15:0>, the total number of Ticks for a data frame when the Pause Pulse is used. In Receive mode, it stores the 16-bit value for SYNCMIN<15:0>, the minimum time interval for a valid Sync period.

2.3 Data Registers

The SENTxSYNC register is a 16-bit readable and writable register. It is used to capture the length of the synchronization time period during Transmit modes.

SYNCxDATH and SYNCxDATL are 16-bit, readable and writable registers, that are used to store transmitted and received data. Data is stored in the registers as packed nibbles, with four nibbles per register, as described in Table 2-1.

Table 2-1: Packing of Message Nibbles in SENTxDATH/L Registers

SENTxDATH		SENTxDATL	
Bit Range	**Contents**	**Bit Range**	**Contents**
<15:12>	Status Nibble	<15:12>	Data Nibble 4
<11:8>	Data Nibble 1	<11:8>	Data Nibble 5
<7:4>	Data Nibble 2	<7:4>	Data Nibble 6
<3:0>	Data Nibble 3	<3:0>	CRC Nibble

Register 2-1: SENTxCON1: SENTx Control Register 1

R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SNTEN	—	SNTSIDL	—	RCVEN	TXM(1)	TXPOL(1)	CRCEN
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-1	R/W-1	R/W-0
PPP	SPCEN(2)	—	PS	—	NIBCNT2	NIBCNT1	NIBCNT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **SNTEN:** SENTx Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SNTSIDL:** SENTx Stop In Idle bit
1 = Module stops operation in Idle mode
0 = Module continues operation in Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **RCVEN:** SENTx Receive Enable bit
1 = Module operates as a receiver
0 = Module operates as a transmitter

bit 10 **TXM:** SENTx Transmit Mode bit(1)
1 = Module transmits data frame only when triggered using the SYNCTXEN status bit
0 = Module transmits data frames continuously while enabled

bit 9 **TXPOL:** SENTx Transmit Polarity bit(1)
1 = Idle state of data output pin is low
0 = Idle state of data output pin is high

bit 8 **CRCEN:** CRC Enable bit
In Receive Mode (RCVEN = 1):
1 = CRC verification is performed using the J2716 method
0 = CRC verification is not performed
In Transmit Mode (RCVEN = 0):
1 = CRC is calculated using the J2716 method
0 = CRC is not calculated

bit 7 **PPP:** Pause Pulse Present bit
1 = SENTx messages transmitted/received with Pause Pulse
0 = SENTx messages transmitted/received without Pause Pulse

bit 6 **SPCEN:** Short PWM Code Enable bit(2)
1 = SPC control from external source is enabled
0 = SPC control from external source is disabled

bit 5 **Unimplemented:** Read as 'SENTx'

bit 4 **PS:** Prescale Select bit
1 = 1:4 (Module clock is TCY/4)
0 = 1:1 (Module clock is TCY)

Note 1: These bits have no function when RCVEN = 1.
2: This bit has no function when RCVEN = 0.

Register 2-1: SENTxCON1: SENTx Control Register 1 (Continued)

bit 3 **Unimplemented:** Read as 'SENTx'

bit 2-0 **NIBCNT<2:0>:** Nibble Count Control bits

111 = Reserved; do not use
110 = 6 data nibbles per data packet
101 = 5 data nibbles per data packet
100 = 4 data nibbles per data packet
011 = 3 data nibbles per data packet
010 = 2 data nibbles per data packet
001 = 1 data nibble per data packet
000 = Reserved; do not use

Note 1: These bits have no function when RCVEN = 1.

2: This bit has no function when RCVEN = 0.

Register 2-2: SENTxSTAT: SENTx Module Status Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R-0	R-0	R-0	R/C-0	R/C-0	R-0	R/W-0, HC(1)
PAUSE	NIB2	NIB1	NIB0	CRCERR	FRMERR	RXIDLE	SYNCTXEN
bit 7							bit 0

Legend:	C = Clearable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **PAUSE:** Pause Period Status bit
1 = The module is transmitting/receiving a Pause period
0 = The module is not transmitting/receiving a Pause period

bit 6-4 **NIB<2:0>:** Nibble Status bits
In Transmit Mode (RCVEN = 0):
111 = Module is transmitting CRC nibble
110 = Module is transmitting Data Nibble 6
101 = Module is transmitting Data Nibble 5
100 = Module is transmitting data nibble 4
011 = Module is transmitting Data Nibble 3
010 = Module is transmitting data Nibble 2
001 = Module is transmitting Data Nibble 1
000 = Module is transmitting status nibble or Pause period, or is not transmitting
In Receive Mode (RCVEN = 1):
111 = Module is receiving CRC nibble or was receiving this nibble when an error occurred
110 = Module is receiving Data Nibble 6 or was receiving this nibble when an error occurred
101 = Module is receiving Data Nibble 5 or was receiving this nibble when an error occurred
100 = Module is receiving Data Nibble 4 or was receiving this nibble when an error occurred
011 = Module is receiving Data Nibble 3 or was receiving this nibble when an error occurred
010 = Module is receiving Data Nibble 2 or was receiving this nibble when an error occurred
001 = Module is receiving Data Nibble 1 or was receiving this nibble when an error occurred
000 = Module is receiving Status nibble or waiting for Sync

bit 3 **CRCERR:** CRC Status bit (Receive mode only)
1 = A CRC error occurred for the data nibbles in SENTxDATH/L
0 = No CRC error has occurred

bit 2 **FRMERR:** Framing Error Status bit (Receive mode only)
1 = A data nibble was received with less than 12 Tick periods or greater than 27 Tick periods
0 = No framing error has occurred

bit 1 **RXIDLE:** Receiver Idle Status bit (Receive mode only)
1 = The SENTx data bus has been Idle (high) for a period of SYNCMAX or greater
0 = The SENTx data bus is not Idle

Note 1: This bit is read-only in Receive mode and writable (settable and clearable) in Transmit mode.

Register 2-2: SENTxSTAT: SENTx Module Status Register (Continued)

bit 0 **SYNCTXEN:** Synchronization Period Status/Transmit Enable bit(1)

In Receive Mode (RCVEN = 1):
1 = A valid synchronization period was detected, the module is receiving nibble data
0 = No synchronization period has been detected, the module is not receiving nibble data

In Synchronous Transmit Mode (RCVEN = 0, TXM = 1):
1 = The module is transmitting a SENT data frame
0 = The module is not transmitting a data frame; software may set SYNCTXEN to start another data frame transmission

In Asynchronous Transmit Mode (RCVEN = 0, TXM = 0):
SYNCTXEN always reads as '1', indicating the module is transmitting frames continuously.

Note 1: This bit is read-only in Receive mode and writable (settable and clearable) in Transmit mode.

3.0 PROTOCOL OVERVIEW

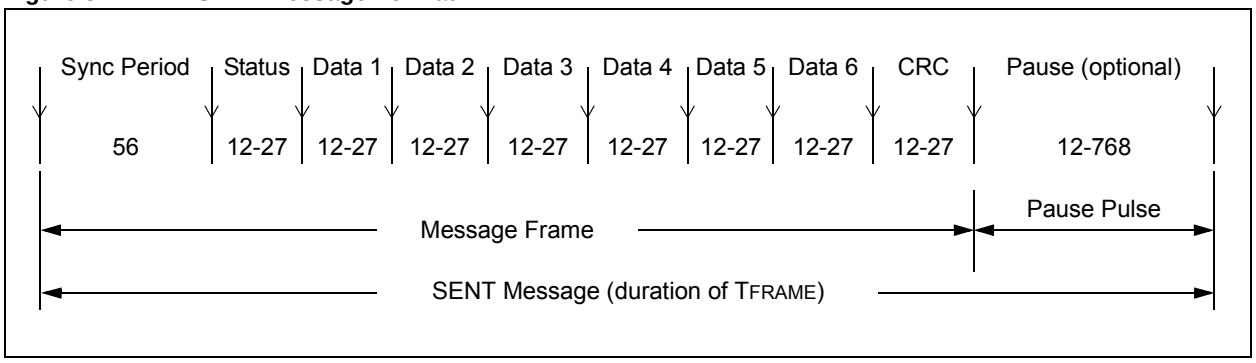
SENT messages are encoded and decoded based on the time between falling edges. The protocol's timing is based on a predetermined time unit, TTICK, which can vary from 3 to 90 µs. Both the transmitter and receiver must be preconfigured for the same value of TTICK. The SENT specification allows messages to be validated with up to a 20% variation in TTICK. This allows for the transmitter and receiver to run from different clocks that may be inaccurate, and drift with time and temperature.

A SENT message consists of the following:

- A Synchronization/Calibration Period ("pulse") of 56 Tick Times
- A Status Nibble of 12 to 27 Tick Times
- Up to Six Data Nibbles of 12 to 27 Tick Times
- A CRC Nibble of 12 to 27 Tick Times
- An Optional Pause Pulse Period of 12 to 768 Tick Times

The period from the start of the Sync period to the end of the CRC nibble comprises the message frame. When the optional Pause period is present, this makes one SENT message with a length of TFRAME (generally expressed in µs). Figure 3-1 shows the construction of a typical 6-nibble data frame, with the numbers representing the minimum or maximum number of Tick times for each section.

Figure 3-1: SENT Message Format



The Sync period starts the message frame, and is used for synchronization of TTICK between the transmitter and receiver. When configured for Transmit mode, the module drives the line low for 5 Ticks and to a high-impedance state for 51 Ticks.

A four-bit status nibble follows the Sync pulse and may be used for device status, identification, or alternatively, used as additional data. The status nibble is formatted the same as a data nibble.

After the status nibble is one or more (up to six) data nibbles. These are 4 bits in length and are encoded as the data value plus 12 Ticks. This yields a minimum value of 12 Ticks for 0h and a maximum value of 27 Ticks for Fh. When configured for Transmit mode, the module drives the line low for 5 Ticks and into a high-impedance state for the remaining 7 to 22 Ticks.

The CRC data nibble follows the data payload. This is a 4-bit CRC of the six data nibbles only. The CRC is calculated using a polynomial of, $x^4 + x^3 + x^2 + 1$, with a seed value of '0101'. It is then padded with '0' to help detect shift errors. The CRC nibble is formatted the same as a data nibble.

Since the data values are encoded in the time between falling edges, the SENT protocol may produce a variable length message. In some applications, the Pause Pulse period is used to pad the message length so that messages will always be received at a constant time interval. The module provides support to automatically calculate the Pause duration needed for periodic transmissions. When configured for Transmit mode, the module drives the line low for 5 Ticks and into a high-impedance state for the remaining Pause time.

Note: A SENT message frame will always have a status and CRC nibble. The shortest message frame with one data nibble (SENTxCON1<2:0> = 001) will have a length of one Sync and three nibbles.

3.1 Short and Enhanced Serial Message Formats

The J2716 specification defines two optional message formats: a Short Serial Message format and an Enhanced Serial Message format. Both of these message formats encode a longer serial message using two bits of the status nibble. A single message is encoded using multiple SENT data frames.

If the module is configured as a transmitter, the application must encode these serial messages by writing the appropriate value. If the module is configured as a receiver, the application must decode these serial messages by storing and analyzing the contents of the received status nibbles.

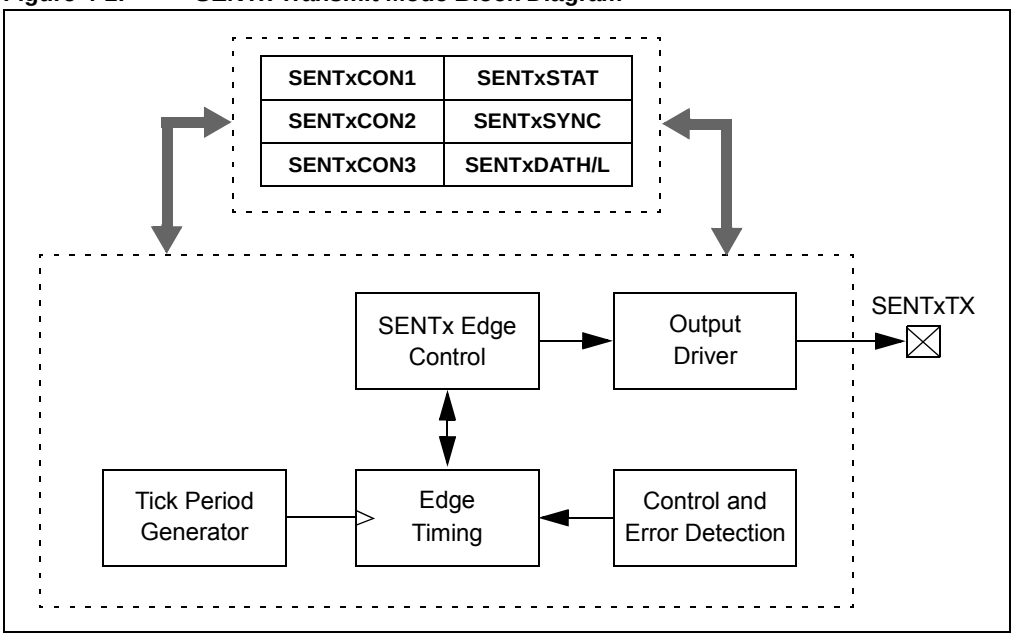
4.0 TRANSMIT MODE

When RCVEN (SENTxCON1<11>) = 0, the module operates as a transmitter. Message frames are generated using the Configuration and Data registers.

The module has two transmit operating modes selected by the TXM bit (SENTxCON1<10>). Asynchronous mode (TXM = 0) continuously sends data message frames when the SNTEN bit (SENTxCON1<15>) is set. Synchronous mode (TXM = 1) sends messages under software control to support additional capabilities, including Short PWM Code (SPC).

A block diagram of Transmit mode is shown in Figure 4-1.

Figure 4-1: SENTx Transmit Mode Block Diagram



4.1 Timing Calculations for Transmit Mode

In Transmit mode, SENTxCON2 and SENTxCON3 hold the values for TICKTIME<15:0> and FRAMETIME<15:0>. The Tick period used by the SENT transmitter (TTICK) is set by writing TICKTIME to the SENTxCON2 register. The Tick period calculations are shown in Equation 4-1. The FCLK value is either FCY or FCY/4, depending on the value of the Prescaler Enable bit, PS (SENTxCON1<4>).

Equation 4-1: Tick Period Calculation

$$TICKTIME = (T_{TICK} \bullet F_{CLK}) - 1$$

Where:

$$F_{CLK} = F_{CY}/Prescaler$$

If the Pause Pulse is to be used, a frame period (TFRAME) must be defined. This is done by writing the value of FRAMETIME<15:0> to SENTxCON3. The formulas used to calculate the value of FRAMETIME (in the same units as TTICK) are shown in Equation 4-2. The FRAMETIME ranges for all settings are summarized in Table 4-1.

Equation 4-2: Calculating TFRAME

$$\text{FRAMETIME} = T_{FRAME}\ (\mu s)/T_{TICK}$$

Where:

$$848 + 12N \geq \text{FRAMETIME} \geq 122 + 27N, \text{ for } 1 \leq N \leq 6$$

Table 4-1: Range of FRAMETIME<15:0> Values

Number of Data Nibbles	Min. FRAMETIME<15:0> Value	Max. FRAMETIME<15:0> Value
1	149	860
2	176	872
3	203	884
4	230	896
5	257	908
6	284	920

4.2 CRC Calculation

The module can optionally calculate the CRC using the recommended method shown in Example 4-1. The CRC is calculated when the CRCEN bit (SENTxCON1<8>) is set and the CRC (SENTxDATAL<3:0>) register bits become read-only. The hardware computed CRC value is indicated in the CRC<3:0> register bits when the calculation is finished.

When CRCEN = 0, no CRC is computed in hardware and the CRC<3:0> bits become writable by software. The application must compute a CRC value and write it to CRC<3:0>.

Example 4-1: Recommended J2716 CRC Implementation

```
#define NUM_NIBBLES  6
// Array holding received nibbles
rec_data[NUM_NIBBLES];
// CRC lookup table
crc_table = {0,13,7,10,14,3,9,4,1,12,6,11,15,2,8,5};
// Initialize checksum to seed value
Checksum = 5;
// For each data nibble, bit-wise XOR with lookup value from table
for(i=0;i<NUM_NIBBLES;i++)
{
    Checksum = rec_data[i] ^ crc_table[Checksum];
}
// Bit-wise XOR with additional 0 value
Checksum = 0 ^ crc_table[Checksum];
```

4.3 Transmitter Status Bits

The SENTxSTAT register provides status information and control when in Transmit mode. The NIB<2:0> status bits (SENTxSTAT<6:4>) display the current data nibble transmitting during a message frame. If the Pause period is enabled (PPP (SENTxCON1<7>) = 1), the PAUSE bit (SENTxSTAT<7>) indicates when a Pause period transmission is in progress.

The SYNCTXEN bit (SENTxSTAT<0>) is used to initiate a synchronous transmission when TXM is set. SYNCTXEN is automatically cleared by hardware when all data nibbles, the CRC nibble and the Pause period have completed.

4.4 Transmit Polarity Option

The polarity of the SENT data pin can be inverted by setting the TXPOL bit (SENTxCON1<9>). This feature can be useful for implementing an external transistor drive circuit. Note that the high-impedance (Idle) condition on the line remains in the same state (high) due to the external pull-up resistor network.

4.5 Transmit Output Pin and PPS

On devices with Peripheral Pin Select (PPS), the SENTx Transmit pin function (SENTxTX) is a remappable feature. To use the module in Transmit mode, SENTxTX must be mapped to an available I/O pin using the appropriate RPORx register. Refer to the device data sheet for specific information.

4.6 Asynchronous Transmitter Mode

The module is, by default, configured as an asynchronous transmitter. In this mode, the module continuously transmits message frames as long as the SNTEN bit is set (SENTxCON1<15>). The final falling edge of the CRC nibble also serves as the first falling edge of the Sync pulse. An interrupt is generated at the completion of the CRC nibble.

Figure 4-2 and Figure 4-3 show the relationship between the control, status and interrupt events.

Figure 4-2: SENTx Data Transmission, Asynchronous Mode

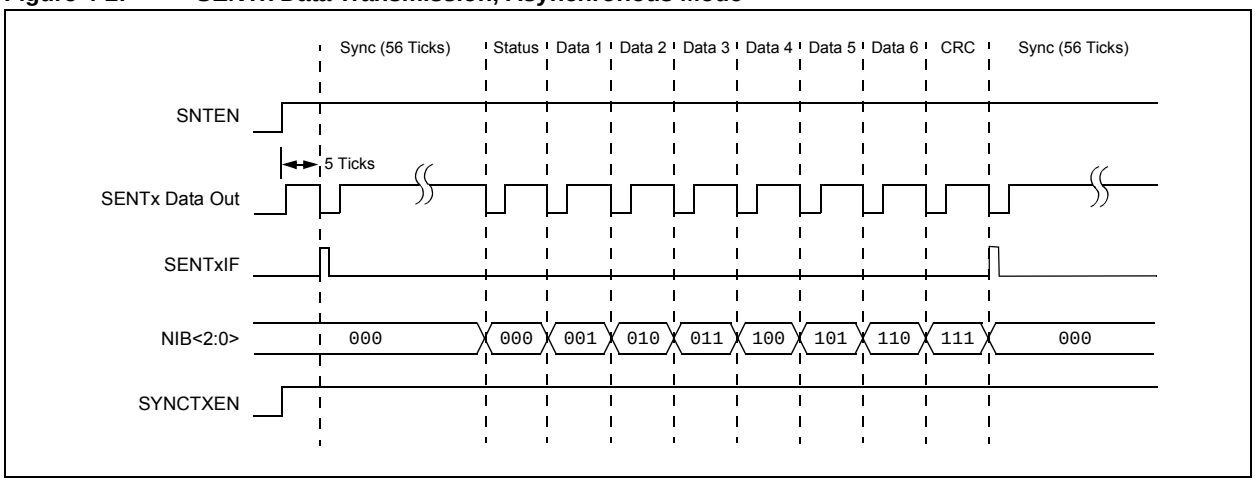
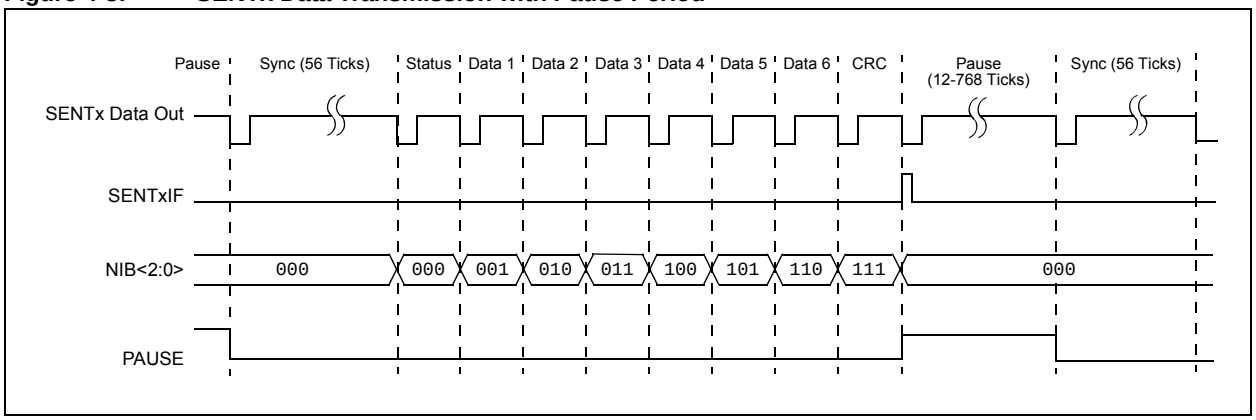


Figure 4-3: SENTx Data Transmission with Pause Period



To fully configure the module, the following must be known:

- Tick Time, TTICK (Equation 4-1)
- Number of Data Nibbles, N
- Hardware or Application Calculated CRC
- Use of Pause Period for Fixed Message Period
- The Overall Duration of the SENT Message if the Pause Period is Present (Equation 4-2)

To initialize the module:

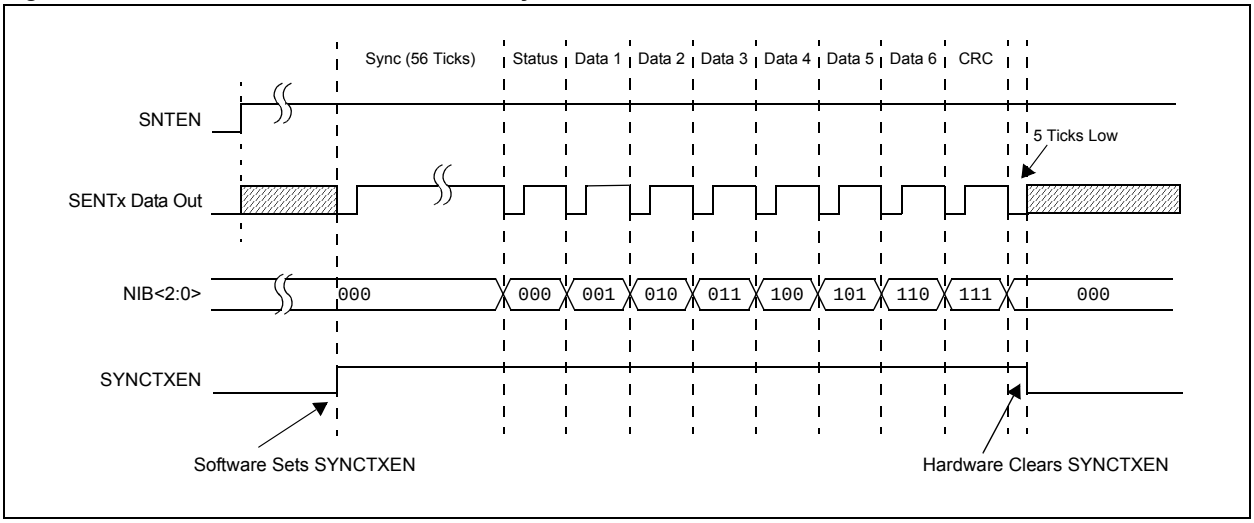
1. Clear RCVEN (SENTxCON1<11>) for Transmit mode.
2. Clear TXM (SENTxCON1<10>) for asynchronous transmit.
3. Write the value of the desired frame length to NIBCNT<2:0> (SENTxCON1<2:0>).
4. Set or clear CRCEN (SENTxCON1<8>) to configure the module for hardware or software CRC calculation.
5. Write the value for the desired TICKTIME to SENTxCON2.
6. If the optional Pause period is required, set PPP (SENTxCON1<7>) to enable the feature, then write the value of FRAMETIME to SENTxCON3.
7. Enable the SENT interrupt(s) and set the interrupt priority.
8. Write the initial status and data values to SENTxDATH/L. If application-based CRC is being used (CRCEN = 0), also calculate the message CRC and write it to CRC<3:0>.
9. Set SNTEN (SENTxCON1<15>) to enable the module.

Updates to SENTxDATH/L must be performed after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt to trigger data writes

4.7 Synchronous Transmitter Mode

The module can be alternatively configured as a synchronous transmitter. In this mode, the module will transmit only one message frame each time the SYNCTXEN bit (SENTxSTAT<0>) is set. When the data frame is complete the SYNCTXEN bit will be cleared in hardware. The line will be driven low for 5 Ticks to complete the CRC nibble and then the line will tri-state and remain in the Idle state until SYNCTXEN is set again. An interrupt is generated, 5 Ticks after the completion of the CRC nibble. Figure 4-4 shows the relationship between the control, status and interrupt events.

Figure 4-4: SENTx Data Transmission, Synchronous Mode



To fully configure the module, the following must be known:

- Tick Time, TTICK (Equation 4-1)
- Number of Data Nibbles
- Hardware or Application Calculated CRC

To initialize the module for synchronous transmission:

1. Clear the RCVEN bit (SENTxCON1<11>) for Transmit mode.
2. Set the TXM bit (SENTxCON1<10>) for synchronous transmit operation.
3. Write the desired data frame length to NIBCNT<2:0> (SENTxCON1<2:0>).
4. Set or clear CRCEN (SENTxCON1<8>) to configure the module for hardware or software CRC calculation.
5. Write the desired value for TICKTIME to SENTxCON2.
6. Enable the SENT interrupts and set the interrupt priority.
7. Set the SNTEN bit (SENTxCON1<15>) to enable module.

When the application is ready to transmit data:

1. Write the data to be transmitted to the SENTxDATH/L registers.
2. Set the SYNCTXEN bit to begin transmission.

Updates to SENTxDATH/L must be performed after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt or poll the SYNCTXEN bit.

Note:	Software may need to wait additional time before starting a new message frame. The J2716 specification allows up to 18 µs of rise time on the SENT data line. The rise time will be a function of the external pull-up resistor and EMI filtering on the SENT data line. It is recommended that the wait time be longer than one Sync time of 56 Ticks + 20%.

4.7.1 SHORT PWM CODE (SPC) SUPPORT

Short PWM Code can be implemented with user software using Synchronous mode. SPC allows bidirectional communication, such as allowing the receiver to request a message frame from the transmitter, changing modes or to calibrate a sensor.

The SPC pulse is an active-low pulse initiated by the receiver. Since the module does not provide hardware functionality for the detection of SPC pulses, the application will need to detect the SPC pulses on the SENT data pin.

When the transmitter is Idle, user software can use one of these methods to detect a SPC pulse on the SENT data pin:

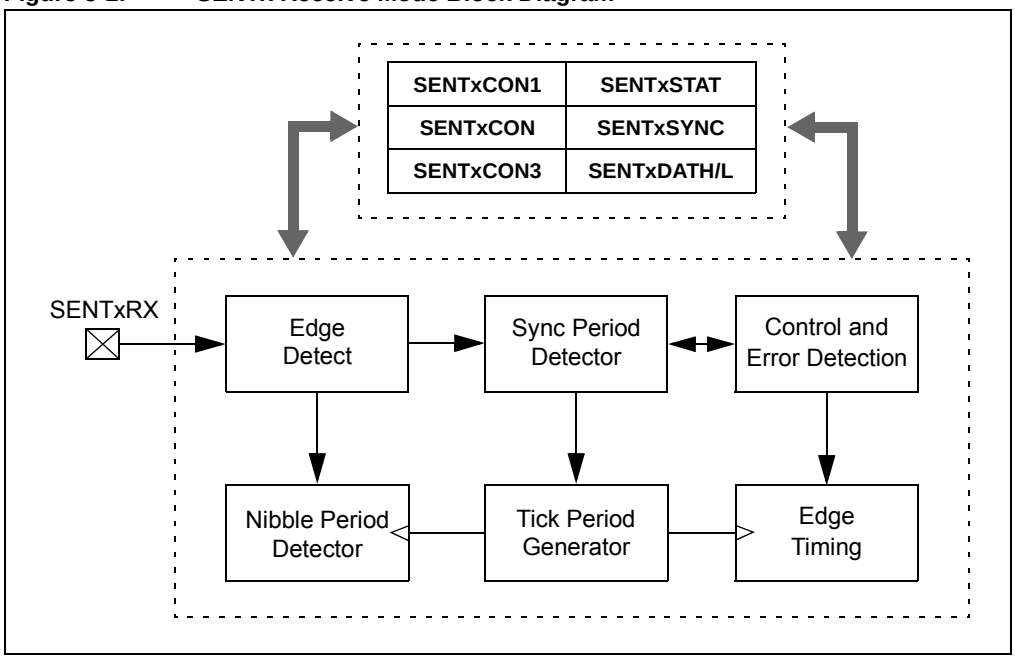
- Poll the data pin using the PORTx register associated with the pin
- Enable an input capture peripheral that is multiplexed on the SENT data pin.
- Enable a Change Notification (CN) input or a comparator that is multiplexed on the SENT data pin.

After a SPC pulse is found, the application disables any peripherals associated with SPC pulse detection, then initiates a SENT transmission by setting the SYNCTXEN bit.

5.0 RECEIVE MODE

The module can be operated as a receiver when RCVEN (SENTxCON1<11>) = 1. If the serial data is valid, it is decoded by the module and made available in the SENTxDATH/L register. Error checking and status information is made available in the SENTxSTAT and SENTxSYNC registers. The captured Sync period value is readable in the SENTxSYNC register. A block diagram of the module in Receive mode is shown in Figure 5-1.

Figure 5-1: SENTx Receive Mode Block Diagram



5.1 Receive Mode Timing Calculations

When configured for Receive mode, SENTxCON2 and SENTxCON3 registers are used to hold the maximum (SYNCMAX<15:0>) and minimum (SYNCMIN<15:0>) boundary values of the Sync period for validation of the Sync pulse. SYNCMIN and SYNCMAX are ±20% of the nominal Sync period. Received Sync periods outside this window will be rejected by the receiver.

The equation for SYNCMIN and SYNCMAX is shown in Equation 5-1. As in the Transmit modes, the value for FRCV is either FCY or FCY/4, depending on the setting of the PS bit.

Equation 5-1: Calculating SYNCMIN and SYNCMAX

$$SyncCount = 8 \cdot F_{RCV} \cdot T_{TICK}$$

$$SYNCMIN = 0.8 \cdot SyncCount$$

$$SYNCMAX = 1.2 \cdot SyncCount$$

Where:

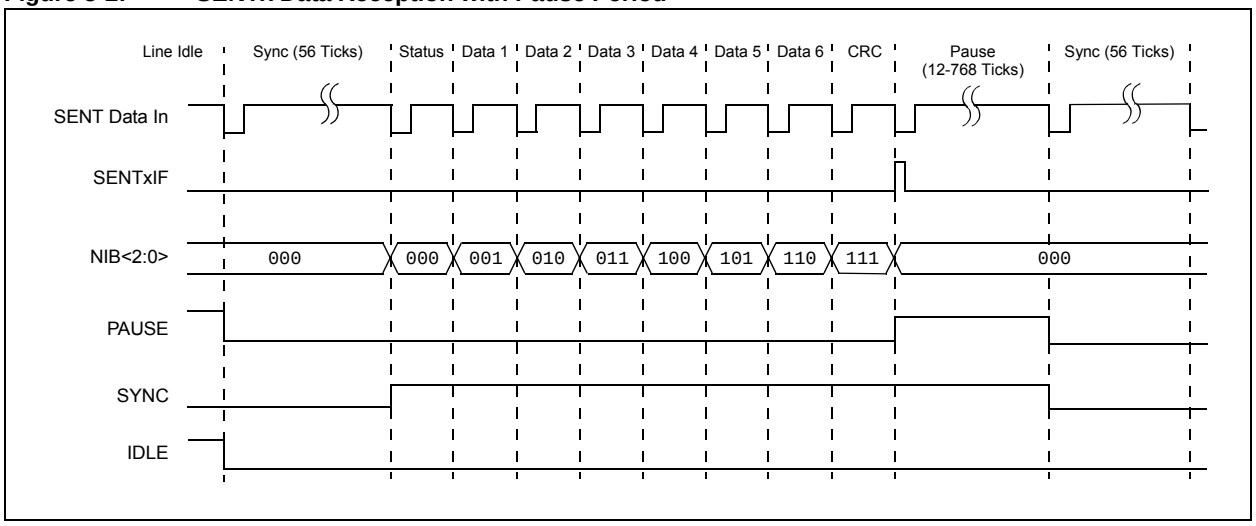
$$F_{RCV} = F_{CY}/Prescaler$$

Note: The SENT protocol allows no more than 1.5625% (1 part in 64) timing variation between successive messages. To verify this condition is met, save the value captured in SENTxSYNC after each data frame is received, then compare it to the value received during the next data frame.

5.2 Receiver Status

When the module is configured as a receiver (RCVEN = 0), the status of the received message (nibble status, line state, Sync and Pause states) is stored in the SENTxSTAT register. Figure 5-2 shows the relationship between the SENT data in the signal and the SENTxSTAT status bits.

Figure 5-2: SENTx Data Reception with Pause Period



Note: The receiver is in the Idle state when the SENT data line has been high for more than the maximum time allowed for a Sync period (SYNCMAXx bits register value).

5.3 Receive Input Pin and PPS

On devices with Peripheral Pin Select (PPS), the SENT Receive (SENTxRX) pin function is an independently remappable feature. To use the module in Receive mode, SENTxRX must be mapped to an available I/O pin using the appropriate RPINRx or RPORx register. If Short PWM Code support is required, a bidirectional mappable pin must be used in order to support the pulse output.

5.4 Receive Setup Procedure

To fully configure the module, the following must be known:

- TTICK (Equation 4-1)
- Number of Data Nibbles
- Hardware or Application Calculated CRC Validation
- Pause Period Present

Note: Application software can be used to implement an alternate CRC algorithm. In these instances, disable hardware CRC checking by clearing CRCEN (SENTxCON1<8>). The received CRC value (SENTxDATA<3:0>) can be read and compared against the application calculated CRC value.

To initialize the module for Receive mode:

1. Set RCVEN (SENTxCON1<11>) for Receive mode.
2. Write the desired data frame length to NIBCNT<2:0> (SENTxCON1<2:0>).
3. Set or clear CRCEN (SENTxCON1<8>) to configure the module for hardware or software CRC calculation.
4. If the Pause period is present, set PPP (SENTxCON1<7>).
5. Write the value of SYNCMAX (nominal Sync period + 20%) to SENTxCON2.
6. Write the value of SYNCMIN (nominal Sync period – 20%) to SENTxCON3.
7. Enable the SENT interrupts and set the interrupt priority.
8. Set the SNTEN bit (SENTxCON1<15>) to enable the module.

Incoming data is read from the SENTxDATH/L registers after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt trigger.

5.5 Error Handling

The module has the capability to automatically detect and flag framing errors and CRC mismatch. A framing error is the detection of a status or data nibble period, less than 12 Ticks or greater than 27 Ticks. If a framing error is detected, the FRMERR bit (SENTxSTAT<2>) is set and a receive error interrupt is generated. After a framing error has been detected, the module clears SYNCTXEN (SENTxSTAT<0>) and begins looking for another valid Sync period. The FRMERR bit remains set until another valid Sync period has been detected and SYNCTXEN = 1. The application may optionally clear the FRMERR bit.

Note:	If the PPP bit is set, the module will not generate a framing error on successive valid Sync pulses. This is due to the possibility that a Pause Pulse could be interpreted as a valid Sync and the following actual Sync pulse interpreted as a frame error. Framing errors for nibble data will still be detected when PPP = 1.

If CRC verification fails, the CRCERR bit (SENTxSTAT<3>) is set and a receive error interrupt is generated. The CRCERR bit remains set until a valid Sync period for a new message has been received. Software may optionally clear the CRCERR bit. The CRCEN bit (SENTxCON1<8>) must be set to receive an interrupt on a CRC error.

5.6 Short PWM Code (SPC) Support

The SENT module provides support for implementing SPC with assistance from other external peripherals. The SPCEN (SENTxCON1<6>) bit enables an external Output Compare (OC) peripheral to control the SENT data input pin. In general, a specific OC module is linked in hardware to a specific SENTx module. Refer to the device data sheet for more information.

To initialize the SENT module for SPC operation:

1. Set the SPCEN (SENTxCON1<6>) bit to enable control of the SENT data pin by an external source.
2. For devices with Peripheral Pin Select, map the SENTxTX function to the same I/O pin as SENTxRX.
3. Configure the Output Compare module as follows:
   a) Configure the module for Triggered mode.
   b) Configure for a single-shot, active-high pulse.
   c) Set the Period and Duty Cycle registers for the desired pulse duration.

After configuration, to use the SPC Pulse trigger:

1. Verify that the line is in a high-impedance state by polling the RXIDLE bit (SENTxSTAT<1>).
2. Set the Trigger bit of the OC module to trigger the SPC pulse.

During the active period of the SPC pulse, the SENT receiver edge detection is disabled and the SENT data input pin is driven low by the module. The receiver logic is reset at this time to prepare for a new data frame. When the pulse is completed, the module releases control of the SENT data input pin and input edge detection is re-enabled so a data frame can be received from the sensor.

Note:	To implement the SPC protocol, the SENT transmitting device(s) must leave the data bus in a high-impedance state after the falling edge that completes the CRC nibble period. At this time, the SENT data line will be pulled high by the external pull-up resistor. The data bus should not be driven by any transmitter devices until the receiver device requests data by placing a low pulse on the SENT data line.

It is also possible to manually control the SENT data pin to implement the SPC protocol. This can be done as follows:

1. Clear the SNTEN bit to disable receiver operation.
2. Manipulate the PORTx and TRISx registers associated with the SENT data pin to drive the data pin low for the desired time.
3. Return the SENT data pin to a high-impedance condition using the TRISx register.
4. Set the SNTEN bit to resume receiver operation.

6.0 INTERRUPTS

Each SENT module has two interrupts associated with its operation: the SENTx Transmit/Receive Interrupt Flag (SENTxIF), and the SENTx Error Interrupt Flag (SENTxEIF). Setting the corresponding SENTx Interrupt Enable bits (SENTxIE and SENTxEIE) allows the module to generate device-level interrupts.

The transmit/receive interrupt is generated after the transmission of a message frame in Transmit mode or the successful reception of a message frame in Receive mode.

The error interrupt is generated after a frame error or a CRC error in Receive mode.There are no error interrupts generated in Transmit mode.

7.0 OPERATION IN POWER-SAVING MODES

7.1 Sleep Mode

The SENT module does not support operation when the device is in Sleep mode. If the application requires the device to enter Sleep mode, the module should be halted by clearing the SNTEN bit (SENTxCON1<15>). If operated as a transmitter, the application can wait until the module is done transmitting a message frame before entering Sleep.

7.2 Idle Mode

The SENT module provides two options of operation when the device enters Idle mode. If SNTSIDL (SENTxCON1<13>) = 1, module operation stops when the device enters Idle mode. The same system considerations described in Sleep mode apply.

If SNTSIDL = 0, the module will continue the transmission or reception process after the device enters Idle mode. When operating in Transmitter mode, the module will continue to send messages with the data contained in SENTxDATH/L unless the device wakes from Idle to write new data. If the module is operating in Receive mode, any old data in the SENTxDATH/L registers will be lost unless the device wakes from Idle to read the data.

8.0 EFFECTS OF A RESET

A device Reset forces all registers to their Reset state. This forces the SENT module to be turned off and any message frames in progress to be aborted. All SENT pins that are multiplexed with analog inputs are configured as analog inputs. The corresponding TRISx bits are also set, effectively making all pins inputs.

9.0 REGISTER MAP

A summary of the Special Function Registers associated with the SENT module is provided in Table 9-1.

Table 9-1: Special Function Registers Associated with the SENT Module

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SENTxCON1	SNTEN	—	SNTSIDL	—	RCVEN	TXM	TXPOL	CRCEN	PPP	SPCEN	—	PS	—	NIBCNT2	NIBCNT1	NIBCNT0	0006
SENTxCON2	TICKTIME<15:0> (Transmit modes) or SYNCMAX<15:0> (Receive mode)																FFFF
SENTxCON3	FRAMETIME<15:0> (Transmit modes) or SYNCMIN<15:0> (Receive mode)																FFFF
SENTxSTAT	—	—	—	—	—	—	—	—	PAUSE	NIB2	NIB1	NIB0	CRCERR	FRMERR	RXIDLE	SYNCTXEN	0000
SENTxSYNC	Synchronization Time Period (Transmit modes)																0000
SENTxDATH	Status Nibble				Data Nibble 1				Data Nibble 2				Data Nibble 3				0000
SENTxDATL	Data Nibble 4				Data Nibble 5				Data Nibble 6				CRC Data Nibble				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

10.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for 16-bit devices, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the SENT module are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the dsPIC33/PIC24F family of devices.

11.0 REFERENCE NOTES

Title

"SENT – Single-Edge Nibble Transmission for Automotive Applications"
Author: SAE International

http://www.sae.org/

12.0 REVISION HISTORY

Revision A (November 2013)

This is the initial released revision of this document.

Revision B (April 2014)

Changed title from *Single-Ended Nibble Transmission (SENT) Module* to *Single-Edge Nibble Transmission (SENT) Module*.

Added reference to *"SENT – Single-Edge Nibble Transmission for Automotive Applications"* SAE International document.

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