



PIC16(L)F183XX Data Signal Modulator (DSM) Technical Brief

Author: Christopher Best

Microchip Technology Inc.

INTRODUCTION

The Data Signal Modulator (DSM) is a peripheral which allows the user to mix a data stream, also known as the modulator (MOD) signal, with a carrier signal to produce a modulated output.

Both the carrier and the modulator signals are supplied to the DSM module either internally, from the output of a peripheral, or externally through an input pin.

The modulated output signal is generated by performing a logical "AND" operation of both the carrier and modulator signals which are then provided to the MDOUT pin.

The carrier signal is comprised of two distinct and separate signals, a carrier high (CARH) signal and a carrier low (CARL) signal. The carrier signal is usually of a frequency higher than the modulator signal.

During the time in which the modulator signal is in a logic high state, the DSM outputs the carrier high signal. When the modulator signal is in a logic low state, the DSM outputs the carrier low signal.

Using this method, the DSM can generate the following types of Key Modulation schemes:

- Frequency-Shift Keying (FSK)
- Phase-Shift Keying (PSK)
- On-Off Keying (OOK)

Additionally, the following features are provided within the DSM module:

- · Carrier Synchronization
- Carrier Source Polarity Select
- · Carrier Source Pin Disable
- Programmable Modulator Data
- Modulator Source Pin Disable
- · Modulated Output Polarity Select
- · Slew Rate Control

Figure 1 shows a Simplified Block Diagram of the Data Signal Modulator peripheral found in the PIC16(L)F18323.

DSM SIMPLIFIED BLOCK DIAGRAM FIGURE 1: MDCH<3:0> Data Signal Modulator V_{SS} 0000 MDCIN1 MDCIN2 CLKR CCP1 CCP2 PWM5 PWM6 NCO 0001 0010 0011 0100 0101 0110 CARH 0111 1000 1001 1010 1011 RESERVED Fosc HFINTOSC MDCHPOL CLC1 CLC2 1100 1101 1110 1111 D RESERVED RESERVED SYNC 1 MDMS<3:0> 0 **MDBIT** 0000 0001 0010 0011 \boxtimes MDMIN CCP1 CCP2 PWM5 PWM6 C1OUT MDCHSYNC 0100 0101 0110 0111 C2OUT SDO1 RESERVED EUSART TX MOD 1000 1001 1010 DSM NCO CLC1 CLC2 RESERVED 1010 1011 1100 1101 1110 1111 **MDOPOL** RESERVED MDCL<3:0>-D SYNC V_{SS}
MDCIN1
MDCIN2
CLKR
CCP1
CCP2
PWM5
PWM6
NCO 0000 0000 0001 0010 0011 1 0100 0101 0 0110 0111 1000 1001 1010 RESERVED Fosc HFINTOSC CLC1 MDCLSYNC 1011 1100 CLC2 RESERVED RESERVED 1101 1110 MDCLPOL 1111

KEY MODULATION SCHEMES

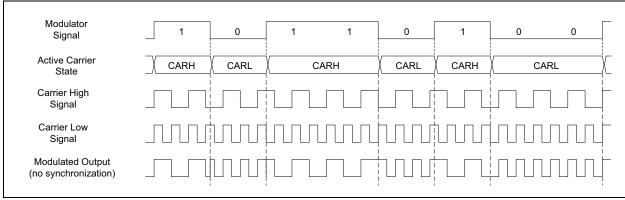
The DSM can generate the following three types of key modulation schemes:

- Frequency-Shift Keying (FSK)
- Phase-Shift Keying (PSK)
- On-Off Keying (OOK)

Frequency-Shift Keying

Frequency-Shift Keying (FSK) uses both carrier signals to determine the digital state of the modulator signal. When using FSK it is important to use carrier signals of different frequencies. Figure 2 illustrates an FSK modulated output. While the modulator signal is at a high state, the carrier high signal (CARH) is the active carrier, and the modulated output frequency will match that of CARH. When the modulator signal is at a low state, the active carrier state switches to the carrier low signal (CARL), and the resulting modulated output frequency will match that of CARL. Each of the two frequencies is then decoded by the receiver as either the high state or low state of the original modulator signal.

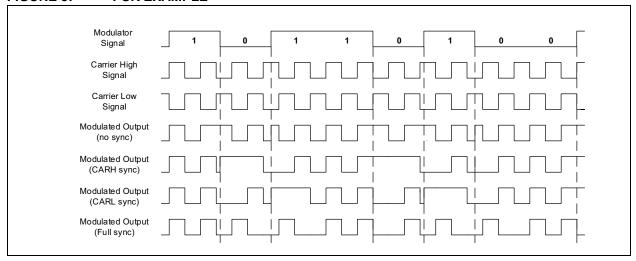




Phase-Shift Keying (PSK)

Phase-Shift Keying (PSK) uses both carrier signals, but rather than relying on a difference of carrier frequencies as with FSK, PSK uses carrier signals that are out of phase with each other. The carrier signals could come from the same source, such as CCP1, but with one of the sources inverted. The signals could also come from different sources, such as CCP1 and CCP2, as long as the signals are out of phase. Figure 3 illustrates a PSK example, with and without carrier synchronization.

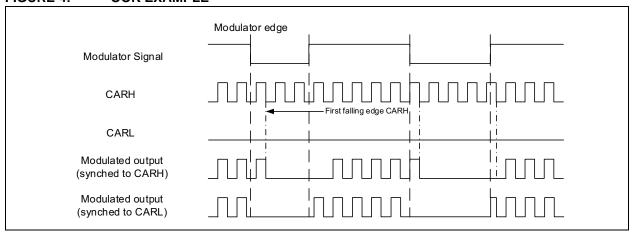
FIGURE 3: PSK EXAMPLE



On-Off Keying (OOK)

On-Off Keying (OOK) uses both carrier sources; however, one of the carrier sources is tied to ground (Vss). In a typical OOK configuration, a binary 'one' occurs when the carrier with an active frequency is present, and a binary 'zero' occurs when the carrier tied to Vss is present. Figure 4 illustrates an OOK configuration in which the carrier high signal is active and the carrier low signal is tied to Vss.

FIGURE 4: OOK EXAMPLE



DSM OPERATION

The DSM module is enabled by setting the MDEN bit in the MDCON register.

Clearing the MDEN bit in the MDCON register disables the DSM module by automatically switching the carrier high and carrier low signals to the VSS signal source. The modulator signal source is also switched to the MDBIT in the MDCON register. This not only assures that the DSM module is inactive, but that it is also consuming the least amount of current. During the time that the DSM is disabled, the DSM pin will remain low.

The values used to select the carrier high, carrier low, and modulator sources held by the Modulation Source, Modulation High Carrier, and Modulation Low Carrier control registers are not affected when the MDEN bit is cleared and the DSM module is disabled. The values inside these registers remain unchanged unless written by the user, while DSM is inactive. When the MDEN bit is set, the sources for the carrier high, carrier low and modulator signals are enabled and active.

Modulator Signal Sources

The modulator signal can be supplied from the following sources:

- · CCP1 Signal
- CCP2 Signal
- PWM5 Output
- PWM6 Output
- MSSP1 SDO1 Signal (SPI mode only)
- · Comparator C1 Signal
- Comparator C2 Signal
- EUSART TX Signal
- · External Signal on MDMIN pin
- NCO Data Output
- CLC1 Output
- CLC2 Output
- · MDBIT bit in the MDCON register

The modulator signal is selected by configuring the MDMS <3:0> bits in the MDSRC register.

Carrier Signal Sources

The carrier high signal and carrier low signal can be supplied from the following sources:

- CCP1 Signal
- · CCP2 Signal
- PWM5 Output
- PWM6 Output
- NCO output
- Fosc (system clock)
- HFINTOSC
- CLC1 output
- CLC2 output
- Reference Clock Module Signal
- External Signal on MDCIN1 pin
- · External Signal on MDCIN2 pin
- Vss

The carrier high signal is selected by configuring the MDCH <3:0> bits in the MDCARH register. The carrier low signal is selected by configuring the MDCL <3:0> bits in the MDCARL register.

Modulation without Carrier Synchronization

When the DSM switches between carrier signal sources (MDCH to MDCL or vice versa), and the MDCxSYNC bit is clear, the current carrier signal is immediately disabled and the new carrier is immediately enabled. In the example in Figure 2, once the modulator signal transitions from high-to-low, the carrier high signal is immediately disabled while the carrier low signal is immediately enabled. When the modulator signal transitions from low-to-high, the low carrier signal is immediately disabled while the high carrier is immediately enabled.

Modulation with Carrier Synchronization

During the time in which the DSM switches between carrier signal sources, the carrier data in the modulated output signal can become truncated. To prevent this, the carrier signal can be synchronized to the modulator signal. Synchronization is enabled separately for the carrier high and carrier low signal sources. Synchronization for the carrier high signal is enabled by setting the MDCHSYNC bit in the MDCARH register, while synchronization for the carrier low signal is enabled by setting the MDCLSYNC bit in the MDCARL register.

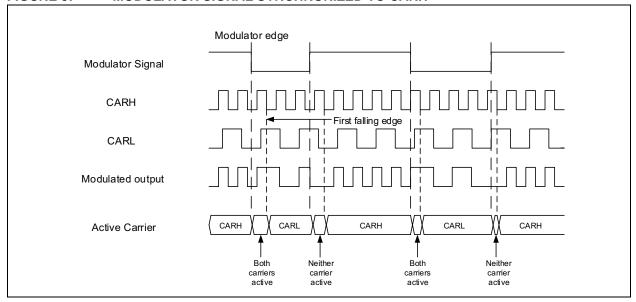
SYNCHRONIZATION TO A SINGLE CARRIER

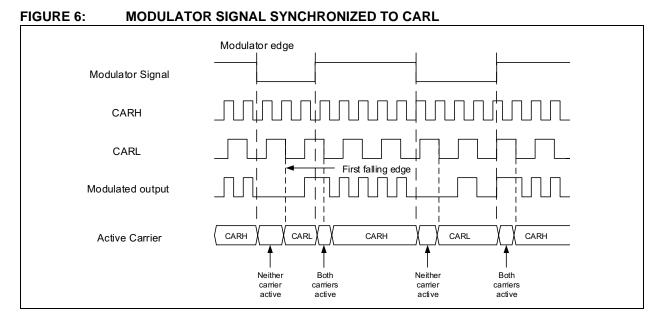
The modulator source can be synchronized to a single carrier source (see Figure 5 and Figure 6). When the modulator signal transitions away from the synchronized carrier, the unsynchronized carrier source is immediately active, while the synchronized carrier remains active until its next falling edge. When the modulator signal transitions back to the synchronized carrier, the unsynchronized carrier is immediately disabled, and the modulator waits until the next falling edge of the synchronized carrier before the synchronized carrier becomes active.

For example, when the modulator is synchronized to the high carrier source (CARH):

- When the modulator pulse transitions from highto-low, the modulator will immediately activate the carrier low signal source (CARL), and both CARL and CARH will be active until the next falling edge of CARH, and when that edge occurs, CARH will be released.
- When the modulator pulse transitions from lowto-high, the modulator releases the CARL signal and remains inactive until the next falling edge of CARH, and once this edge occurs, the modulator will immediately follow the CARH signal.

FIGURE 5: MODULATOR SIGNAL SYNCHRONIZED TO CARH





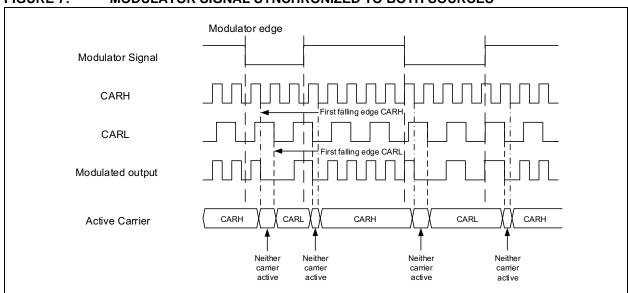
SYNCHRONIZATION TO BOTH CARRIER SOURCES

The modulator can also be synchronized to both carrier sources.

When the modulator pulse transitions from high-to-low, the CARH remains the active carrier until the next falling edge of CARH. Once this edge occurs, CARH is released, and the modulator remains inactive until the next falling edge of CARL, and once that edge occurs, the DSM output follows carrier low signal.

When the modulator pulse transitions from low-to-high, the CARL remains the active carrier source until the next falling edge of CARL. Once this edge occurs, CARL is released and the modulator remains inactive until the next falling edge of CARH, and once that edge occurs, the DSM output follows carrier high signal (see Figure 7).





Carrier Source Polarity Select

The signal provided from any selected input source for the carrier high and carrier low signals can be inverted. Inverting the signal for the carrier high source is enabled by setting the MDCHPOL bit in the MDCARH register. Inverting the signal for the carrier low source is enabled by setting the MDCLPOL bit in the MDCARL register.

When using the Phase-Shift Keying method, it may be convenient to use the same carrier signal source for both carriers, and simply inverting one of the signals to get the phase shift.

Modulated Output Polarity

The modulated output signal on the DSM pin can also be inverted. Inverting the modulated output signal is achieved by setting the MDOPOL bit in the MDCON register.

Programmable Modulator Input Signal

The MDBIT in the MDCON register can be selected as the source for the modulator signal. This allows the software to directly control the value used for the modulator signal.

Slew Rate Control

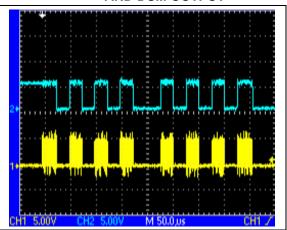
The slew rate limitation on the output port pin can be disabled. This may be necessary when using signal frequencies greater than 8 MHz. The slew rate limitation can be disabled by clearing the SLR bit in the SLRCON register associated with the output pin.

DSM Code Example

The following code example illustrates the use of the DSM. The example uses a push-button to output a 6-byte code as a modulated signal. The 6-byte code is stored in an array, and is sent internally from the SPI serial data output (SDO) to the modulator source input of the DSM. Several carrier and polarity selections are included in the example for reference, but are commented out.

Figure 8 shows a scope plot of the SPI SDO output (trace 2) and the output of the DSM (trace 1). The first two bytes of the output code, 0xAA and 0x55, are shown.

FIGURE 8: ACTUAL SPI SDO OUTPUT AND DSM OUTPUT



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EXAMPLE 1: DSM CODE EXAMPLE

```
/* File: main.c
* Author: Christopher Best, Microchip Technology
 * DSM Test code - PIC16F18323
#include <stdint.h>
#include <xc.h>
// ADD CONFIGURATION WORD SETTINGS !!!
uint8 t
             Output Code Buffer[] = \{0xAA, 0x55, 0x00, 0x00, 0xCC, 0xF1\};
volatile uint8 t send data = 0;
void initialize(void);
void SPI Exchange8bit(void);
main()
{
    initialize();
    while(1)
         if(send_data)
         {
            SPI Exchange8bit();
            send data = 0;
    }
}
void initialize (void)
{
     // Oscillator settings
    OSCFRQbits.HFFRQ = 0b1111; // Change HFINTOSC freq to 16 MHz
    // SPI settings
    SSPCON1bits.SSPM = Ob1010; // SPI Master Clock @ FOSC/(4*(SSP1ADD + 1)
    SSPCON1bits.SSPEN = 1;  // Enable SPI
    SSP1ADD = 0x62;
     // DSM general settings
    MDSRCbits.MDMS = 0b1000; // Select SPI SDO as modulator source
    \label{eq:mdcarhbits.mdchsync} \texttt{MDCARHbits.MDCHSYNC} = 1; \qquad // \text{ Synch carrier with modulator signal}
                                 // Synch carrier with modulator signal if needed
// DSM output not inverted
    MDCARLbits.MDCLSYNC = 0;
    MDCONbits.MDOPOL = 0;
    // On-Off Keying (OOK) Example Settings
    MDCARHbits.MDCH = 0b1011; // High carrier source = HFINTOSC MDCARLbits.MDCL = 0b0000; // Low carrier to Vss (to use as OOK)
```

EXAMPLE 1: DSM CODE EXAMPLE (CONTINUED)

```
// Phase-Shift Keying (PSK) Example Settings
 // Uses same carrier source, but inverts the low carrier to shift phase
//MDCARHbits.MDCH = 0b1011; // High carrier source = HFINTOSC
//MDCARLbits.MDCL = 0b1011; // Low carrier source = HFINTOSC
 //MDCARLbits.MDCLPOL = 1;
                               // Invert carrier to shift phase
// Frequency-Shift Keying (FSK) Example Settings
 // Uses Carrier sources of different frequencies
//MDCARHbits.MDCH = 0b0001; // High carrier source = MDCIN1PPS
//MDCARLbits.MDCL = 0b0010; // Low carrier source = MDCIN2PPS
// I/O Port settings
LATC = 0 \times 00;
                             // Clear PORTC latches
ANSELC = 0 \times 00;
                             // Make PORTC digital I/O's
                            // SPI SCK output
TRISCbits.TRISC0 = 0;
TRISCbits.TRISC2 = 0;
                           // SPI SDO output (used to compare to actual DSM signal)
 TRISCbits.TRISC3 = 0;
                             // DSM modulated output
TRISCbits.TRISC5 = 1;
                           // Enable weak pull-up for SDI input
WPUCbits.WPUC1 = 1;
SLRCONCbits.SLRC3 = 0; // Use slew rate at maximum
I.ATA = 0x00:
 ANSELA = 0 \times 00;
TRISAbits.TRISA4 = 1;
TRISAbits.TRISA5 = 1;
 // SPI settings:
SSP1DATPPSbits.SSP1DATPPS = 0b10001; // Use RC1 as SDI input
                                       // Use RC0 as SCK output
// Use RC2 as SDO output
 RCOPPSbits.RCOPPS = 0b11000;
RC2PPSbits.RC2PPS = 0b11001:
 // DSM settings:
MDCIN1PPSbits.MDCIN1PPS = 0b00101; // use RA5 as input
MDCIN2PPSbits.MDCIN2PPS = 0b00100; // use RA4 as input
RC3PPSbits.RC3PPS = 0b11111; // Use RC3 as DSM output
 // INT pin settings:
INTPPSbits.INTPPS = 0b10101;
                                        // Use RC5 as INT input
 // Interrupt settings
                        // Enable IOC interrupts
// Clear IOC flag
PIE0bits.INTE = 1;
 PIRObits.INTF = 0;
 INTCONbits.INTEDG = 0;
                            // Enable peripheral interrupts
INTCONbits.PEIE = 1;
INTCONbits.GIE = 1;
                           // Enable global interrupts
void interrupt ISR(void)
   if(PIRObits.INTF)
                                   // Has button been pushed?
   {
        send_data = 1;
                                   // Set bit to enable SPI transmission
        PIRObits.INTF = 0;
   if(PIR3bits.CSWIF) PIR3bits.CSWIF = 0;
void SPI Exchange8bit(void)
   uint8_t bytesWritten = 0;
   uint8_t generic_read = 0;
   MDCONbits.MDEN = 1;
                                // Enable Modulator
   while(bytesWritten < 6)</pre>
        SSP1BUF = Output_Code_Buffer[bytesWritten++];
        while(!SSPSTATbits.BF){};
        generic_read = SSP1BUF;
   MDCONbits.MDEN = 0;
                                // Disable Modulator
```

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