TC962

High Current Charge Pump DC-to-DC Converter

Features

- Pin Compatible With TC7662/ICL7662/SI7661
- High Output Current 80 mA
- No External Diodes Required
- Wide Operating Range 3V to 18V
- Low Output Impedance 28Ω Typical
- No Low-Voltage Terminal Required
- Application Zener On-Chip
- OSC Frequency Doubling Pin Option for Smaller Output Capacitors

Applications

- Laptop Computers
- Disk Drives
- Process Instrumentation
- μP-Based Controllers

Device Selection Table

Part Number	Package	Operating Temp. Range
TC962CPA	8-Pin Plastic DIP	0°C to +70°C
TC962EPA	8-Pin Plastic DIP	-40°C to +85°C
TC962COE	16-Pin SOIC Wide	0°C to +70°C

General Description

The TC962 is an advanced version of the industry standard TC7662 high-voltage DC-to-DC converter. Using improved design techniques and CMOS construction, the TC962 can source as much as 80 mA versus the TC7662's 20 mA capability.

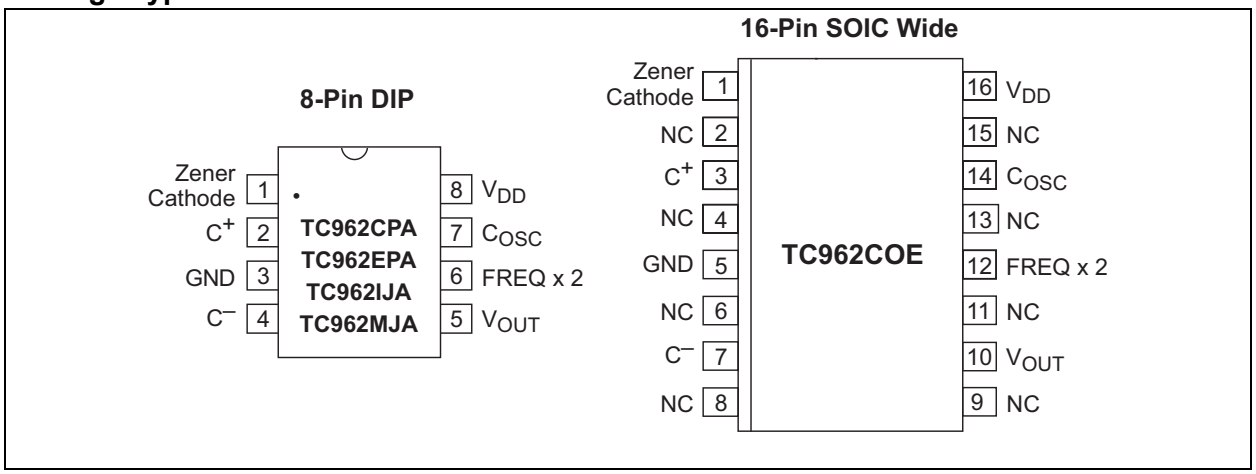
As an inverter, the TC962 can put out voltages as high as 18V and as low as 3V without the need for external diodes. The output impedance of the device is a low 28Ω (with the proper capacitors), voltage conversion efficiency is 99.9 and power conversion efficiency is 97%.

The low-voltage terminal (pin 6) required in some TC7662 applications has been eliminated. Grounding this terminal will double the oscillator frequency from 12 kHz to 24 kHz (note that the measurable switching frequency is 6 kHz and 12 kHz, respectively). This will allow the use of smaller capacitors for the same output current and ripple in most applications. Only two external capacitors are required for inverter applications. In the event an external clock is needed to drive the TC962 (such as paralleling), driving this pin directly will cause the internal oscillator to sync to the external clock.

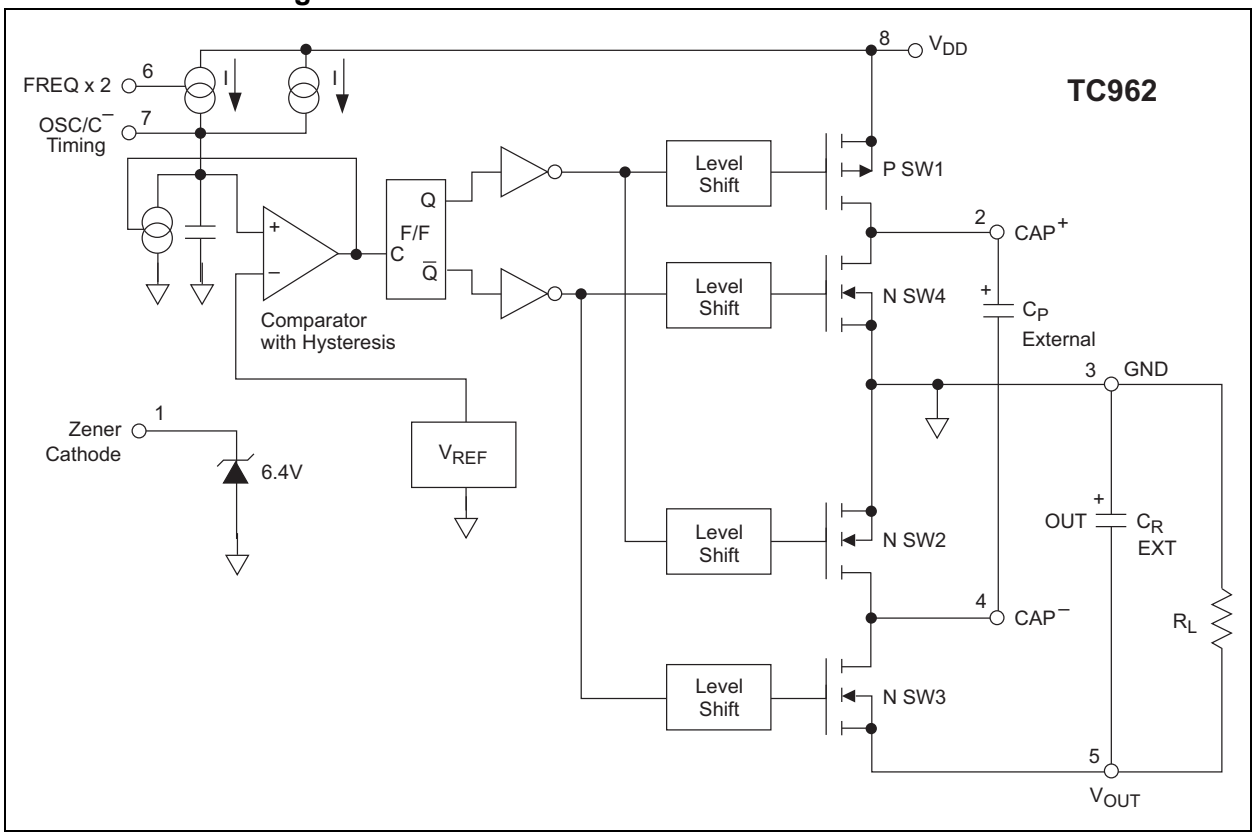
Pin 1, which is used as a test pin on the TC7662, is a voltage reference Zener on the TC962. This Zener (6.4V at 5 mA) has a dynamic impedance of 12Ω and is intended for use where the TC962 is supplying current to external regulator circuitry and a reference is needed for the regulator circuit. (See ***Section 3.0 "Applications Information"***).

The TC962 is compatible with the LTC1044, SI7661 and ICL7662. It should be used in designs that require greater power and/or less input to output voltage drop. It offers superior performance over the ICL7660S.

Package Type



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD} to GND) ..... +18V
Input Voltage Any Pin ..... (V_{DD} + 0.3) to (V_{SS} – 0.3) **(Note 1)**
Current Into Any Pin ..... 10 mA
ESD Protection ..... ±2000V
Output Short Circuit ..... Continuous (at 5.5V Input)
Package Power Dissipation ($T_A \leq 70°C$)
SOIC ..... 760 mW
PDIP ..... 730 mW
Package Thermal Resistance
PDIP, $R\theta_{J-A}$ ..... 140°C/W
Operating Temperature Range
CPA, COE ..... 0°C to +70°C
EPA ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC962 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_{DD} = 15V, T_A = 25°C unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Supply Voltage	V_{DD}	3	—	18	V	
Supply Current V_{DD} = 15V	I_S	— — — —	— 510 560 650	— 700 — —	µA	$R_L = \infty$ T_A = +25°C $0 \leq T_A \leq +70°C$ $-55°C \leq T_A \leq +125°C$
Supply Current V_{DD} = 5V	I_S	— — —	190 210 210	— — —	µA	T_A = +25°C $0 \leq T_A \leq +70°C$ $-55°C \leq T_A \leq +125°C$
Output Source Resistance	R_O	— — —	32 35 —	37 40 50	Ω	I_L = 20 mA, V_{DD} = 15V I_L = 80 mA, V_{DD} = 15V I_L = 3 mA, V_{DD} = 5V
Oscillator Frequency	F_{OSC}	— —	12 24	— —	kHz	Pin 6 Open Pin 6 GND
Switching Frequency **(Note 2)**	F_{SW}	— —	6 12	— —	kHz	Pin 6 Open Pin 6 GND
Power Efficiency	P_{EFF}	93 —	97 —	— —	%	R_L = 2 kΩ
Voltage Efficiency	V_{DEF}	99 — 96	99.9 — —	— — —	%	$R_L = \infty$ Over temperature range
Zener Voltage	V_Z	6.0	6.2	6.4	V	I_Z = 5 mA
Zener Impedance	Z_{ZT}	—	12	—	Ω	I_L = 2.5 mA to 7.5 mA

Note 1: Connecting any input terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to “power-up” of the TC962.
2: Switching frequency is one-half of the internal oscillator frequency.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in the table below:

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin DIP)	Symbol	Description
1	Zener Cathode	Cathode of an internal Zener diode
2	C^+	Positive side of an external CP capacitor (pump cap)
3	GND	Ground terminal
4	C^-	Negative side of an external CP capacitor (pump cap)
5	V_{OUT}	Output voltage
6	FREQ x 2	If grounded, the frequency doubles
7	C_{OSC}	Capacitor to GND will decrease the frequency
8	V_{DD}	Input voltage

Pin No. (16-Pin SOIC)	Symbol	Description
1	Zener Cathode	Cathode of an internal Zener diode
2	NC	No connect
3	C^+	Positive side of an external CP capacitor (pump cap)
4	NC	No connect
5	GND	Ground terminal
6	NC	No connect
7	C^-	Negative side of an external CP capacitor (pump cap)
8	NC	No connect
9	NC	No connect
10	V_{OUT}	Output voltage
11	NC	No connect
12	FREQ x 2	If grounded, the frequency doubles
13	NC	No connect
14	C_{OSC}	Capacitor to GND will decrease the frequency
15	NC	No connect
16	V_{DD}	Input voltage

3.0 APPLICATIONS INFORMATION

3.1 Theory of Operation

The TC962 is a capacitive pump (sometimes called a switched capacitor circuit), where four MOSFET switches control the charge and discharge of a capacitor.

The functional block diagram shows how the switching action works. SW1 and SW2 are turned on simultaneously, charging C_P to the supply voltage, V_{IN}. This assumes that the on resistance of the MOSFETs in series with the capacitor results in a charging time (three time constants) that is less than the on time provided by the oscillator frequency, as shown:

$$3\ (R_{DS(ON)}\ C_P) < C_P/(0.5\ f_{OSC})$$

In the next cycle, SW1 and SW2 are turned off and after a very short interval of all switches being off (this prevents large currents from occurring due to cross conduction), SW3 and SW4 are turned on. The charge in C_P is then transferred to C_R, *but with the polarity inverted*. In this way, a negative voltage is now derived.

An oscillator supplies pulses to a flip-flop that is then fed to a set of level shifters. These level shifters then drive each set of switches at one-half the oscillator frequency.

The oscillator has two pins that control the frequency of oscillation. Pin 7 can have a capacitor added that is returned to ground. This will lower the frequency of the oscillator by adding capacitance to the timing capacitor internal to the TC962. Grounding pin 6 will turn on a current source and double the frequency. This will double the charge current going into the internal capacitor as well as any capacitor added to pin 7.

A Zener diode has been added to the TC962 for use as a reference in building external regulators. This Zener runs from pin 1 to ground.

3.2 Latch-Up

All CMOS structures contain a parasitic SCR. Care must be taken to prevent any input from going above or below the supply rail, or a latch-up will occur. The result of a latch-up is an effective short between V_{DD} and V_{SS}. Unless the power supply input has a current limit, this latch-up phenomena will result in damage to the device. (*See AN763, Latch-up Protection for MOSFET Drivers*).

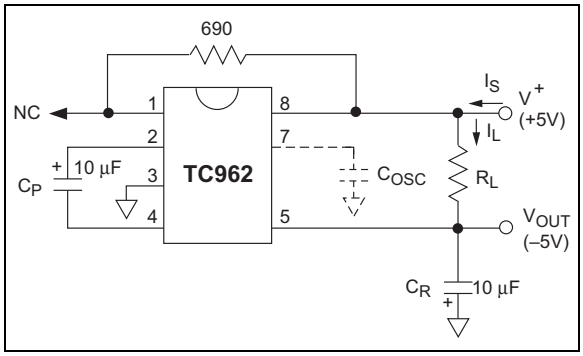


FIGURE 3-1: *Test Circuit.*

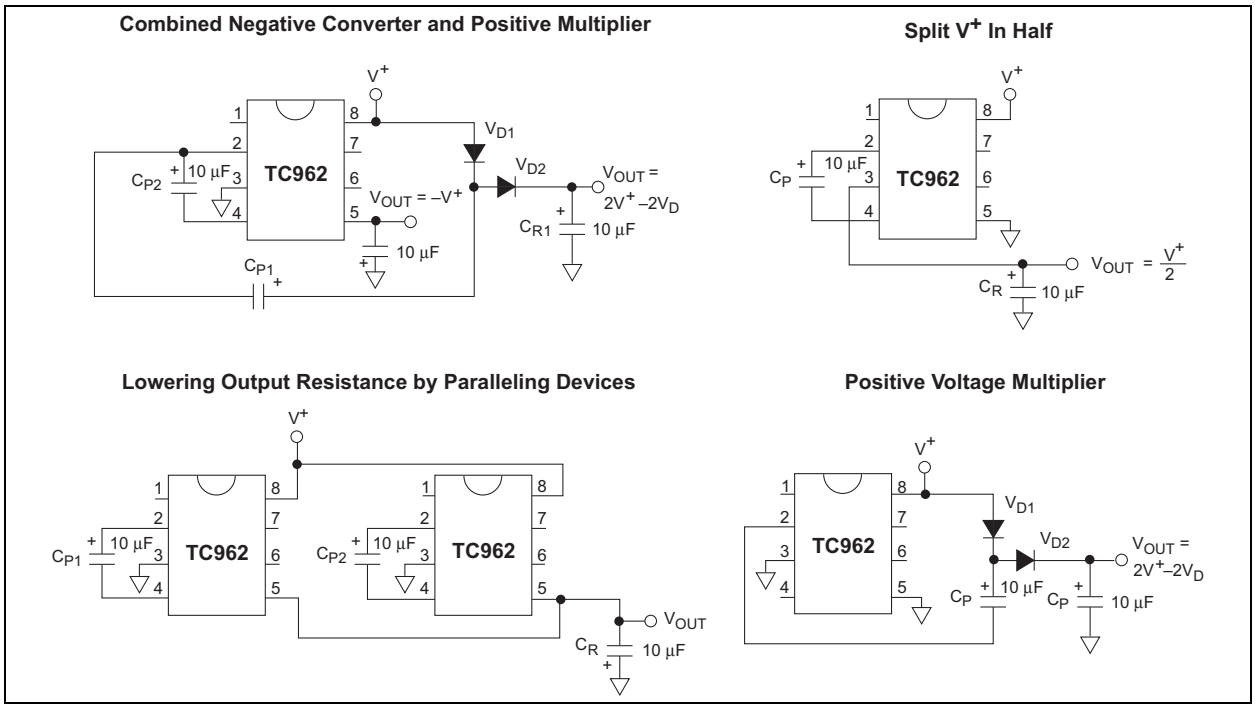


FIGURE 3-2: *Typical Applications.*

4.0 TYPICAL CHARACTERISTICS

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and, therefore, outside the warranted range.

The test circuit is shown in Figure 3-1, $C_P = C_R = 10\ \mu F$, $C_{PESR} \approx C_{RESR} \approx 1\Omega$.

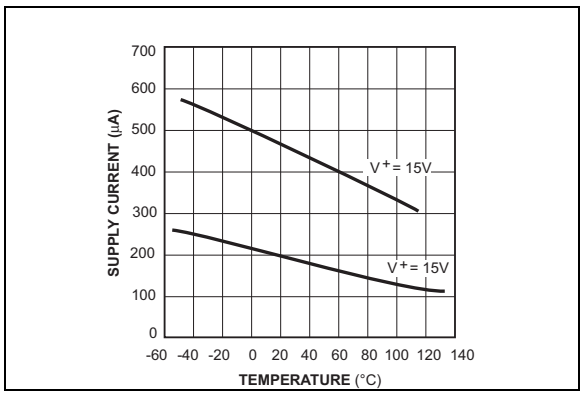


FIGURE 4-1: *Supply Current vs. Temperature.*

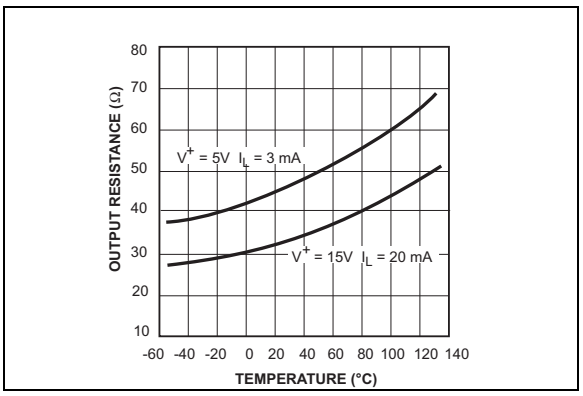


FIGURE 4-4: *Output Resistance vs. Temperature.*

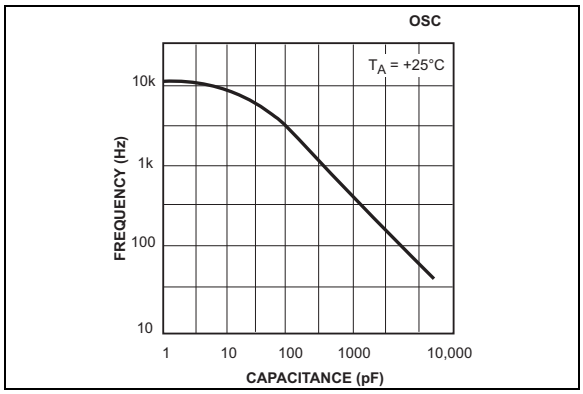


FIGURE 4-2: *Oscillator Frequency vs. C_{OSC}.*

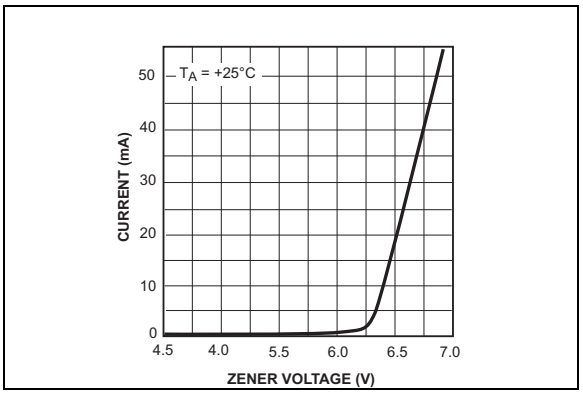


FIGURE 4-5: *Current vs. Zener Voltage.*

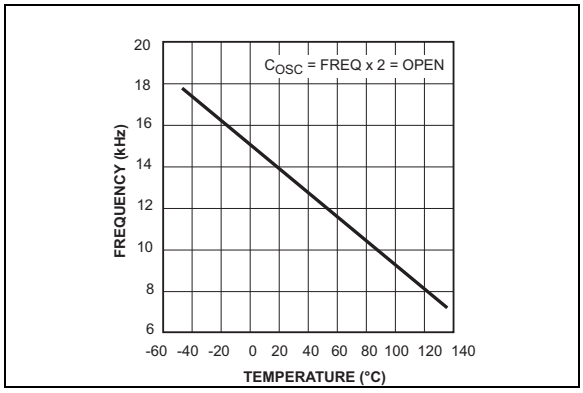


FIGURE 4-3: *Frequency vs. Temperature.*

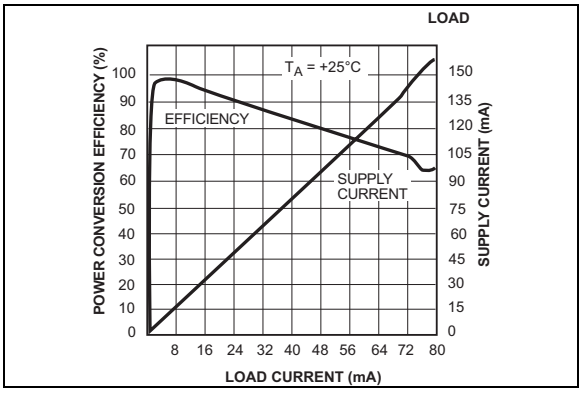


FIGURE 4-6: *Power Conversion Efficiency vs. I_{LOAD}.*

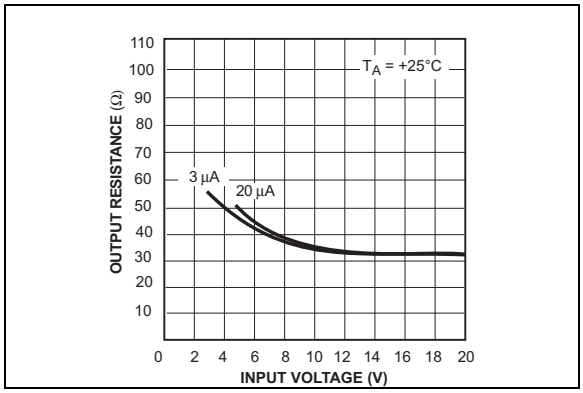
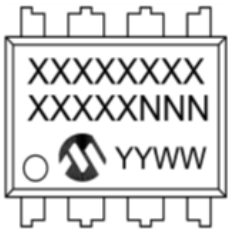


FIGURE 4-7: *Output Resistance vs. Input Voltage.*

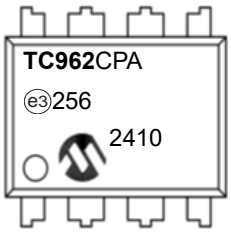
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

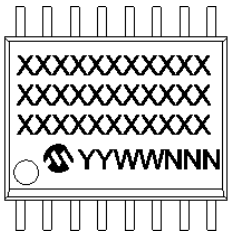
8-Lead PDIP



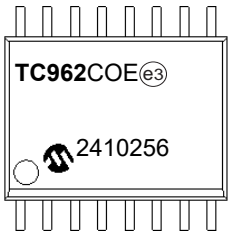
Example:



19-Lead SOIC



Example:

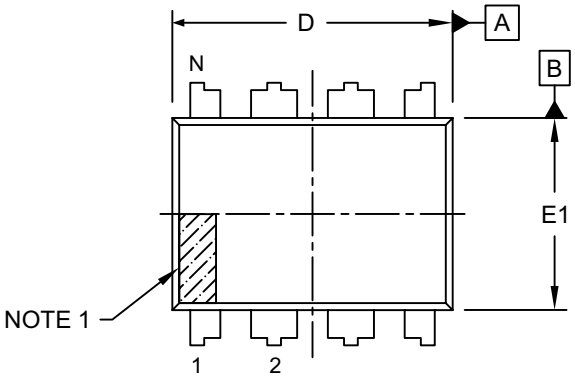


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

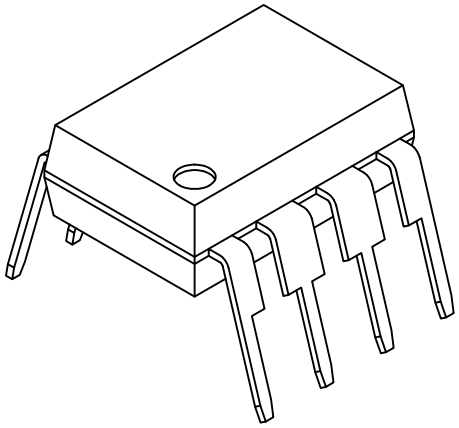
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. The package may or not include the corporate logo.

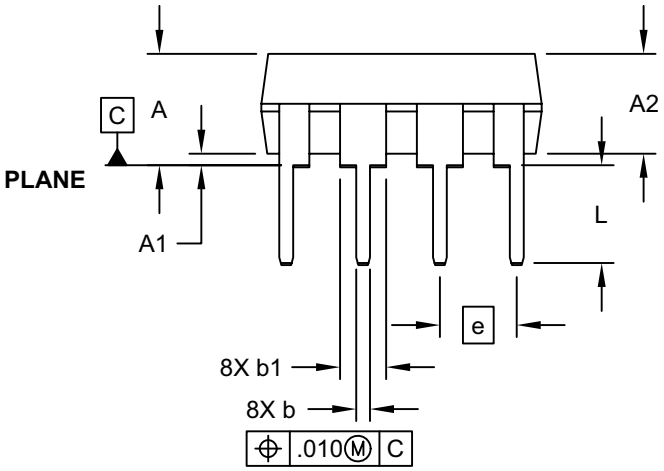
8-Lead Plastic Dual In-Line (C4X) - 300 mil Body [PDIP]
Atmel Legacy Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

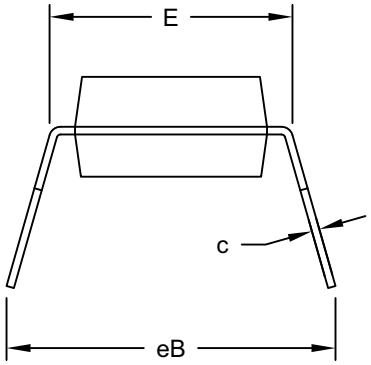


TOP VIEW





SIDE VIEW

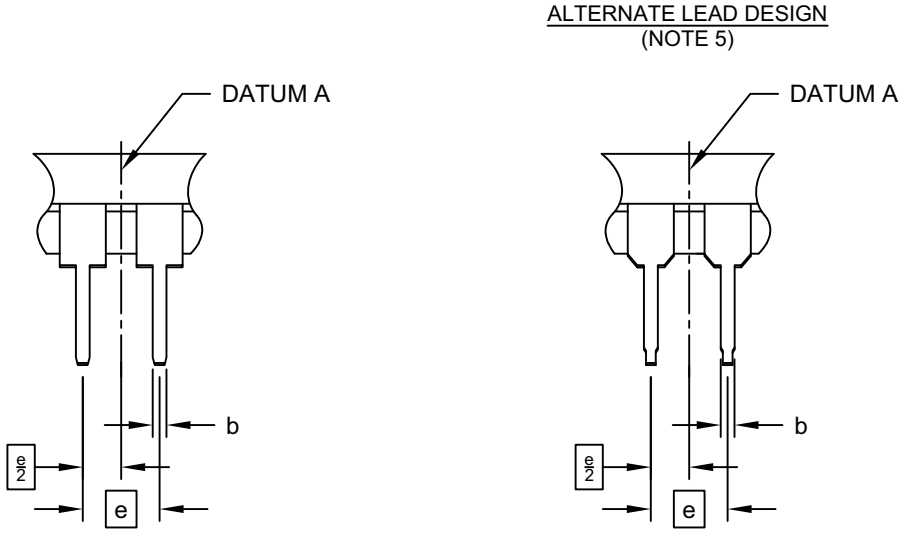


END VIEW

Microchip Technology Drawing No. C04-018-C4X Rev G Sheet 1 of 2

8-Lead Plastic Dual In-Line (C4X) - 300 mil Body [PDIP]
Atmel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

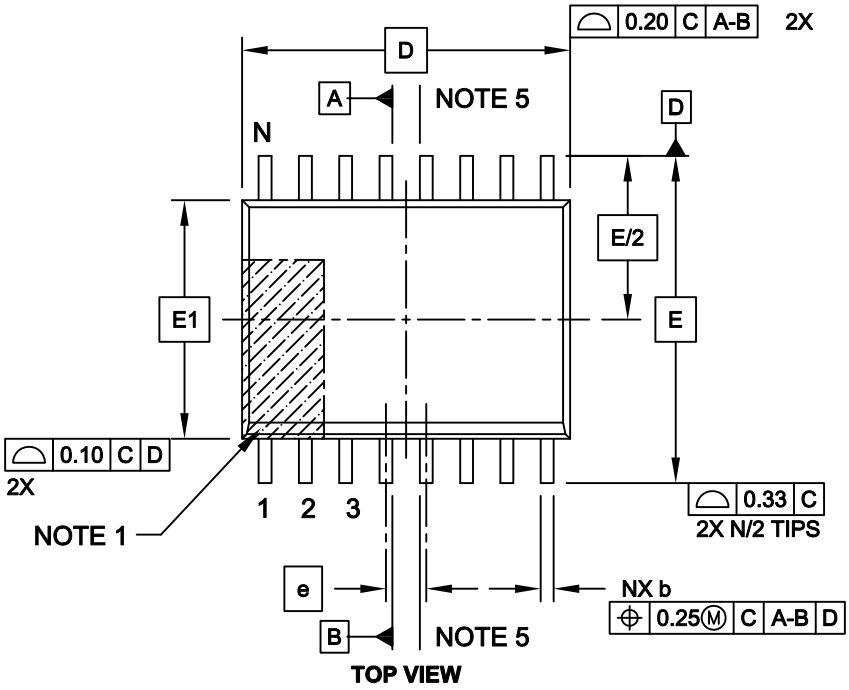
Notes:

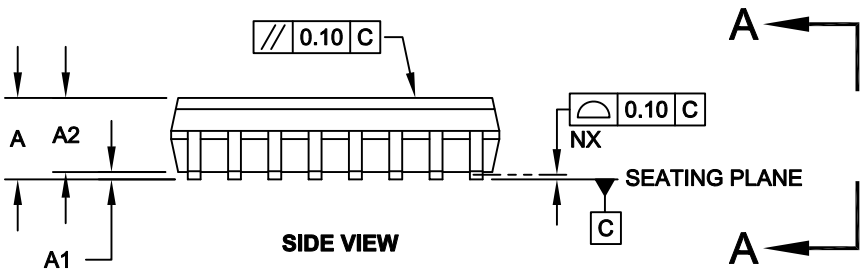
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

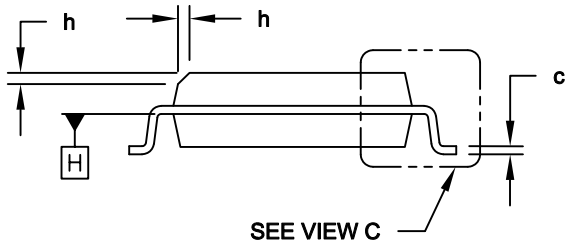
Microchip Technology Drawing No. C04-018-C4X Rev G Sheet 2 of 2

16-Lead Plastic Small Outline (OE) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





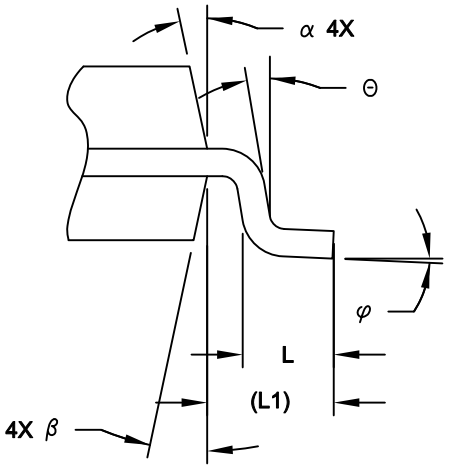


VIEW A-A

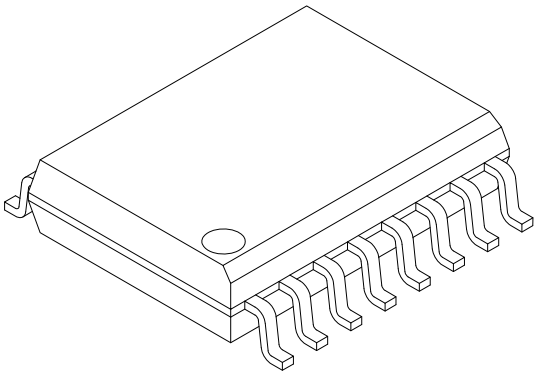
Microchip Technology Drawing C04-102C Sheet 1 of 2

16-Lead Plastic Small Outline (OE) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		10.30 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

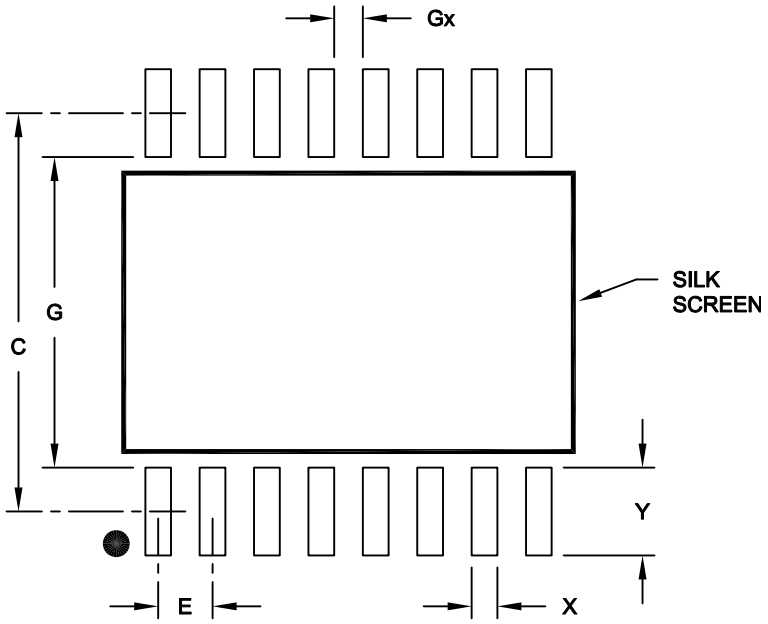
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-102C Sheet 2 of 2

16-Lead Plastic Small Outline (OE) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.30	
Contact Pad Width	X			0.60
Contact Pad Length	Y			2.05
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.25		

Notes:

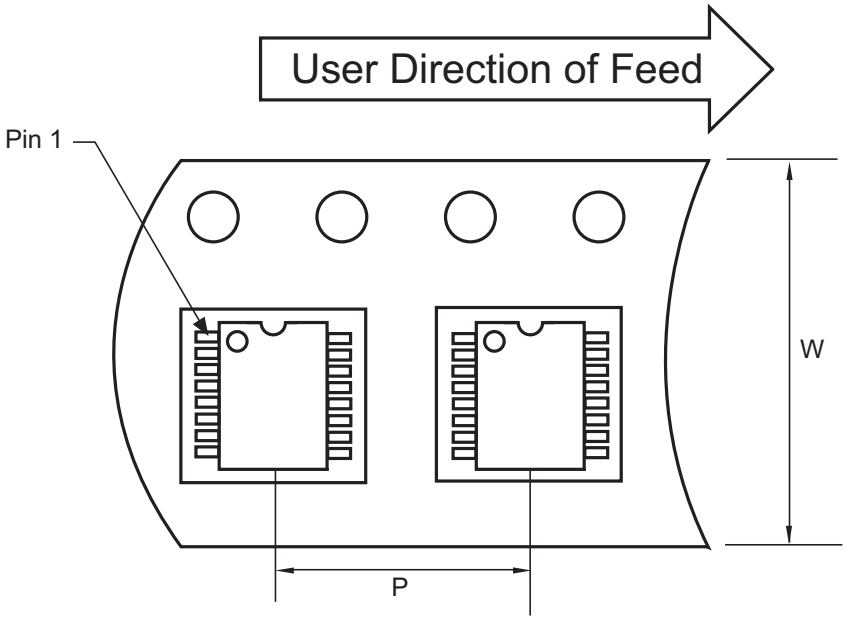
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2102A

5.2 Taping Form

Component Taping Orientation for 16-Pin SOIC (Wide) Devices



Standard Reel Component Orientation
for 713 Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
16-Pin SOIC (W)	16 mm	12 mm	1000	13 in

APPENDIX A: REVISION HISTORY

Revision E (March 2025)

- Removed all mentions of CERDIP package.
- Updated General Description to better describe the part.
- Added Note 2 to TC962 Electrical Specifications.
- Updated **Section 5.0 "Packaging Information"** with current laser marking examples and drawings.
- Updated document layout.

Revision D (December 2012)

- Added a note to each package outline drawing.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XXX
Device	Temperature Range	Package	Tape and Reel

Device:	TC962:	High Current Charge Pump DC-to-DC Converter
Temperature Range:	C	= 0°C to +70°C (Commercial)
	E	= -40°C to +85°C (Extended)
Package:	PA	= Plastic Dual-in-line Package, PDIP, 8 Lead
	OE	= Plastic Small Outline Package, SOIC, 16-Lead
Tape and Reel Option(1):	(Blank)	= Standard packaging (PDIP: 60/tube, SOIC: 47/Tube)
	713	= Tape and Reel[1] (1000/reel, SOIC package only)

Examples:

a) TC962CPA: High Current Charge Pump DC-to-DC Converter, Commercial Temperature, 8L PDIP, Standard Packaging

b) TC962EPA: High Current Charge Pump DC-to-DC Converter, Extended Temperature, 8L PDIP, Standard Packaging

c) TC962COE: High Current Charge Pump DC-to-DC Converter, Commercial Temperature, 16L SOIC, Standard Packaging

d) TC962COE713: High Current Charge Pump DC-to-DC Converter, Commercial Temperature, 16L SOIC, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legalinformation/microchip-trademarks.

ISBN: 979-8-3371-0760-8

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.