

User Guide
SparX-III PoE/PoE+ Reference Design



a  **MICROCHIP** company

Contents

1	Revision History	1
1.1	Revision 1.0	1
2	Introduction	2
3	Quick Start	3
4	PoE and PoE+ Overview	4
4.1	PoE	4
4.2	PoE+	4
5	SparX-III PoE/PoE+ Reference Design	5
5.1	Hardware Design	5
5.1.1	Evaluation Board	5
5.1.2	PoE/PoE+ Modules	5
5.1.3	Design Considerations	5
5.2	Software Design	6
5.2.1	Command Line Interface (CLI)	6
5.2.2	Web GUI	7

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in July 2010. It is the first publication of this document.

2 Introduction

Power over Ethernet (PoE) and Power over Ethernet Plus (PoE+) are two methods of supplying power to network devices via Ethernet LAN cables. Power is injected on the Ethernet cable along with data by Power Sourcing Equipment (PSE), and a Powered Device (PD) receives power and data over the Ethernet cable without using electrical outlets for power.

This document provides a brief description of PoE/PoE+, as well as an overview of the Vitesse SparX-III™ PoE/PoE+ reference design (PSE) with design considerations.

3 Quick Start

The following basic steps provide a brief overview of how to prepare the Vitesse SparX- III equipped PoE/PoE+ system for operation. Additional details are provided in the following sections.

1. Plug the PoE/PoE+ module into the SparX-III managed reference board
2. Ensure that the power supply of the reference board and PoE/PoE+ module are both connected and turned on
3. Click the PoE Management link on the web GUI interface after the system powers up.
4. Fill in the power value for the primary power supply and save it
5. Plug a PD into a powered port

4 PoE and PoE+ Overview

This section describes the PoE and PoE+ overview.

4.1 PoE

The IEEE802.3af standard specifies how power should be distributed over Ethernet LAN cables. It eliminates the need to have separate Ethernet LAN cables for data and electrical outlets for power. Considering the worst case power loss in the cable between PSE and PD, the PSE can provide up to 15.4 W of power at 48 V and the PD can use no more than 12.95 W under IEEE 802.3af. Five PD classes specify the maximum power level output at the PSE side.

4.2 PoE+

Due to the need for higher power required by a newer generation of network devices, PoE+ (IEEE 802.3at) can provide up to 30 W of power at the PSE and the PD can draw up to 25.5 W of power. In addition, the IEEE 802.3at standard provides a more flexible Layer 2 power classification method based on Link Layer Discovery Protocol (LLDP). The main benefit of LLDP is providing power allocation of 0.1 W granularity along with the ability to dynamically reallocate power, for improved power allocation and management between the PSE and PD.

Additionally, IEEE 802.3at allows both 2P and 4P solutions. 2P solutions transfer power through 2 pairs in the UTP cable (as does legacy 802.3af/PoE solutions), while 4P solutions use all four pairs in the UTP cable for power transfer (simply doubles the power). The current Vitesse reference design focuses on 2P solutions as the most commercially available 802.3at/PoE+ PSE controllers and PoE+ compatible magnetics do.

5 SparX-III PoE/PoE+ Reference Design

This section describes the hardware and software designs associated with the Vitesse SparX-III PoE/PoE+ (PSE) turn-key solution.

5.1 Hardware Design

The SparX-III is available as managed (VSC5610EV, 26-port managed) and unmanaged (VSC5609EV, 25-port unmanaged) switch evaluation boards. Only the managed switch evaluation board is able to support the function of PoE/PoE+ as the PSE powering PD devices on all switch ports.

5.1.1 Evaluation Board

In order to provide a reference design which pairs the SparX-III switch family with as many different PoE/PoE+ controllers as possible, three connectors are used on the VSC5610EV evaluation board.

- J24 and J25 are the pins connected to the center tap of the magnetics for total 24 ports PoE/PoE+ classification/power feeding.
- J23 contains the low-bandwidth control interfaces including SPI and I2C signals. Furthermore, the power up reset for PoE/PoE+ controllers and one interrupt pin of the VCore-III CPU are also available from J23.

The power supply for PoE/PoE+ is designed to directly connect with the PoE/PoE+ module and not the switch main board since the VSC5610EV could function as a switch reference board without the PoE/PoE+ module.

5.1.2 PoE/PoE+ Modules

Currently there are three PoE/PoE+ controller vendors who provide PoE/PoE+ modules for SparX-III reference board firmware/software development and testing purposes.

The following table lists the company names and contact information.

Table 1 • PoE/PoE+ Controller Vendors

Company Name	Contact Information
Microsemi Corp.	www.microsemi.com
Silicon Laboratories, Inc.	www.silabs.com
Texas Instruments	www.ti.com

5.1.3 Design Considerations

IEEE802.3at specifies that the maximum current is 600 mA per channel. 600 mA is considerably more than a typical 0.1 mm wide trace on ½ Oz copper foil can handle, so care must be taken not to design a PCB trace that will inadvertently act as a fuse. In addition, insulation is required in order to pass Hi-Port testing. The following describes how the SparX-III reference board addresses these two requirements.

5.1.3.1 PCB Trace/Copper Foil Thickness for Maximum Power

The maximum current that a PCB trace can carry depends mainly on operating temperature range, allowed temperature rise, PCB trace width, copper foil thickness, whether the trace is placed on an outer or inner layer (an outer layer trace can more easily transfer heat to ambient air), and on surrounding parts which might act as heat sources, for example. The maximum carrying current of a PCB trace can be calculated according to the IPC-2221 specification. Some typical trace designs are listed in the table below (see the actual IPC-2221 specification for the most current recommendations).

On the SparX-III reference board, the PCB traces connecting the PoE/PoE+ module to the center tap pins of integrated magnetics are placed on the top layer and are 0.75 mm wide on a ½ oz copper foil. This is quite conservative, resulting in a calculated temperature rise of less than 3 °C at a current of 650 mA. If the PCB space in a customer's design is limited, 1 oz copper foil could be considered, resulting in a power trace width of around 0.4 mm. Properly-sized power traces will help provide adequate design margin.

The following table lists few typical trace designs from IPC-2221.

Table 2 • Some Typical Trace Designs from IPC-2221

Temperature	Temperature Rise	Trace Width	Copper Foil Thickness	Outer/Inner	Maximum Current
50 °C	5 °C	0.4 mm	18 μ / ½ oz	Outer	650 mA
50 °C	15 °C	0.2 mm	18 μ / ½ oz	Outer	660 mA
50 °C	2 °C	0.4 mm	35 μ / 1 oz	Outer	600 mA
50 °C	2 °C	0.45 mm	35 μ / 1 oz	Outer	650 mA
50 °C	5 °C	1.8 mm	18 μ / 1 oz	Inner	640 mA
50 °C	15 °C	0.8 mm	18 μ / 1 oz	Inner	640 mA
50 °C	5 °C	0.9 mm	35 μ / 1 oz	Inner	630 mA
50 °C	15 °C	0.4 mm	35 μ / 1 oz	Inner	630 mA

5.1.3.2 Insulation

For standard FR-4 PCB material, 2 kV isolation is achieved by a clearance of 2 mm on outer layers and a clearance of 0.1 mm on inner layers (note, this applies also layer- to-layer, but most laminates are > 0.1 mm thick). The difference between outer layers and inner layers is caused by the fact that on outer layers a high voltage arc can travel through the air from one exposed copper pad to another, whereas on inner layers the arc has to travel through the FR-4 material with a voltage rating of, for example, 1 kV/mil.

On the SparX-III reference board the PCB traces connecting the PoE/PoE+ module to the center tap pins of the integrated magnetics are placed on the top layer with a clearance to other net classes (that is, other signals, ground) of at least 2 mm. The 1000BASE-T signals are placed in an inner layer with a clearance to the PoE+ center tap signals (for example, the center tap pins of the integrated magnetics) of at least 0.1 mm. The integrated magnetics part is used so that clearance from the PoE+ center tap pins to the 1000BASE-T signal pins is > 2 mm. As a result the physical distance from the PoE+ center tap pins and PCB traces placed on the top layer is > 2 mm to achieve this insulation.

5.2 Software Design

The PoE/PoE+ software solution is designed for the managed reference system (VSC5610EV, 26 ports switches). Both a CLI (command line interface) and Web GUI are provided to configure the PoE/PoE+ features such as priority setup, power allocation on each port, power management method and to enable PoE+ link layer management capability.

5.2.1 Command Line Interface (CLI)

The available commands are as follows.

- PoE Configuration [<port_list>]
- PoE Mode [<port_list>] [disabled|poe|poe++]
- PoE Priority [<port_list>] [low|high|critical]
- PoE Mgmt_mode [class_con|class_res|al_con|al_res|lldp_res|lldp_con]
- PoE Maximum_Power [<port_list>] [<port_power>]
- PoE Status
- PoE Primary_Supply [<supply_power>]
- PoE Backup_Supply [<supply_power>]

5.2.2 Web GUI

The PoE Management Web GUI features are described in the sections below. See [Figure 1](#) for an image of this GUI.

5.2.2.1 Reserved Power Modes

There are three modes for configuring how the ports/PDs may reserve power.

1. **Allocated Mode:** The user allocates the amount of power that each port may reserve. The allocated/reserved power for each port/PD is specified in the Maximum Power fields.
2. **Class Mode:** Each port automatically determines how much power to reserve according to the class the connected PD belongs to, and reserves the power accordingly. Three different port classes exist and one for 4 W, 7 W, and 15.4 W.

Note: In this mode, the Maximum Power fields have no effect.

3. **LLDP-MED Mode:** This mode is similar to the Class mode except that each port determines the amount of power it reserves by exchanging PoE information using the LLDP protocol and reserves power accordingly. If no LLDP information is available for a port, the port will reserve power using the class mode.

Note: In this mode the Maximum Power fields have no effect.

For all modes: If a port uses more power than the reserved power for the port, the port is shut down.

5.2.2.2 Power Management Mode

There are two modes for configuring when the ports are shut down.

1. **Actual Consumption:** In this mode the ports are shut down when the actual power consumption for all ports exceeds the amount of power that the power supply can deliver, or if the actual power consumption for a given port exceeds the reserved power for that port. The ports are shut down according to the ports' priority. If two ports have the same priority then the port with the highest port number is shut down.
2. **Reserved Power:** In this mode the ports are shut down when total reserved powered exceeds the amount of power that the power supply can deliver. In this mode the port power is not turned on if the PD requests more power than available from the power supply.

5.2.2.3 Power Supply Configuration

The switch can have two PoE power supplies. One is used as a primary power source, and the other as a backup power source. In case the primary power source fails, the backup power source will take over. In order to determine the amount of power the PD may use, it must be defined what amount of power the primary and backup power sources can deliver.

5.2.2.4 Ethernet Port Configuration

- **PoE Mode**
The PoE Mode represents the PoE operating mode for the port.
 - Disabled: PoE disabled for the port.
 - PoE: Enables PoE IEEE 802.3af (Class 4 PDs limited to 15.4 W)
 - PoE++: Enables PoE++ IEEE 802.3at (Class 4 PDs limited to 30 W)
- **Priority**
Priority represents the ports priority. There are three levels of power priority: Low, High and Critical. The priority is used in the case where the remote devices require more power than the power supply can deliver. In this case the port with the lowest priority will be turned off starting from the port with the highest port number.

- Maximum Power
The maximum power value contains a numerical value that indicates the maximum power in watts that can be delivered to a remote device.
The maximum allowed value is 30 W.

The following figure illustrates the PoE management GUI image.

Figure 1 • POE_Management_GUI

Power Over Ethernet Configuration

Reserved Power determined by	☒ Class	☐ Allocation	☐ LLDP-MED
Power Management Mode	☐ Actual Consumption	☒ Reserved Power	

Primary Power Supply [W]	Backup Power Supply [W]
100	100

Port	PoE Mode	Priority	Maximum Power [W]
1	PoE	Low	15.4
2	PoE	Low	15.4
3	PoE	Low	15.4
4	PoE	Low	15.4
5	PoE	Low	15.4
6	PoE	Low	15.4
7	PoE	Low	15.4
8	PoE	Low	15.4
9	PoE	Low	15.4
10	PoE	Low	15.4
11	PoE	Low	15.4
12	PoE	Low	15.4
13	PoE	Low	15.4
14	PoE	Low	15.4
15	PoE	Low	15.4
16	PoE	Low	15.4
17	PoE	Low	15.4
18	PoE	Low	15.4
19	PoE	Low	15.4
20	PoE	Low	15.4
21	PoE	Low	15.4
22	PoE	Low	15.4
23	PoE	Low	15.4
24	PoE	Low	15.4

Save

Reset

**Microsemi Headquarters**

One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Sales: +1 (949) 380-6136

Fax: +1 (949) 215-4996

Email: sales.support@microsemi.com

www.microsemi.com

© 2010 Microsemi. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions; setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

VPPD-02635