
How to Optimize the BOM of a SAMA5D3-based System

ARM-based Embedded MPU

Scope

Based on the ARM® Cortex®-A5 processor, the Atmel® SAMA5D3 series of embedded microprocessor units (eMPUs) is a high-performance, low-power platform operating at up to 536 MHz. The BOM cost is a key parameter for most industrial and consumer applications. This application note describes some considerations for selecting optimal components for a SAMA5D3-based system.

A system based on an eMPU requires several basic parts such as:

- Power management units: DC to DC converter (DCDC), Low-dropout regulator (LDO) or Power Management IC (PMIC) and power filtering
- Clock sources: slow clock and main clock
- Main memory: DDR2 or LPDDR2
- Boot and storage memory: NAND Flash, NOR Flash, EEPROM, SD/eMMC
- Ethernet interfacing: 100BASE-M or 1000BASE -M

Reference Documents

Type	Reference Documentation
Datasheet	SAMA5D3 Series Datasheet

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1. Power Management

1.1 SAMA5D3 Power Supply Requirement and Type

The SAMA5D3 series needs different power domains that can be grouped in two main categories: “big” consumers that have a high power consumption rate and “small” consumers that have a low power consumption rate.

Rails with high power consumption:

- VDDCORE: 1.2 V, used to power the processor core, the internal memory and the peripherals. The current consumption is normally about 100 mA and depends on the application.
- VDDIODDR: 1.8 V in the case of LPDDR1/DDR2 or 1.2 V in the case of LPDDR2. The total current consumption is about several hundred milliamperes for an internal memory controller and external memory chips. The current value depends on the memory type and on the operation frequency.
- VDDIOM: used for memory interface of static memory and NAND Flash; there are two power levels: 1.8 V and 3.3 V. The current consumption is normally low (within 100 mA).
- VDDIOP0, VDDIOP1: used for some GPIO peripheral pins like LCD, GMAC, MCI, SPI, etc. The voltage range is from 1.65 V to 3.6 V. The maximum rating current on all I/O lines is about 350 mA, but in-application current consumption is much lower than this maximum rating.

Rails with low power consumption:

- VDDPLLA: 1.2 V, used for PLLA cells.
- VDDOSC: 1.65-3.6 V, used for main oscillator cells.
- VDDBU: 1.65-3.6 V, used for slow clock oscillators and parts of the system controller; the power consumption is very low.
- VDDUTMIC: 1.2 V, used for USB cores and PLLs.
- VDDUTMII: 3.3 V, used for USB interfaces.
- VDDANA: 3.3 V, used for ADCs.

1.2 DCDC/LDO Power Scheme and Considerations

This power scheme is composed of several DCDCs and/or LDOs to supply each power rail separately.

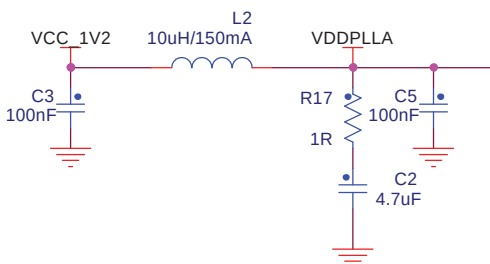
The advantage is that the thermal dissipation is good and, for each power component, the rail can be placed in different board locations, which offers a better flexibility from a layout point of view.

The disadvantage is that the PCB size is larger and the timing management of the different power rails is more complex.

The following are some design considerations on this scheme:

- Considering the power efficiency of the 1.2V and 1.8V power rails on the board for VDDCORE and VDDIODDR, it is recommended to use DCDC if the input power supply is 5V or above; if there is a 3.3V power rail with a sufficient sourcing capacity in the system, then an LDO can be used to generate these power rails from the 3.3V input.
- If some sensitive power rails like VDDPLLA, VDDOSC and VDDUTMIC share the source with other power rails, it is recommended to add a power filter to isolate the high-frequency noise. [Figure 1-1](#) provides an example.

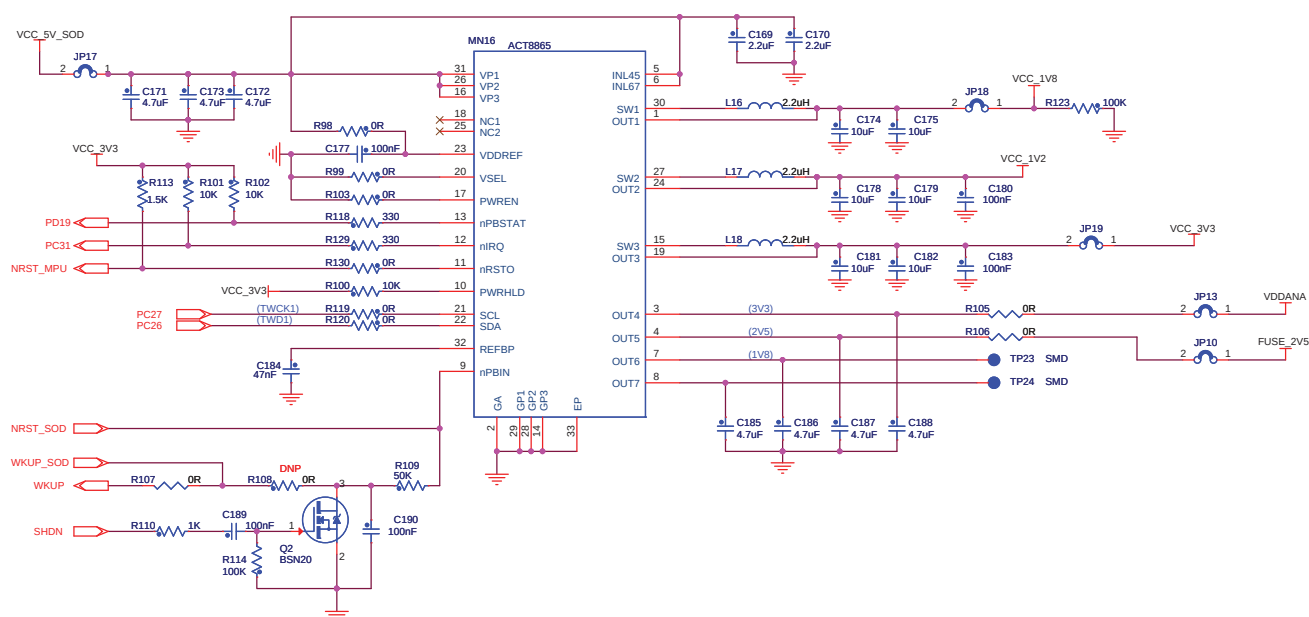
Figure 1-1. Power Filter



1.3 PMIC Power Scheme and Considerations

The PMIC power scheme uses a single IC to manage all power rails and their sequence for the whole system. The PMIC usually integrates several DCDCs and LDOs in one chip and users just need to add some necessary external components such as inductors, capacitors and resistors. [Figure 1-2](#) provides an example of a schematic featuring a PMIC.

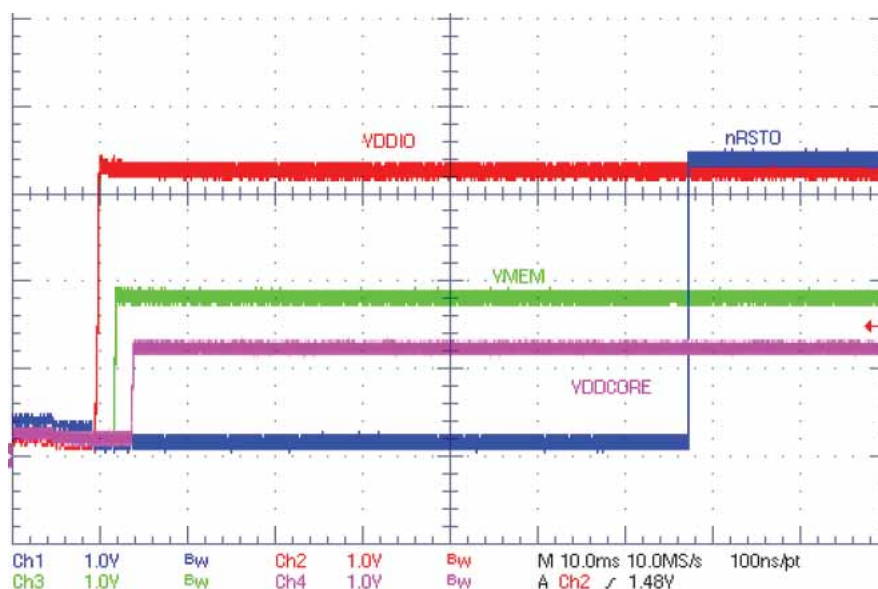
Figure 1-2. PMIC Power Scheme



The advantages of the PMIC power scheme are:

- The integration of all DCDCs and LDOs into one chip, saving PCB space and offering a very cost-effective solution;
- The support of a TWI interface to easily manage the power sequence;
- The ability to manage the sequence of each power rail and reset signal by the PMIC logic to meet the requirements of the MPU. [Figure 1-3](#) shows a power-on sequence generated by a PMIC.

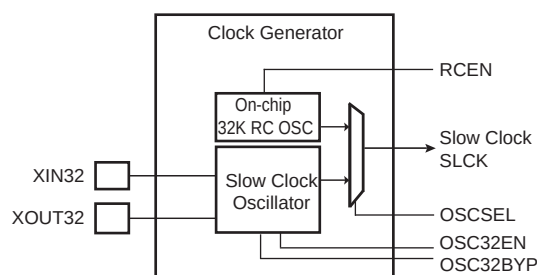
Figure 1-3. Power-on Sequence Generated by a PMIC



2. Clock Sources

2.1 Slow Clock

Figure 2-1. Slow Clock Diagram

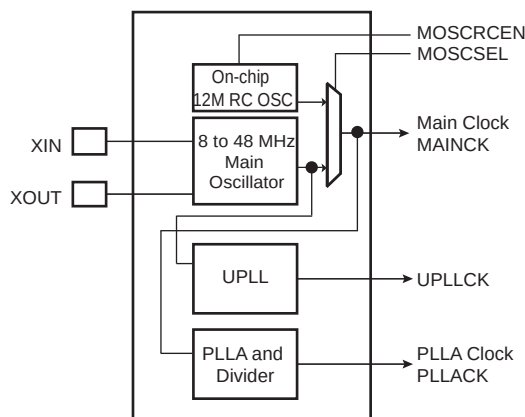


The slow clock is used for the internal real-time clock (RTC), the watchdog timer and the reset controller. Three different methods are available to generate the slow clock:

- Using an internal on-chip 32-kHz RC oscillator. This method does not need the addition of external components but the accuracy is low. However, if this low accuracy is acceptable in the user's system, then this method saves both cost and PCB size.
- Using an external crystal with the internal slow clock oscillator. This method needs a 32-kHz crystal and two load capacitors, which ensures a high accuracy of the clock at normal temperature.
- Setting the internal slow clock oscillator in by-pass mode. Then XIN32 (slow clock oscillator input) can be connected to the output of a high-quality clock generator with temperature compensation.

2.2 Main Clock

Figure 2-2. Main Clock Diagram



The main clock can be used to feed the PLLA and UTMI PLL (UPLL) blocks and to generate the processor clock, the DDR2 clock and the other peripheral clocks. The user can select either the 12-MHz fast RC oscillator or the crystal oscillator as the main clock source.

The advantages of the 12-MHz fast RC oscillator are as follows:

- fast startup time.
- no need for any external components.
- selected by default to start up the system.
- can be used for continuous operation in a low-cost/ low-accuracy solution.

However, in most cases, including in USB high-speed operations, a high-accuracy solution is required for a continuous operation. Two methods are available to implement it:

- Connect a 3-20 MHz crystal and its load capacitors to the on-chip oscillator, which provides a high accuracy over a normal temperature range.
- Connect an external oscillator clock output to XIN (main oscillator input) and set the internal oscillator in by-pass mode. Using an oscillator with temperature compensation can provide a high accuracy level over a wide temperature range.

3. Main Memory

The SAMA5D3 series supports several types of dynamic RAM including DDR2, LPDDR2 and LPDDR1. The maximum address space is 512 MB. It supports a 32-bit memory data bus width, a maximum row number of 16 K, and up to eight banks. For example, the user can select two chips of 128 MB with a 16-bit data width to achieve the maximum address space and a total memory capacity of 4 Gbits.

For each type of DDR, the higher the density of a single chip is, the higher the price per bit is. For example, the price of four 1-Gbit DDR2 chips is lower than that of two 2-Gbit DDR2 chips.

4. Boot Memory

In standard Boot mode, when BMS is tied to 0 at reset, the SAMA5D3 boots from an external parallel interface with the Static Memory Controller at address 0x0 on EBI CS0. These types of memories are usually expensive, such as parallel NOR Flash, EEPROM, etc.

When BMS is tied to 1 at reset, the ROM code in SAMA5D3 runs and attempts to detect valid code from external non-volatile memories such as SPI data Flash, SD/eMMC, NAND Flash and TWI EEPROM.

To select the external memory, the user can take into account the following considerations:

- Generally, NAND Flash devices have higher memory capacity and are cheaper than comparable EEPROM and NOR Flash. However, due to bit-flipping issues, the NAND Flash requires an extra error management bit. Moreover, the NAND Flash must be accessed sequentially.
- EEPROM and NOR Flash have up to 10% fewer bit-flipping issues than NAND Flash and can be accessed randomly.

5. Ethernet Interfacing

The SAMA5D33/D34/D35 devices have an on-chip Gigabit Ethernet MAC that supports 10/100/1000 Mbps Ethernet compatible with the IEEE 802.3 standard. They also support several interface types: MII, GMII and RGMII.

If the system requires a speed of 1000 Mbps, then users must select a Gigabit Ethernet PHY to connect with the GMII or RGMII interface. If the system only requires a speed of 10Mbps or 100Mbps, then users can select a 10BASE-M/100BASE-M Ethernet PHY to connect with the MII interface, which is a more cost-efficient solution.

6. Conclusion

The Atmel SAMA5D3 devices offer a design flexibility that enable multiple choices for the different components of a system. This application note helps users choose a sound and cost-efficient solution for BOMs.

7. Revision History

Table 7-1. How to Optimize the BOM of a SAMA5D3 Rev. 11256A 16-Dec-13

Doc. Rev	Changes
11256A	First issue.



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