

## **Emulating High-Endurance Data EEPROM for PIC10 and PIC12**

Author: Willem J. Smit

Microchip Technology Inc.

#### INTRODUCTION

Given Microchip's growing portfolio of microcontrollers, it is self-evident that no two families of microcontrollers are exactly similar in features and specifications. One such feature that is available on select microcontrollers is the ability for users to internally store user data in a nonvolatile manner, such as on internal EEPROM. In order to provide a low-cost solution, some devices exclude internal EEPROM but have the capability to read and write Flash Program Memory (FPM) using self-read/write. This feature allows users to write and read user data to and from any unused portion of FPM in a nonvolatile manner.

It is important to note a few things about FPM to better understand the structures set in place for erase and programming operations.

First, FPM is arranged in rows that consist of a fixed number of 14-bit program memory words. For example, on the PIC10F322, the FPM is broken down into rows consisting of sixteen 14-bit words, which are accessible by an address of XX0h to XXFh.

Second, the FPM can only be erased by a minimum of a row at a time. When erased, the contents are set to all '1's. When writing, only '0's can be written.

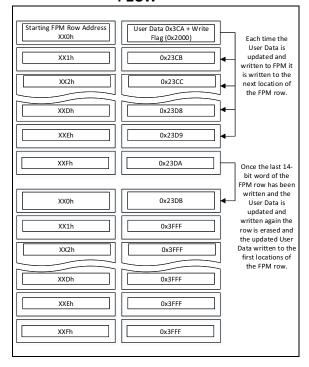
Third, again using the PIC10F322 as an example, Microchip specifies the minimum program Flash memory cell endurance to be 10K erase and write cycles from -40°C to +85°C. Considering each memory cell as 1-bit in the 14-bit FPM word, this application note introduces software library routines, which increase the minimum program FPM cell endurance to a theoretical minimum 160K erase and write cycles, when storing user data in the FPM in rolling-page format (10K FPM cell endurance x 16 rows = 160K FPM cell endurance). Thus, the FPM is brought into the high-endurance range, which is specified as a minimum of 100K erase and write cycles.

#### **OVERVIEW**

The supplied software library makes use of a minimum of one row of FPM to store one 12-bit user data value, which is continually updated, requiring a minimum endurance greater than 10K erase and write cycles.

The increased endurance is achieved by incrementing the location of the 12-bit user data by one FPM address location in the row each time a write takes place. Once all sixteen locations within the row have been filled and a new value written, the row is erased and the new value is written to the first 14-bit word location of the same row.

FIGURE 1: ONE ROW OF FPM
HIGH-ENDURANCE WRITE
FLOW



#### **IMPLEMENTATION DETAILS**

The software library consists of one main function routine:

 uint16\_t ReadWrite\_HEFlash(uint8\_t rw, uint16\_t data, uint8\_t rowstartaddr)

The arguments for the above function are the following:

- "rw" designates if the function will perform a read of the FPM or a write to the FPM
- "rw" = 1 = Write to FPM
- "rw" = 0 = Read of FPM
- "data" is the 12-bit value written by the user
- "rowstartaddr" is the starting address of the FPM row being used. A row's starting address can be determined by looking at the first nibble starting with the LSB of the FPM addresses. The beginning row address always starting with the first nibble equal to 0x0. For example, 0xE0 to 0xEF is one row, with 0xE0 being the row start address.

This function writes and reads 12 bits of user data to and from the FPM. A write is done by writing the next available/open FPM location (bits <11:0>). Bits <13:12> are used as flags, indicating if a FPM row location has been written or not, as follows:

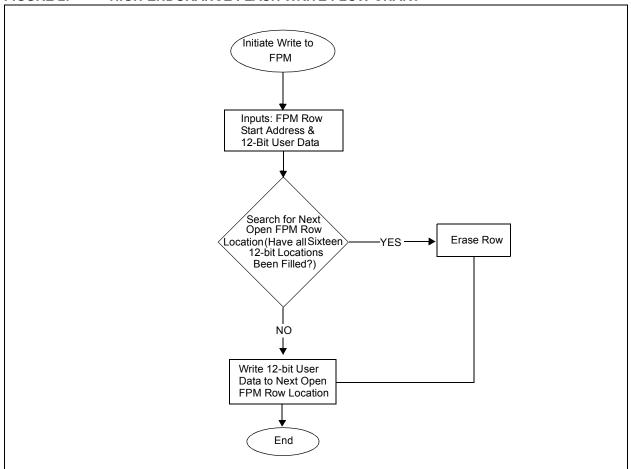
- Bits <13:12> = 0b11 = Open
- Bits <13:12> = 0b10 = Written (Closed)

Write example:

• ReadWrite HEFlash(1, 0x3CA, 0xF0)

The above function will write a value of 0x3CA to the next available/open FPM location within the row, which has a starting address of 0xF0 (see Figure 1 and Figure 2).

FIGURE 2: HIGH-ENDURANCE FLASH WRITE FLOW CHART



#### Read example:

 buffer = ReadWrite\_HEFlash(0, 0x000, 0xF0)

The above function will return the last 12-bits value of user data written to the selected FPM row and place the value in "buffer". In the case of a read, the "data" field is a "don't care" and will be ignored. If a read is performed and no user data has been written to the FPM, a value of 0xFFF will be returned (see Figure 3 and Figure 4).

FIGURE 3: ONE ROW OF FPM HIGH-ENDURANCE READ FLOW

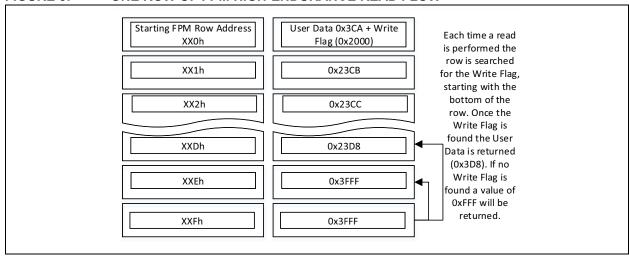
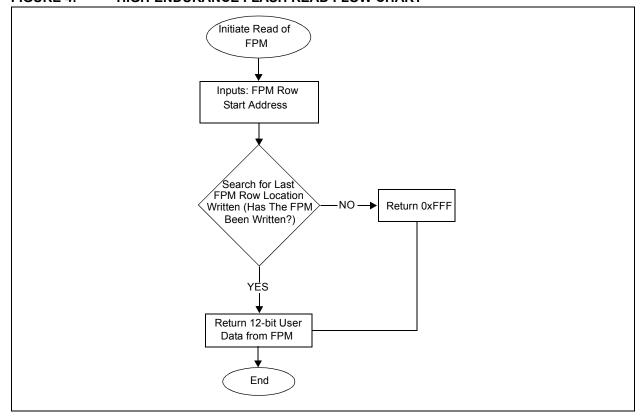


FIGURE 4: HIGH-ENDURANCE FLASH READ FLOW CHART



#### Selecting a Row

When selecting a row or rows to write, a few things should be noted:

- Never attempt to write to a section of FPM occupied by the firmware itself. In addition, areas where the Reset vector and Interrupt vector reside should always be avoided; these are usually located between FPM address 0x0000 and 0x0004.
- The best way to select an applicable row or rows is to look at the program memory map in MPLAB<sup>®</sup> X after doing a compile.

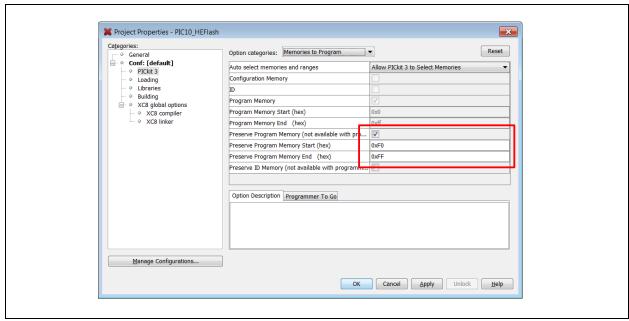
### Preserving FPM During Programming Cycles

During program cycles, via MPLAB X by default, the whole FPM on the device is erased. If a user requires user data already written to FPM to be preserved during the programming cycle in MPLAB X, this can be done in the following way:

- · Open Project Properties
- Select the programmer being used in the left hand column (e.g., PICkit™ 3, REAL ICE™, ICD3)
- Check the Preserve Program Memory box
- Enter the range of the rows selected for High-Endurance Flash Emulation in the Preserve Program Memory Start and Stop box

Figure 5 shows how to preserve FPM location 0x0F through 0xFF.





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#### EXAMPLE 1: PIC10\_PIC12\_EHEDEEPROM.C (EMULATING HIGH ENDURANCE DATA EPPROM)

```
uint16 t ReadWrite HEFlash (uint8 t rw,
uint16 t data, uint8 t rowstartaddr) {
       uint8 t addr;
       Save_INTERRUPT();
       if (rw == 1) {
         addr = rowstartaddr;
        } else {
         addr = (rowstartaddr + 0xF);
       uint8 t cnt;
        //CHECK FOR NEXT AVAILABLE WORD LOCATION
       for (cnt = 0x10; cnt != 0x0; cnt--) {
         Read FLASH(addr); //Read FLASH
        if (rw == 1) {//SEARCH FOR NEXT OPEN LOCATION
         if (PMDATH == 0x3F) { //IF NEXT ROW IS AVAILABLE
         PMDAT = data; //PLACE USER DATA IN PMDAT TO BE WRITTEN TO FLASH
         asm("bsf PMDATH, 5"); //SET FPM FREE FLAG (FPM LOCATION HAS BEEN WRITTEN)
         asm("bcf PMDATH, 4");
         Write FLASH(); //Write TO FLASH
         break;
        addr++;
        //CHECK IF THE ROW HAS EXPIRED
        if (cnt \leq 0x1) {
         //THE ROW HAS EXPIRED IT WILL NOW BE ERASED
         PMCON1 = 0b00010100; //CLEAR PM1CON & FREE = 1, WREN = 1
         PMADR = rowstartaddr;
         Unlock_FLASH();
         //Write USER DATA
         PMDAT = data; //PLACE USER DATA IN PMDAT TO BE WRITTEN TO FLASH
         asm("bsf PMDATH, 5");//SET FPM FREE FLAG (FPM LOCATION HAS BEEN WRITTEN)
         asm("bcf PMDATH, 4");
         Write FLASH(); //Write TO FLASH
      } else { //SEARCH FOR LAST WRITTEN LOCATION
        if ((PMDATH & 0x20) && (PMDATH != 0x3F)) {//CHECK FPM FREE FLAG
         data = (PMDAT & 0xfff); //RETURN DATA FROM LAST WRITTEN LOCATION
         break;
```

#### PIC10\_PIC12\_EHEDEEPROM.C (EMULATING HIGH ENDURANCE DATA EPPROM) (CONTINUED)

```
addr--;
      INTCON = SaveInt;
    }
    return data ;
void Save INTERRUPT(void) {
      SaveInt = INTCON; //save interrupt status
       GIE = 0; //Disable ints so required sequences will execute properly
void Read FLASH(uint8 t address) {
       PMADR = address;
       PMCON1 = 0b00000001; //RD = 1 Read PROGRAM FLASH
           while (RD);
      }
void Unlock FLASH(void) {
       PMCON2 = 0x55; //FLASH Write/ERASE Unlock SEQUENCE
       PMCON2 = 0xAA;
       WR = 1;
       while (WR);
       WREN = 0; //INHIBITS PROGRAMMING AND ERASING OF PROGRAM FLASH
void Write FLASH(void) {
       //PMCON1 = 0b00100100; //LOAD PROGRAM MEMORY Write LATCHES
       //Unlock FLASH();
       PMCON1 = 0b00000100; //Write PROGRAM Write LATCHES TO PROGRAM MEMORY
    Unlock_FLASH();
```

#### Interrupts

Special attention should be paid if interrupts are used in the application. When interrupts are being used in the main user code, "save\_INTERRUPT();" and "INTCON = SaveInt;" should be on uncommented in LPC\_HEFlash.C.

This will cause the device to disable all interrupts during read and write high-endurance FPM cycles, as well as saving the state of the INTCON register before a read or write cycle and restoring it afterwards. The interrupts are disabled to avoid an interrupt occurring during a read or write cycle and resulting in FPM data corruption.

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