Questions to ask when debugging I^{2}C and SPI interfaces to Microchip Timing Devices:

Applicable to both I^{2}C & SPI

1. Are the pins that determine device interface set correctly? (E.g. pins IF[1:0]=11 signifies SPI interface, other value signifies I2C)
2. Is this issue occurring on multiple devices and boards? If only on one board, it may be a device problem.
3. Can the ID registers be read correctly? Being able to do a simple read is a good early debug step.
4. Do the schematic and hardware match?
5. Are there noise issues? Is better decoupling needed?
6. Have the power-up sequence and reset-time specifications of the device been correctly followed?
7. Are the N/C, pull-ups, and pull-downs per the datasheet pin descriptions properly followed?
8. If writing to a device and the Data Read ≠ Data written or possibly Data Read = all 0xFF:
   Has there been enough time allowed for the device (e.g. EEPROM) to write the data to its internal memory? (e.g. 5ms wait between end of write before accessing the EEPROM again)
9. If writing to an EEPROM, have the (32-byte) page boundaries been crossed (which leads to overwriting the lower bytes of the same page instead of writing addressed on the next page)?
10. If attempting to write to a device that has been configured by its pre-programmed EEPROM:
    Has enough time elapsed for the configuration to load? Has the flag (e.g. BCDONE = Boot Controller Done) been set?
11. Do the read and write transactions follow the functional timing described in the datasheet? (Scope or Logic Analyzer capture helpful here)
12. Have the wait statements that are in the configuration file been implemented? Not waiting when needed can result in an incorrect configuration.
13. Are all of the GND pins connected?
14. Are all signals that are supposed to be low/high driven low/high (not floating)?
15. Is the proper clock rate being used that corresponds to the slowest device on the bus?
16. Are setup/hold times per datasheet specs being followed?

Applicable specifically to I^{2}C

1. Are the pull-up resistors installed and the correct values?
   $R_{PUP}(Max) = T_R(Max)\ /\ [0.8473 \times C_L]$
   $R_{PUP}(Min) = [V_{CC} - V_{OL}(Max)]\ /\ I_{OL}$

   where
   T_R = Max Rise Time
   C_L = Total Bus Capacitance
   V_{OL} = Low-Level Output Voltage
   I_{OL} = Output Leakage Current
2. Is the pull-up level (e.g. 3.3V) the same as the Master/Slave bus Vdd?
3. Does the address being written match the address of the slave device?
4. Was the start condition properly generated? (SDA goes L-to-H while SCL is H)
5. Does the Master receive the ACK from the slave after issuing a write enable sequence?
6. Is the bus idle while Master is attempting to communicate on the bus (i.e., does SDA = SCL = H)?
7. Are the SCK and SDA signals reversed?

Applicable specifically to SPI

1. Is Master's MOSI connected to Slave's MOSI and not the Slave's MISO?
2. Are the Master and Slave MOSI/MISO busses on the same Vdd level?
3. Does each device have its own CS\?
4. Is only one device's CS\ asserted at a time?
5. Is any CS\ hardwired to gnd? (It should not be)
6. Because SPI operates in the MHz range, high speed design considerations must be taken into account, such as impedance matching. For example, it may help to insert a series R close to the driver on a MISO or MOSI line. Have high-speed design practices been used?