
Enterprise Storage Backplane Management Processor

- Complete Universal Storage Backplane Management Processor
 - SFF-TA-1005 Universal Backplane Management (UBM) over I2C
 - Provides SFF-8654 compliant Host Facing Connector (HFC) communication support over I2C
 - HFC connection responds to all standard UBM commands from the host
 - Integrates the UBM FRU non-volatile memory on the UBM FRU I2C Address
 - Provides SFF-8639 compliant U.2 Drive Facing Connector (DFC) Support
 - Provides SFF-TA-1001 compliant U.3 Drive Facing Connector (DFC) Support
 - Support for SES over UBM
- Supports I2C communication to Baseboard Management Controller
- Up to 8 I2C ports for UBM and BMC host interfaces
- SFF-8485 Support
 - Implements up to 4 Hardware Accelerated SGPIO Legacy Interfaces for SAS/SATA backplane implementations
- Secure Boot
 - EEC1005 code is authenticated by a secure boot loader prior to loading from internal flash
 - Hardware accelerated crypto blocks provide fast secure boot
 - Secure Firmware update
 - Key revocation
- Supports Storage LED Management as per SFF-8489 IBPI specifications by default
- Custom LED patterns can be configured
- Scalable Solution for up to 16 Hard Drives on a Single Device
 - SGPIO Host Interfaces support up to 16 drives (SAS/SATA drive types)
 - UBM Host Interfaces support up to 12 drives (NVMe drive types)
 - Up to 6 HFCs
- Supports multiple backplanes on a single chassis
- Support for NVME Hot plug and Power Disable for drives
- Integrated NV Memory for:
 - UBM FRU (Field Replaceable Unit) for every HFC
 - General Purpose FRU
 - NV Configuration Memory
- Configurable Interfaces using a single analog configuration pin
 - Host interface (SGPIO vs UBM)
 - Number of HFCs and Drive Facing Connectors (DFCs)
 - Other supported features
- Monitors system PERST
 - One pin per DFC for PERST support
- Monitors for drive insertion from IFDET and PRSNT signals
 - IFDET2 support (for SFF-TA-1001)
- Package Options
 - 144 pin WFBGA RoHS Compliant package
 - 84 pin WFBGA RoHS Compliant package

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1.0 GENERAL DESCRIPTION

EEC1005 is a generic, easily configurable, True Universal Backplane Management (UBM) device that can be used on hard drive backplanes to provide complete storage enclosure management and reporting to computing host systems using industry standard communication protocols.

EEC1005 supports a variety of host interfaces to accommodate SAS/SATS/NVMe backplane. The SFF-8654 slimline connector (Host facing Connector) can be used to route SAS signals in which case the HBA will manage SAS/SATA drives, the same connector protocol (physically a different connector) can be used to route PCIe signals in which case the HBA will manage NVME drives. In both cases UBM will be used as management protocol with support of SGPIO as well on SAS Slimline (Configuration dependent). The device supports using U.2 and U.3 Drive facing Connectors. EEC1005 also supports Multiple Backplanes on a single chassis.

EEC1005 supports 2 or 3 LED IBPI blinking patterns for up to 16 drives. Customized LED blink pattern can also be programmed through the FRU.

The EEC1005 has a secure boot loader that authenticates and decrypts the Flash boot image (UBM application) using the AES-256, ECDSA P-256, SHA-256 cryptographic hardware accelerators. EEC1005 hardware accelerators support 128-bit and 256-bit AES encryption, ECDSA and EC_KCDSA signing algorithms, 1024-bits to 4096-bits RSA and Elliptic asymmetric public key algorithms, and a True Random Number Generator (TRNG). Additionally, the device offers lockable OTP storage for private keys and IDs.

EEC1005 is available in 84 pin and 144 pin WFBGA packages.

2.0 UBM BACKPLANE ARCHITECTURE

EEC1005 on the back plane communicates to the Host through SGPIO or I2C interface over the Host facing Connector (Host attach configuration) or dedicated cable (Direct attach configuration). It detects hard drive being installed in the backplane and notifies the host of the insertion/removal/failure of the drive. It also blinks Leds for each hard drive's status.

There are different types of Backplanes based on:

1. Number of drives the back plane supports
2. Type of host communication (For eg. I2C or SGPIO)
3. Type of Drive slots (For eg. U.2 or U.3)

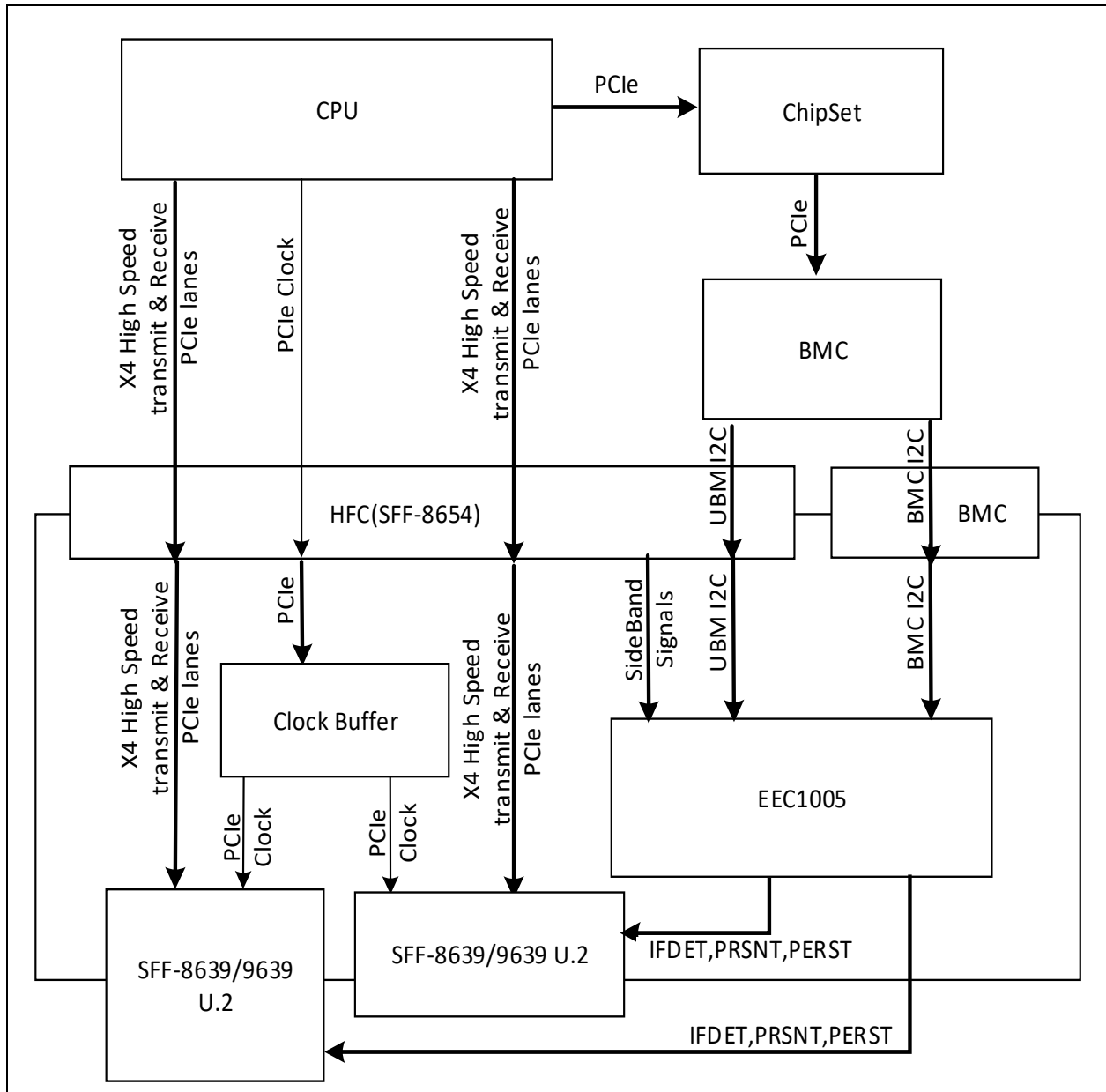
The different configurations of the backplane that EEC1005 supports is covered in [Section 3.0, "Configurations"](#).

2.1 Direct Attach UBM Backplane

A direct attach configuration is enabled when user connects the backplane directly to mother board and the drives are not managed by an HBA. In this case the drives are managed either by BMC or PCIe Switch/Expander for switch-based configurations. EEC1005 can be used in Direct attach configurations using UBM as the management protocol from BMC (BMC Emulation) or Switch/Expander.

EEC1005 based backplane architectures are capable of supporting Y-cable configurations where the PCIe lanes from a single Host HFC will be split into 2x backplane HFC's, this allows splitting on PCIe clocks using clock buffers as shown in the following diagram.

FIGURE 2-1: DIRECT ATTACH CONFIGURATION



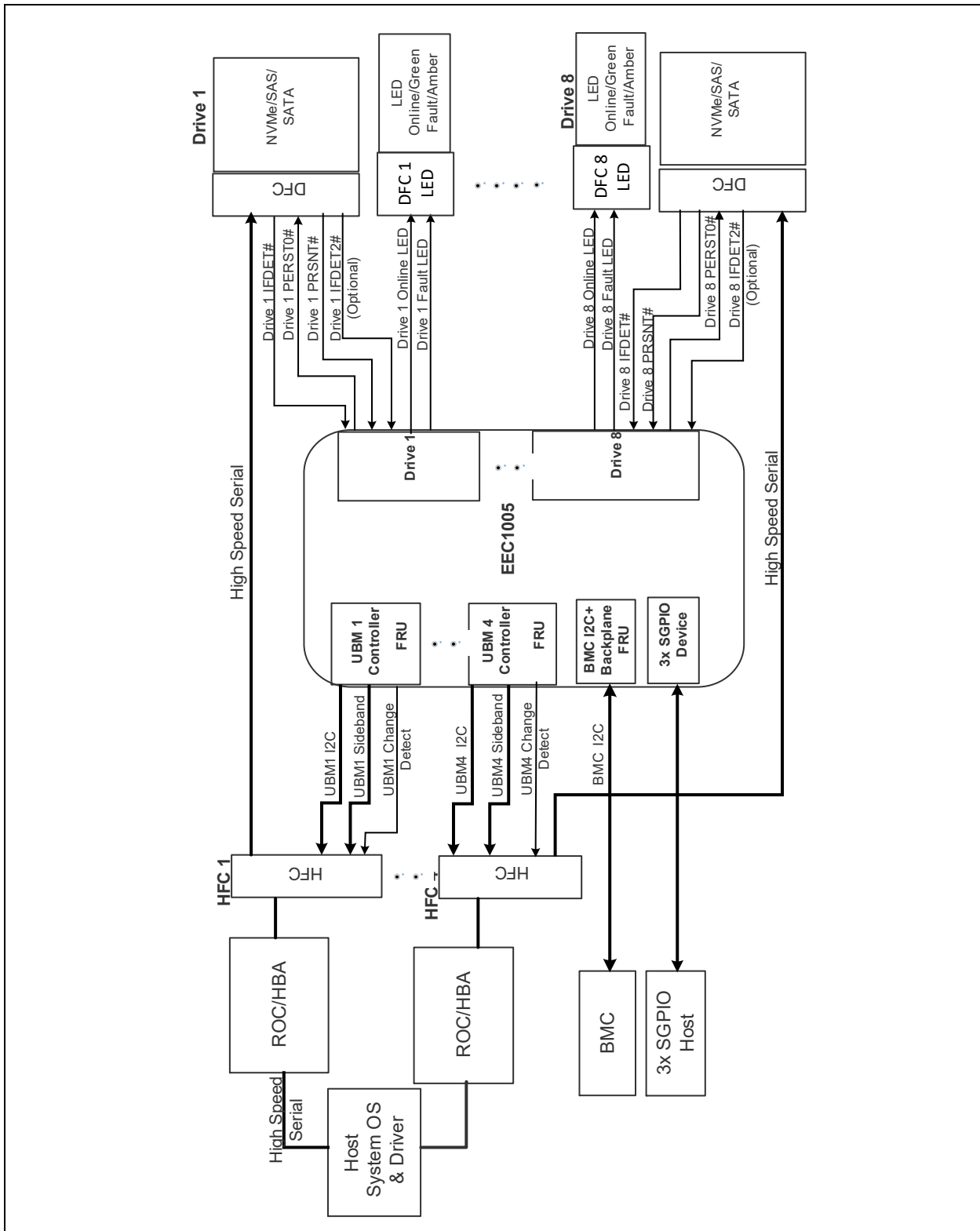
2.2 Host Attach UBM Backplane

A Host attach configuration is enabled when user connects the backplane directly to SMARTROC/HBA and the drives are managed by an HBA. EEC1005 can be used in Host attach configuration as in [FIGURE 2-2: "Host Attach Configuration"](#). Each HFC is connected to a Host through a cable to communicate with EEC1005.

EEC1005 based backplane architecture supports NVME PERST functionality by allowing the Host to directly control the PERST signal. This allows the Host to directly control the reset behavior of NVME drive without adding any latency. The PERST signal will be driven from HFC and then split into 2 signals to control 2 drives from a single signal.

Note: The hardware bifurcation of the PCIe lanes is application dependent. Usually each HFC bifurcates x8 lanes into two x4 connections.

FIGURE 2-2: HOST ATTACH CONFIGURATION



3.0 CONFIGURATIONS

Multiple Backplane architectures are supported using EEC1005 that are configured by firmware based on an analog value sampled at one of EEC1005 input ADC pin (Config Pin) at startup. [Table 3-1, “EEC1005 Configuration select”](#) provides the complete list of Configurations selectable based on the analog value on CONFIG_PIN. The analog value can be set by a resistor divider network, the values of the resistors are user defined. The configuration is fixed for a Backplane and is not runtime modified.

TABLE 3-1: EEC1005 CONFIGURATION SELECT

EEC1005 Config	Pin Count	HFC Total ^a	HFC - SAS	HFC - PCIe	DFC Total	DFC SAS/SATA	DFC PCIe
4 Drive SGPIO	84	1	1	0	4	4	0
8 Drive SGPIO	84	1	1	0	8	8	0
12 Drive SPGIO	144	2	2	0	12	12	0
16 Drive SPGIO	144	2	2	0	16	16	0
4 Drive UBM U.2	84	3	1	2	4	4	4
8 Drive UBM U.2	84	5	1	4	8	8	8
8 Drive UBM U.2 (Full Feature)	144	5	1	4	8	8	8
8 Drive UBM U.3 (Minimum Feature)	84	4	4	4	8	8	8
8 Drive UBM U.3 (Full Feature)	144	4	4	4	8	8	8
12 Drive UBM U.2 PCIe Only (Full Featured)	144	6	0	6	12	0	12
12 Drive UBM U.3 PCIe Only (Full Featured)	144	6	0	6	12	0	12
8 Drive UBM+SGPIO U.2	144	5	1	4	8	8	8

^a. HFC Total is the number of a particular configuration.

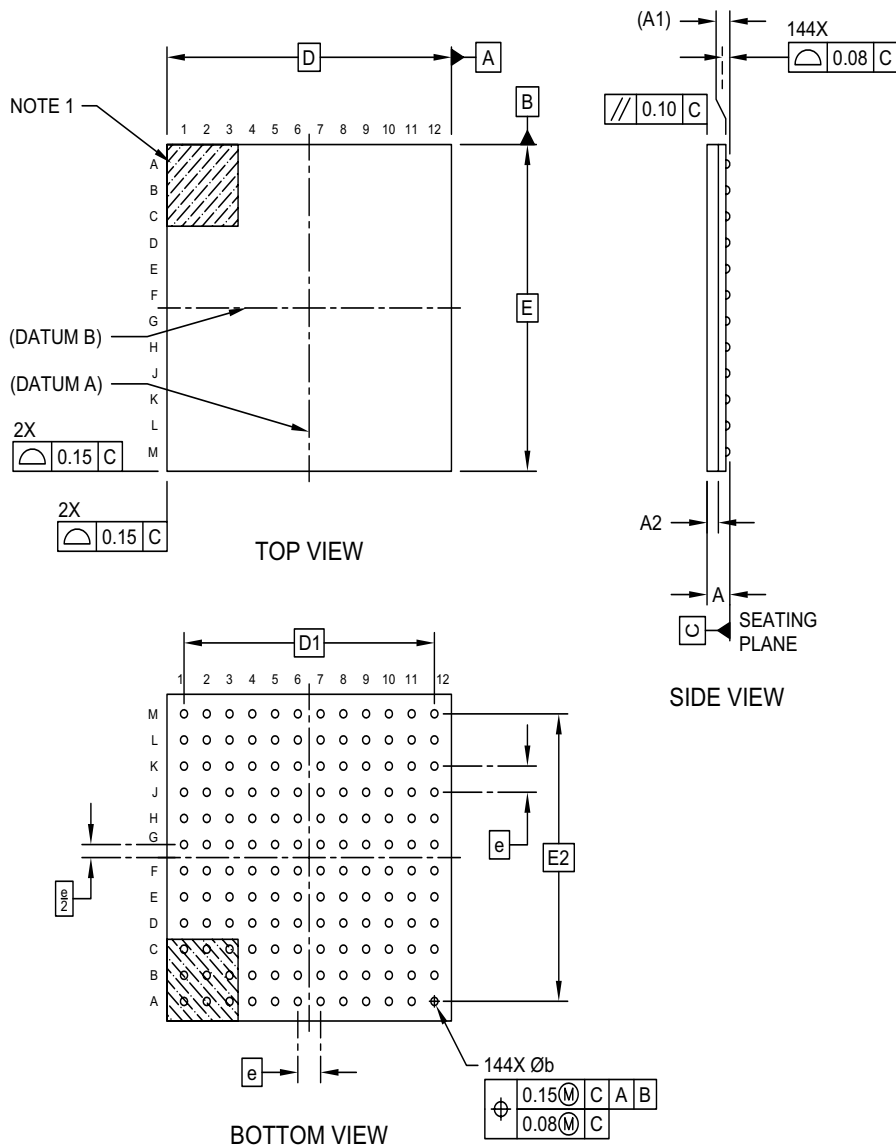
4.0 PACKAGE INFORMATION

4.1 144 Pin WFBGA/WC Package

Note: For the most current package drawings, see the Microchip Packaging Specification at <http://www.microchip.com/packaging>.

144-Ball Very, Very Thin Fine Pitch Ball Grid Array (WCX) - 10x10 mm Body [WFBGA]

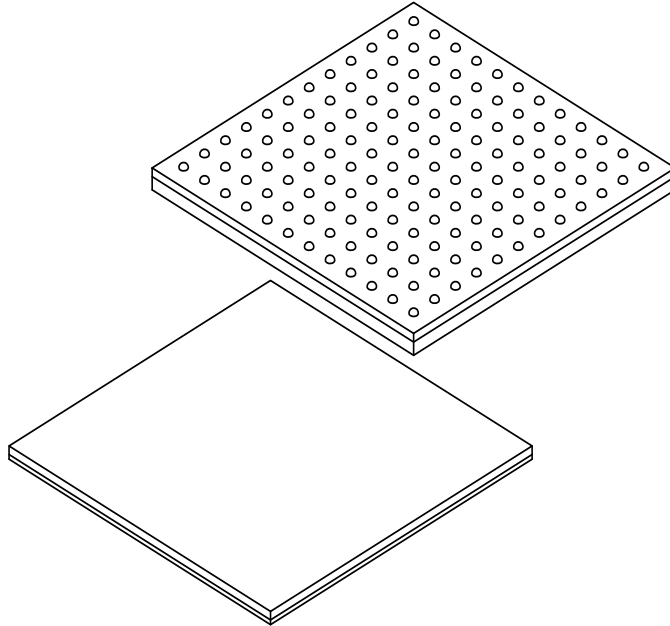
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Microchip Technology Drawing C04-416A Sheet 1 of 2

144-Ball Very, Very Thin Fine Pitch Ball Grid Array (WCX) - 10x10 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	144		
Pitch	e	0.80 BSC		
Overall Height	A	-	-	0.80
Standoff	A1	0.17 REF		
Mold Package Thickness	A2	0.35	0.40	0.45
Overall Length	D	10.00 BSC		
Exposed Pad Length	D1	8.80 BSC		
Overall Width	E	10.00 BSC		
Exposed Pad Width	E1	8.80 BSC		
Terminal Diameter	b	0.20	0.25	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

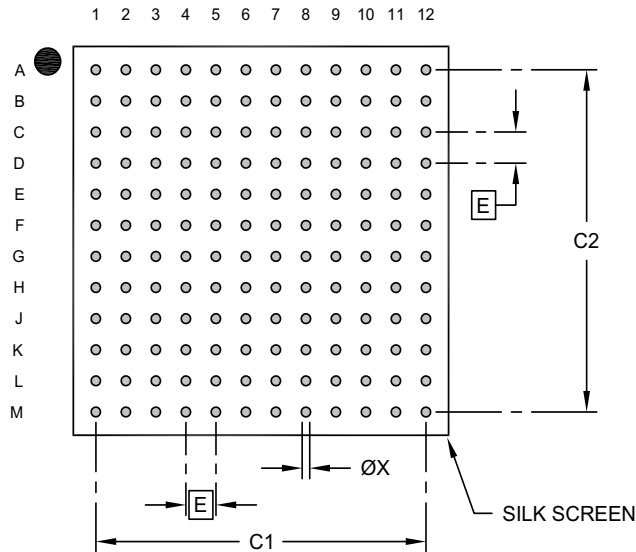
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-416A Sheet 2 of 2

144-Ball Very, Very Thin Fine Pitch Ball Grid Array (WCX) - 10x10 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		8.80	
Contact Pad Spacing	C2		8.80	
Contact Pad Width (X20)	X		0.25	

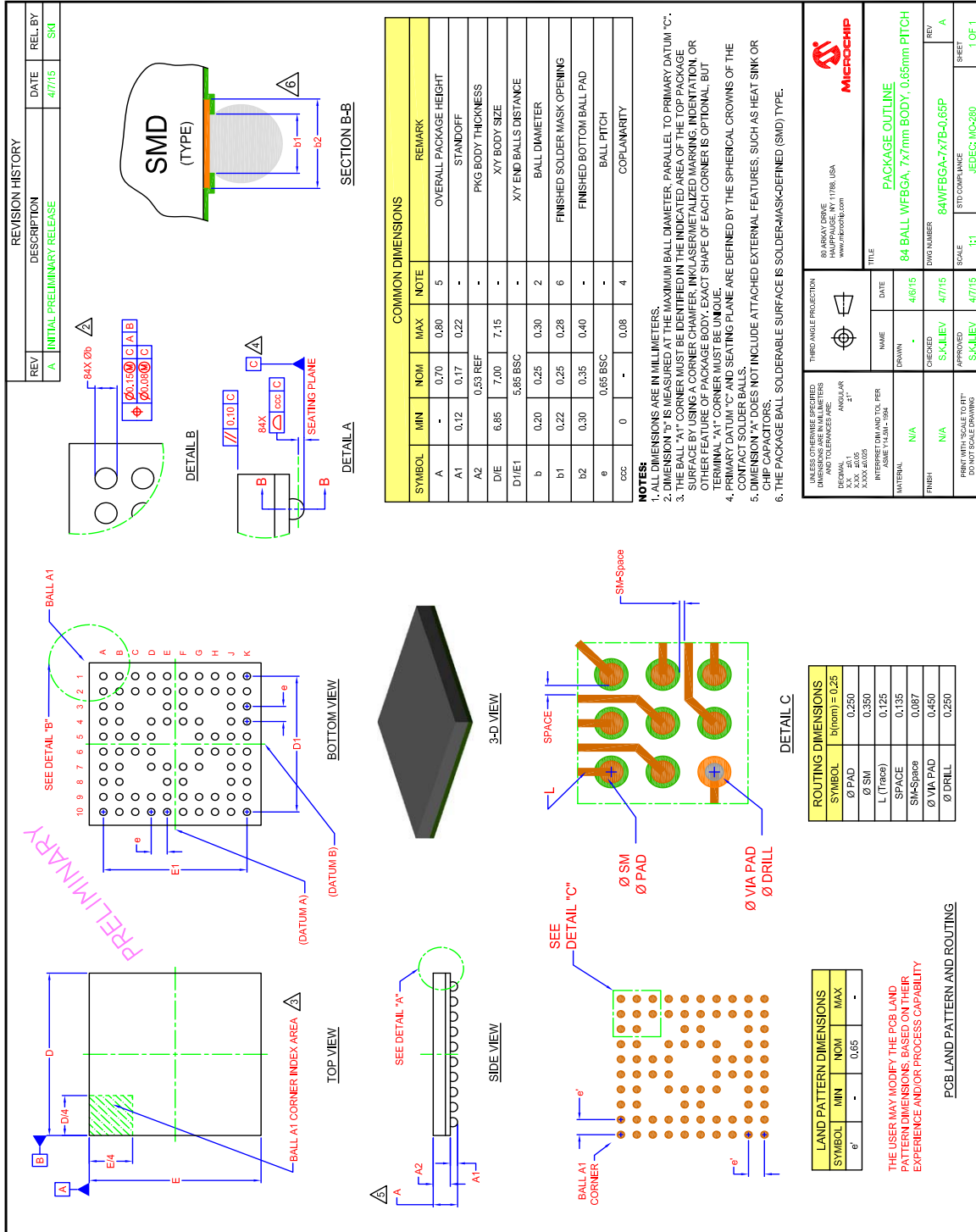
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2416A

4.2 84 Pin WFBGA/SX1 Package

Note: For the most current package drawings, see the Microchip Packaging Specification at <http://www.microchip.com/packaging>.



APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00003488A (05-06-20)	Initial document	

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EEC1005

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<u>PART NO.</u> ⁽¹⁾	-	<u>X</u>	-	<u>XX</u>	-	<u>X/XXX</u> ⁽²⁾	-	<u>X1</u> ⁽³⁾
Device		Total SRAM		Version/ Revision		Temp Range/ Package		Tape and Reel Option
Device:		EEC1005 ⁽¹⁾		UBM Controller				
Total SRAM:		H		256KB				
Version/ Revision:		B#		B = Version, # = Version Revision Number				
Temperature Range:	I/	= -40°C to +85°C (Industrial)						
Package:	WC	144 pin WFBGA 10x10mm body, 0.80mm pitch						
	SX1	84 pin WFBGA 7x7mm body, 0.65mm pitch						
Tape and Reel Option:	Blank	= Tray packaging						
	TR	= Tape and Reel ⁽³⁾						

Example:

a) EEC1005-I/WC = EEC1005 with 12-drive UBM solution provided with FW

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit <http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html>

3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option

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