AN5104

MPLAB® Connect PCI1XXXX Options

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1.0 INTRODUCTION

MPLAB® Connect provides a GUI for configuring the EEPROM or OTP in the following series of devices: PCI11414, PCI11400, PCI11101, PCI11010, and PCI12000. When a device is selected, MPLAB Connect only shows configuration options that are available for that specific device. For more information on which peripherals are available for a given device, consult the model number's appropriate data sheet.

This document details each configuration option that can be found in the PCI1xxxx series. For settings not specifically broken out in MPLAB Connect, the user has the option of providing direct register writes. Additionally, a function is provided to read an EEPROM/OTP binary file and display the specific register writes.

1.1 Sections

This application note covers the following topics:

- Section 2.1, Configuration File Parser
- Section 2.2, Device Descriptors
- Section 2.3, Configuration Files
- Section 2.4, Direct Register Access
- Section 2.5, System Configuration
- Section 2.6, Ethernet Subsystem Options
- Section 2.7, Device Capabilities 2
- Section 2.8, USB Subsystem
- Section 2.9, Peripheral Subsystem

1.2 References

Refer to the following documents when using this application note:

- *PCI11414 Data Sheet*
- *PCI11400 Data Sheet*
- *PCI11101 Data Sheet*
- *PCI11010 Data Sheet*
- *PCI12000 Data Sheet*
- *AN4885 Interfacing PCI1xxx with RS-232, RS-422 and RS-485 Through UART*
- *PCI Express Base Specification Revision 4.0*
- *MPLAB® Connect Configurator GUI User Manual*

2.0 CONFIGURATION

2.1 Configuration File Parser

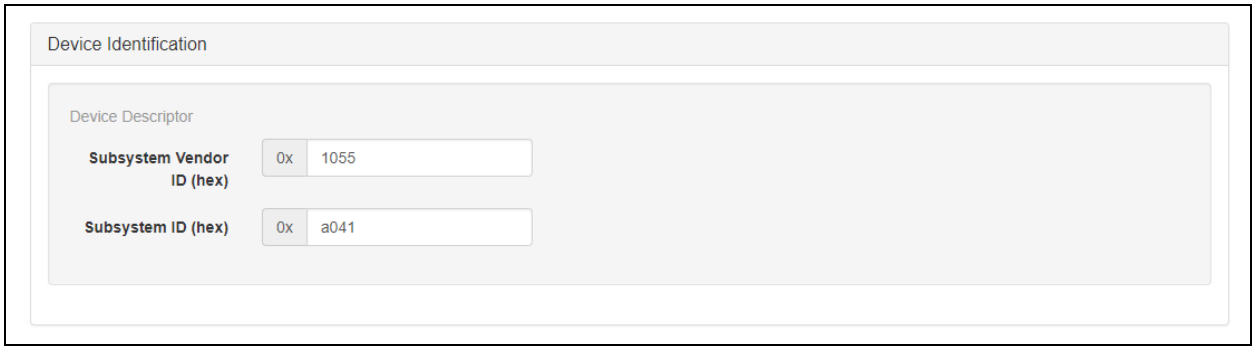
After loading the application, the Configuration File Parser allows a binary configuration file (".bin") to be converted into a human readable configuration generation file (".ini"). Using *Choose File*, a user can point MPLAB Connect to a valid PCI1xxxx .bin file. Once the file is selected, the user can choose *Save Parse Output*, if they wish to save the output as an .ini file. If the *Save Parse Output* box is checked, a *Choose File* button will appear that will allow the selection of a save location.

FIGURE 1: CONFIGURATION FILE PARSER

2.2 Device Descriptors

This section can be found in every subsystem. It allows the user to set the vendor ID and subsystem ID per subsystem.

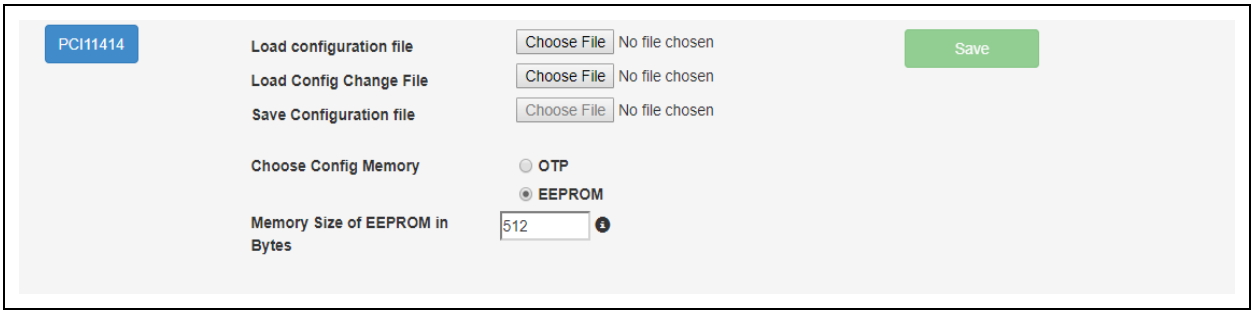
FIGURE 2: DEVICE DESCRIPTORS



2.3 Configuration Files

This menu allows the user to save or load a configuration file. Both the *Save* and *Save Configuration* buttons remain grayed out until at least one setting is changed from the default.

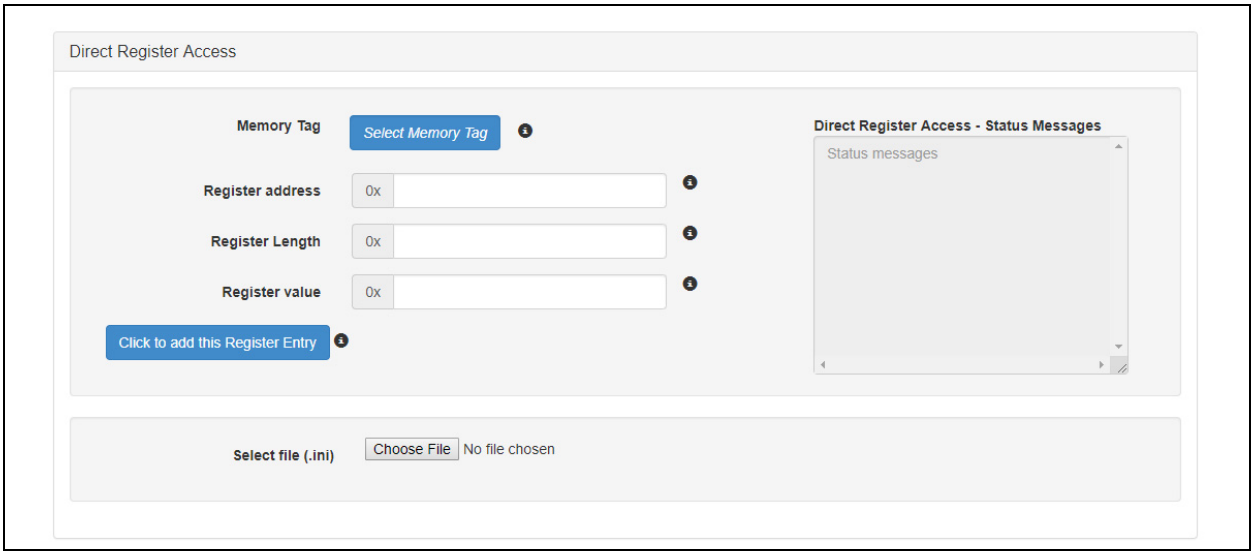
FIGURE 3: CONFIGURATION FILES



2.4 Direct Register Access

Direct Register Access allows the user to directly write values to registers. Register offsets and descriptions can be found in a separate PCI1xxxx configuration and register map application note.

FIGURE 4: DIRECT REGISTER ACCESS



2.5 System Configuration

2.5.1 SUBSYSTEMS

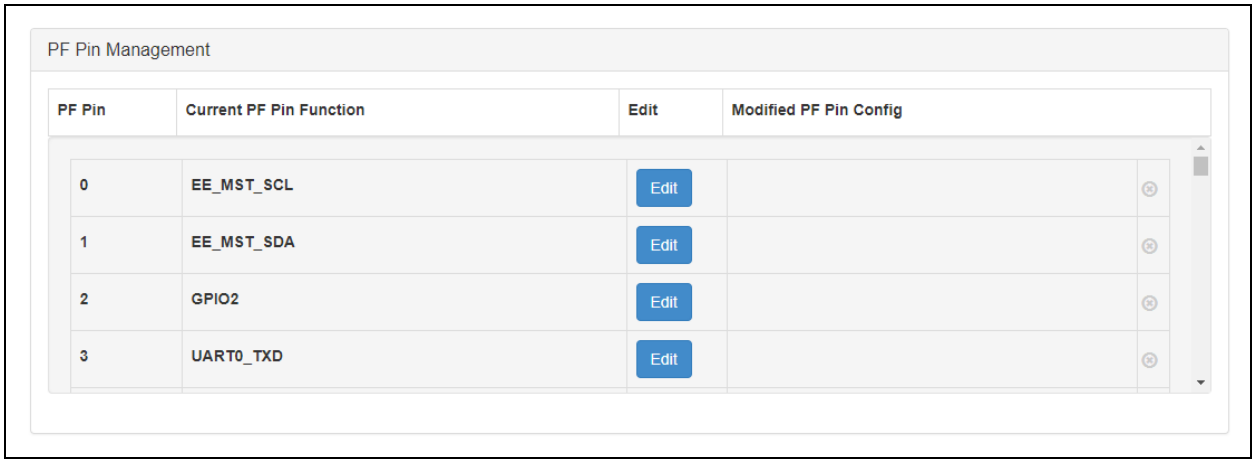
The Subsystems menu allows the user to enable or disable the various subsystems. When a subsystem is disabled, it will not enumerate on a host. The Peripheral Subsystem includes GPIO, I^2C, SPI, and UART.

FIGURE 5: SUBSYSTEMS

2.5.2 PF PIN MANAGEMENT

This section allows users to assign functions per pin to the PROG*X* pins. After clicking on *Edit*, the user is presented with a dropdown menu with the up to 16 possible functions available for the corresponding pin. Selecting the desired function and clicking *Save PF Config* will display the new function under the Modified PF Pin Config column.

FIGURE 6: PF PIN MANAGEMENT



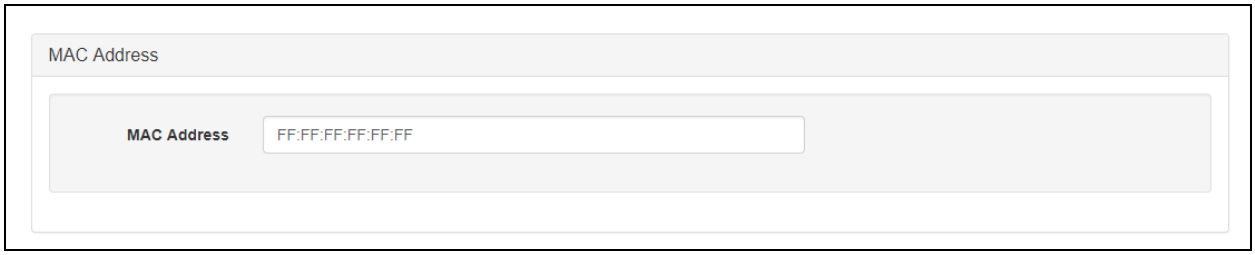
2.6 Ethernet Subsystem Options

Note:	This Ethernet Subsystem is only available with PCI11414 and PCI11010.

2.6.1 MAC ADDRESS

This configurable setting allows the user to set the MAC address. This field requires six colon-separated bytes.

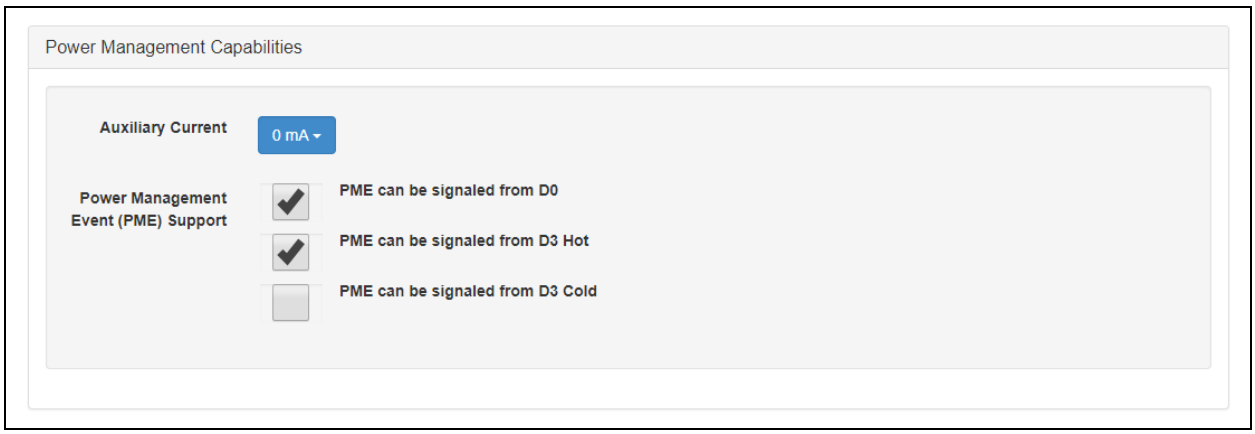
FIGURE 7: MAC ADDRESS



2.6.2 POWER MANAGEMENT CAPABILITIES

The Power Management Capabilities menu allows the user to define the maximum auxiliary current available on the 3.3V AUX PCIe power rail by choosing the value from the Auxiliary Current dropdown menu. Three separate Power Management Event variables may be toggled to set the device power states that signal PME events.

FIGURE 8: POWER MANAGEMENT CAPABILITIES



2.6.3 LINK CAPABILITIES

This section allows the user to set the Clock Power Management bit of the Link Capabilities register. If Set is selected, the PCI11414/PCI11010 will use CLKREQ# to control REFCLK. If Clear is chosen, PCI11414/PCI11010 will not use CLKREQ#.

FIGURE 9: LINK CAPABILITIES

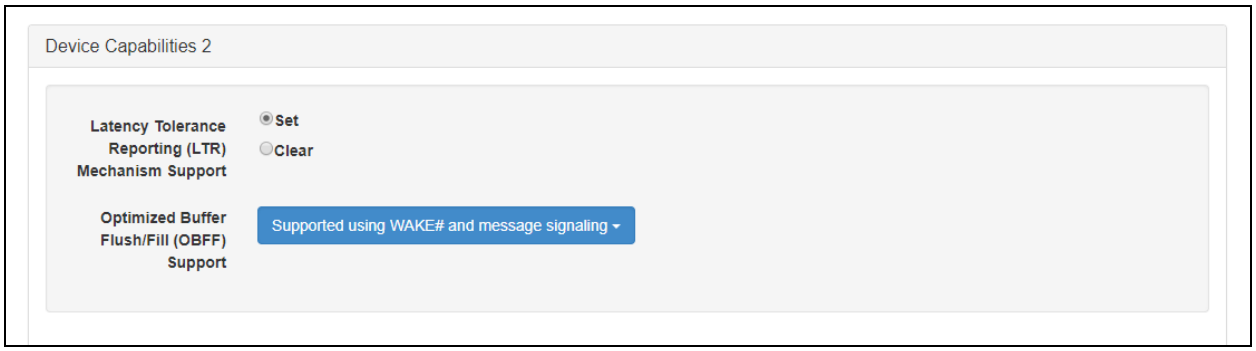
2.7 Device Capabilities 2

The Device Capabilities 2 menu features options for setting Latency Tolerance Reporting (LTR) Mechanism Support. When Set is chosen, the use of PCIe LTR messages is enabled. When Clear is selected, PCI11414/PCI11010 will treat LTR messages as Unsupported Requests.

The user may also toggle Optimized Buffer Flush/Fill (OBFF) Support. For more information on how OBFF works, refer to PCI Express Base Specification Revision 4.0 Version 1.0. Both PCI11414 and PCI11010 have four modes of OBFF:

- Not Supported
- Supported using message Signaling only
- Supported using WAKE# Signaling only
- Supported using WAKE# and message signaling

FIGURE 10: DEVICE CAPABILITIES 2

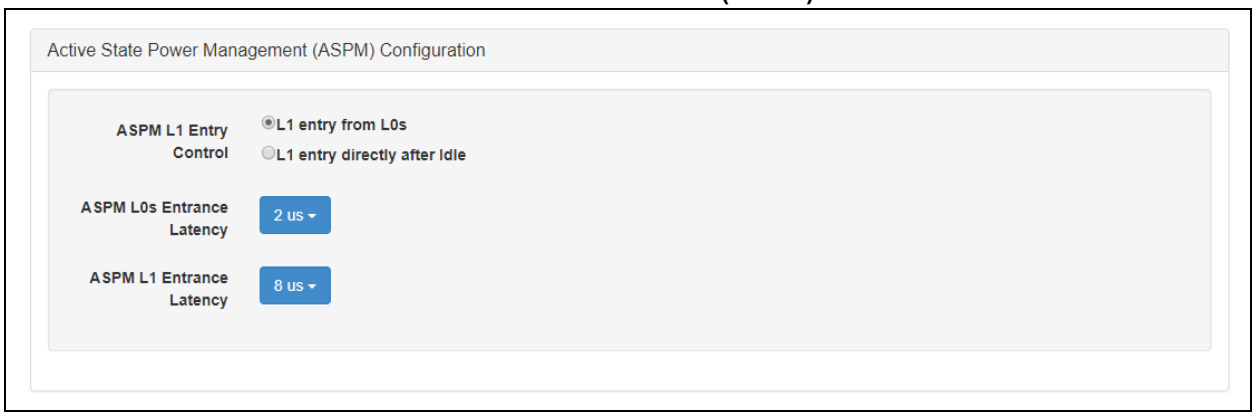


2.7.1 ACTIVE STATE POWER MANAGEMENT (ASPM) CONFIGURATION

ASPM Configuration determines variables for L1 Entry Control as well as L0s and L1 Entrance Latency. Entry Control determines when PCI11414/PCI11010 enters the L1 power state. If L1 entry from L0s is selected, the device will enter L1 after the transmitter and receiver have been in idle for the amount of time chosen by ASPM L1 Entrance Latency. L1 entry from L0s will enter L1 after the selected ASPM L1 Entrance Latency amount of time.

- ASPM L0s Entrance Latency: Amount of time before entering into L0s.
- ASPM L1 Entrance Latency: Amount of time before entering into L1.

FIGURE 11: ACTIVE STATE POWER MANAGEMENT (ASPM) CONFIGURATION



2.7.2 L1 PM SUBSTATES CAPABILITIES

The L1 PM Substates Capabilities menu provides several options for Substate configuration. When L1 PM Substates Support is set, the user is allowed to enable or disable L1 substates. When set to clear, the other L1 substate settings are ignored.

For the following settings, refer to PCI Express Base Specification Revision 4.0 for more information on how they work:

- PCI-PM L1.2 Support
- PCI-PM L1.1 Support
- ASPM L1.2
- ASPM L1.1

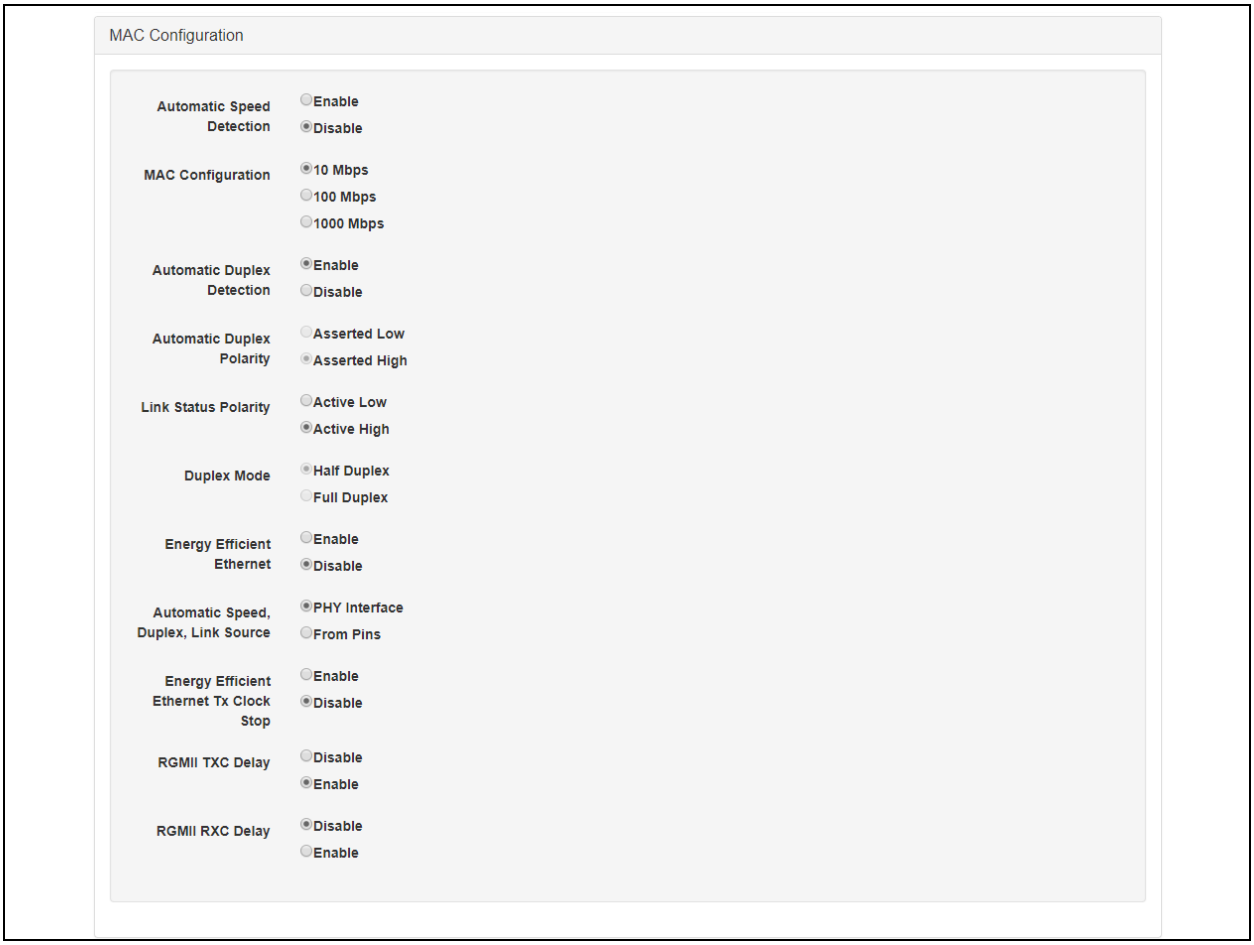
FIGURE 12: L1 PM SUBSTATES CAPABILITIES

2.7.3 MAC CONFIGURATION

MAC Configuration for PCI11414/PCI11010 is determined by the following options in the MAC Configuration menu:

- **Automatic Speed Detection:** If disabled, MAC Configuration sets the speed of the connection. If enabled, the speed of the connection is determined automatically.
- **MAC Configuration:** Sets the speed for Ethernet MAC communication. This setting is ignored if Automatic Speed Detection is set.
- **Automatic Duplex Detection:** If disabled, Duplex mode determines whether the MAC communicates at half duplex or full duplex. If enabled, the duplex setting is determined automatically.
- **Automatic Duplex Polarity:** This determines the behavior of the duplex PHY LED. If asserted low, the duplex PHY LED will be low in Full Duplex mode. If asserted high, the duplex PHY LED will be high in Full Duplex mode.
- **Link Status Polarity:** Sets the polarity of the link status bit. If Active Low is set, link status will be 0 when the PHY has a valid link. If Active High is set, link status will be 1 when the PHY has a valid link.
- **Duplex Mode:** Allows the user to set the Ethernet MAC to half or full duplex. If Automatic Duplex Detection is set, this setting is ignored, and the corresponding bit reflects the last determined duplex operating mode.
- **Energy Efficient Ethernet:** Enables or disables Energy Efficient Ethernet.
- **Automatic Speed, Duplex, Link Source:** Sets the source of Automatic Speed, Duplex, and Link. If PHY Interface is set, Automatic Speed, Duplex, and Link are all set by the PHY. If From Pins is set, Automatic Speed is calculated from the receive clock and Duplex and Link are both set by pins.
- **Energy Efficient Ethernet Tx Clock Stop:** When enabled, the MAC will halt the clock to the PHY during TX LPI.
- **RGMII TXC Delay:** When enabled, adds a delay of ~8 ns for 1000BASE-T, ~40 ns for 100BASE-TX, or ~400 ns for 10BASE-T.
- **RGMII RXC Delay:** When enabled, adds a delay of ~8 ns for 1000BASE-T, ~40 ns for 100BASE-TX, or ~400 ns for 10BASE-T.

FIGURE 13: MAC CONFIGURATION



2.7.4 ETHERNET STRAP

Ethernet Strap configuration for PCI11414/PCI11010 is determined by the following options:

- **SGMII Enable Strap:** When activated, this strap will set SGMII Enable to enable and SGMII Power Down to disable during EEPROM configuration.
- **SGMII Reference Clock Strap:** This strap is used by software to select the correct SGMII 1000/2500BASE-X reference clock source.
- **2.5G Strap:** This strap is used by software to perform any configuration required for operation at 2.5 Gbps.
- **Base-X Strap:** This strap is used by software to perform any configuration required for operation at 1000 or 2500 BASE-X mode.
- **RGMII TXC Delay Enable Strap:** When enabled, this strap will set RGMII TXC Delay to enable during EEPROM Configuration.
- **RGMII RXC Delay Enable Strap:** When enabled, this strap will set RGMII RXC Delay to enable during EEPROM Configuration.
- **Advance Power management Disable Strap:** When this strap is set, the following settings are disabled during EEPROM Configuration:
  - Clock Power Management
  - L1 PM Substates Supported
  - ASPM L1.1 Supported
  - ASPM L1.2 Supported
  - PCI-PM L1.1 Supported
  - PCI-PM L1.2 Supported

Note: The settings these straps control may be overwritten in EEPROM/OTP configuration. The straps will change the appropriate values during a chip-level reset or a reload command.

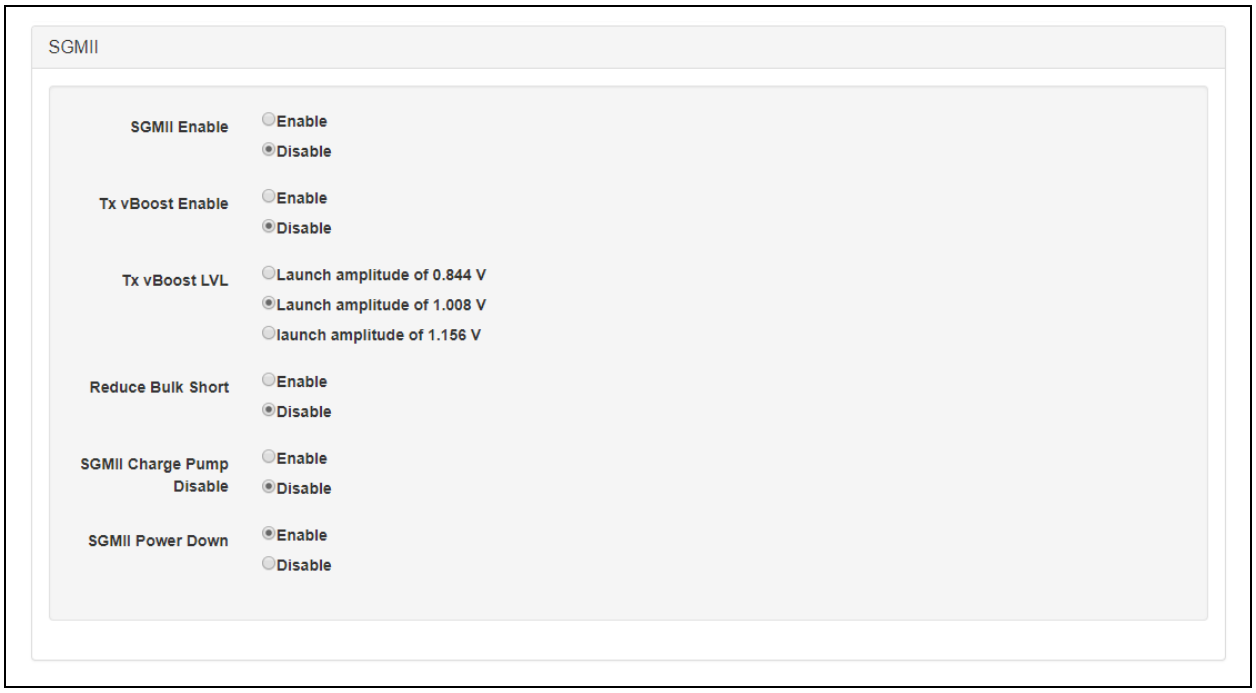
FIGURE 14: ETHERNET STRAP

2.7.5 SGMII

SGMII configuration for PCI11414/PCI11010 is determined by the following options:

- **SGMII Enable:** When enabled, the ethernet MAC operates in SGMII 1000/2500BASE-X mode.
- **Tx vBoost Enable:** Enables the use of Tx vBoost. This setting should be left disabled unless the Ethernet eye diagram is failing.
- **Tx vBoost LVL:** Sets the emphasis level of transmitted data. This value should be left at a default of 1.008V unless the Ethernet eye diagram is failing.
- **Reduce Bulk Short:** When enabled, reduces the resistance between bulk and ground from 10 kΩ to 1 kΩ.
- **SGMII Charge Pump Disable:** When enabled, the charge pump is controlled by the internal SGMII/RGMII controller based on RGMII/SGMII mode and the analog voltage.
- **SGMII Power Down:** When enabled, the SGMII 1000/2500BASE-X interface is disabled and in a power down state.

FIGURE 15: SGMII



2.8 USB Subsystem

Note: This option is only available on PCI11414, PCI11400, and PCI11101

2.8.1 DOWNSTREAM PORT CONFIGURATION

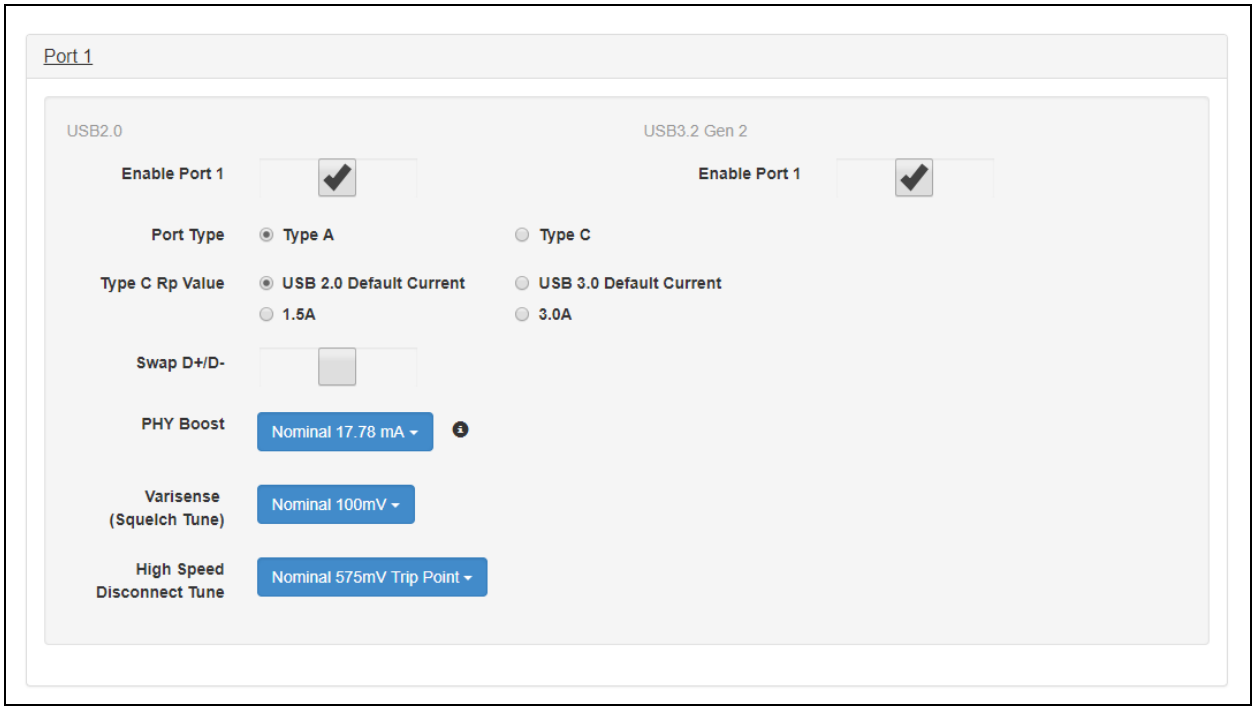
2.8.1.1 Port x

Port configuration for PCI11414, PCI11400, and PCI11101 is determined by the following options:

- **Enable Port x:** Enables the USB port. All 4 ports support USB2, but only ports 1 and 2 support USB3.2 Gen 2.
- **Port Type:** Sets the port connector type to type-A or -C. This setting should be based off the hardware design.
- **Type C Rp Value:** Defines the maximum current the USB port can source.
- **Swap D+/D-:** Swaps the D+ and D- lines for USB2. This setting should be informed by the hardware layout.
- **PHY Boost:** Sets the driving current of the USB2 transceiver from -5% to +25%.
- **Varisense (Squelch Tune):** This setting helps tune the receiver allowing a greater range of options for receiver Sensitivity.
- **High Speed Disconnect Tune:** This setting helps tune the receiver allowing a greater range of options for receiver sensitivity.

  Note: This setting must align with the physical hardware current sourcing capability of the 5V load switch which sources power to the USB port.

FIGURE 16: DOWNSTREAM PORT CONFIGURATION

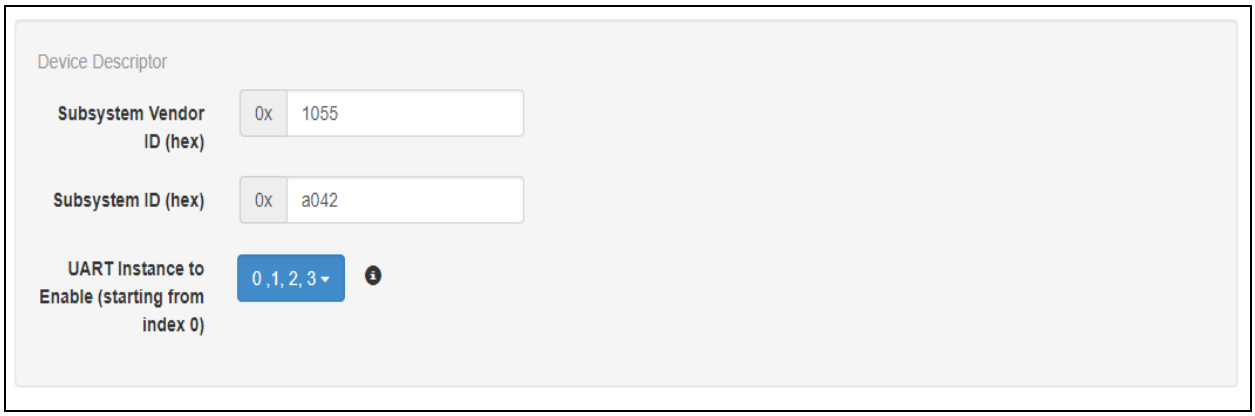


2.9 Peripheral Subsystem

2.9.1 PERIPHERAL: SERIAL PORT (UART)

The value of the UART subsystem ID determines which UART instances enumerate. In MPLAB CONNECT this is generated automatically using the UART Instance to Enable (starting from index 0) dropdown menu.

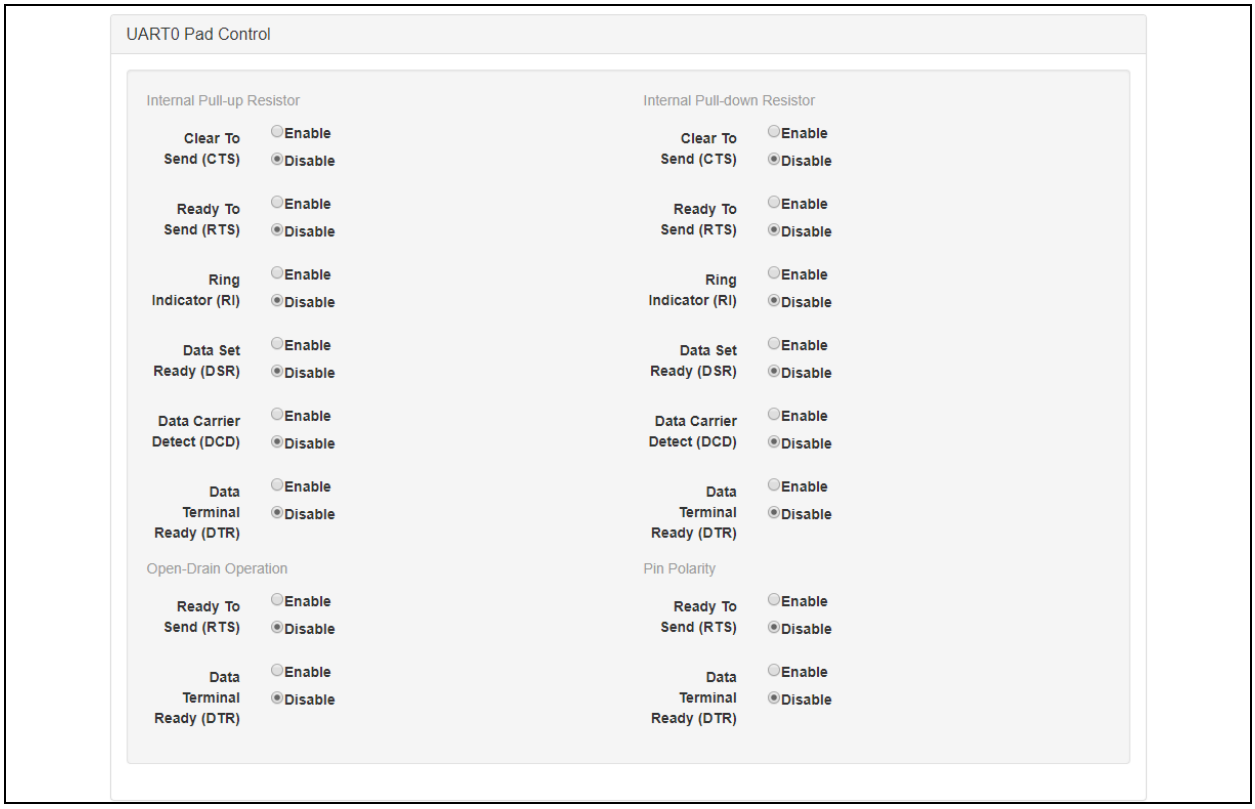
FIGURE 17: UARTX PAD CONTROL



2.9.1.1 UARTX Pad Control

This section allows the user to enable internal pull up or pull down resistors for the UART flow control signals. For more detail on these signals, please refer to AN4885 “Interfacing PCI1xxx with RS-232, RS-422 and RS-485 Through UART".

FIGURE 18: UARTX PAD CONTROL



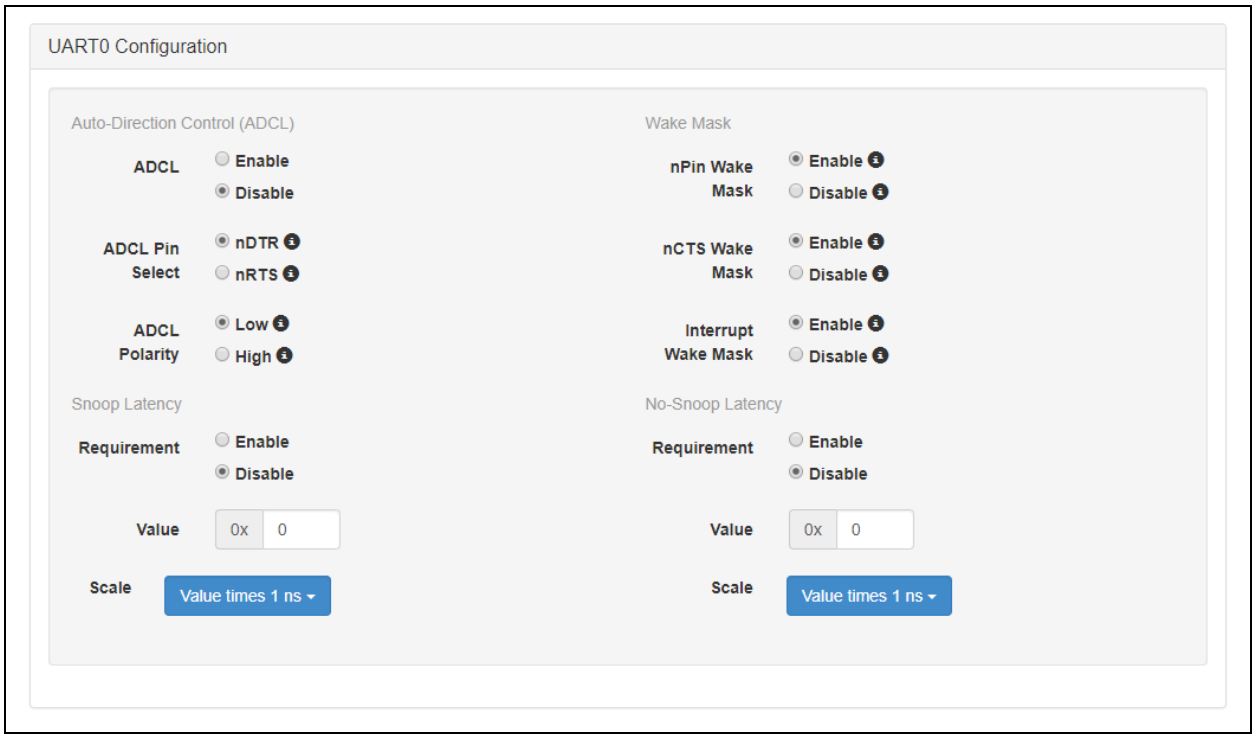
Note: For pin polarity, Enable means high polarity and Disable means low polarity.

2.9.1.2 UARTX Configuration

UARTX Configuration is determined by the following options:

- **ADCL:** Auto Direction Control Enable. When enabled, UART uses ADCL Pin Select and ADCL Polarity to determine which pin to use to control direction.
- **ADCL Pin Select:** Sets which pin is used for Auto Direction Control, RTS, or DTR. This setting is ignored if ADCL is disabled.
- **ADCL Polarity:** When set to Low, ADCL Pin Select will be 0 when the transmit buffer is empty and 1 when the transmit buffer is full. When set to High, ADCL Pin Select will be 1 when the transmit buffer is empty and 0 when the transmit buffer is full.
- **nPin Wake Mask:** When enabled, UART will not generate a wake event when the WAKE pin is asserted.
- **nCTS Wake Mask:** When enabled, UART will not generate a wake event when the CTS pin is asserted while UART is in suspend.
- **Interrupt Wake Mask:** When enabled, UART will not generate a wake event when it receives an interrupt when not in suspend.
- **Snoop Latency Requirement:** Snoop latency is the time it takes a processor to access data in a cache in one of the peripherals. For more information on Snoop and no-Snoop, refer to PCI Express Base Specification Revision 4.0.

FIGURE 19: UARTX CONFIGURATION



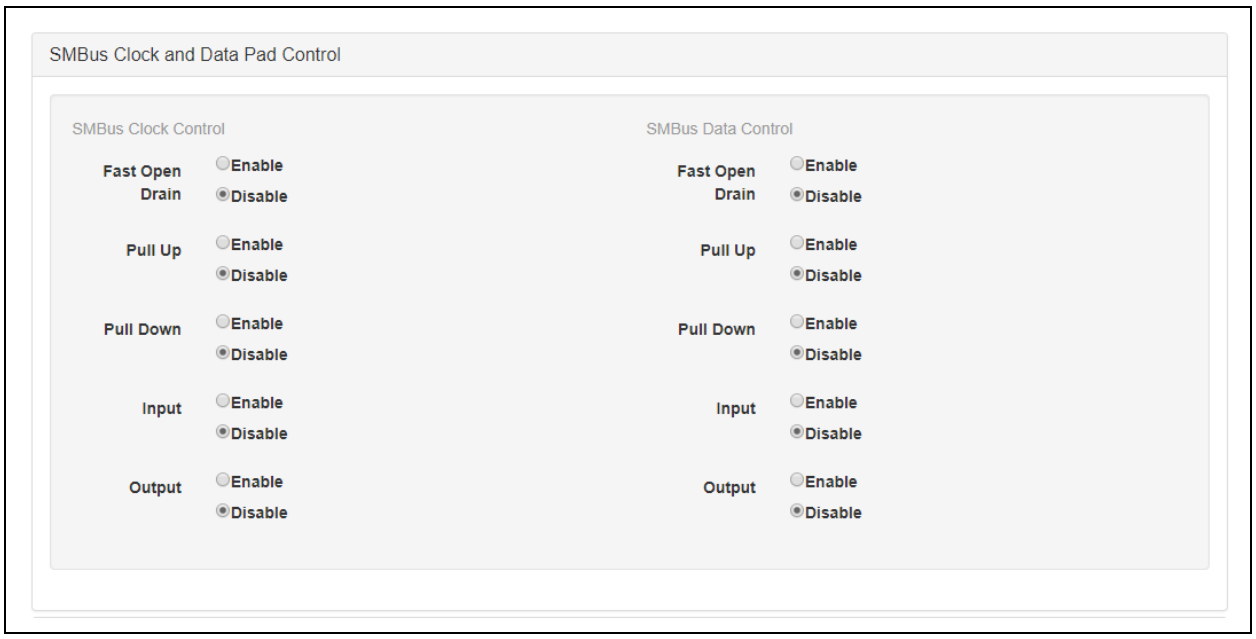
2.9.2 PERIPHERAL: SMBUS CONTROLLER

2.9.2.1 SMBus Clock and Data Pad Control

The SMBus Clock and Data Pad Control menu has the following options:

- **SMBus Clock Control:** Allows the user to set open-drain, pullup/pulldown resistors, and input/output settings for the SMBus clock pin.
- **SMBus Data Control:** Allows the user to set open-drain, pullup/pulldown resistors, and input/output settings for the SMBus Data pin.

FIGURE 20: SMBUS CLOCK AND DATA PAD CONTROL

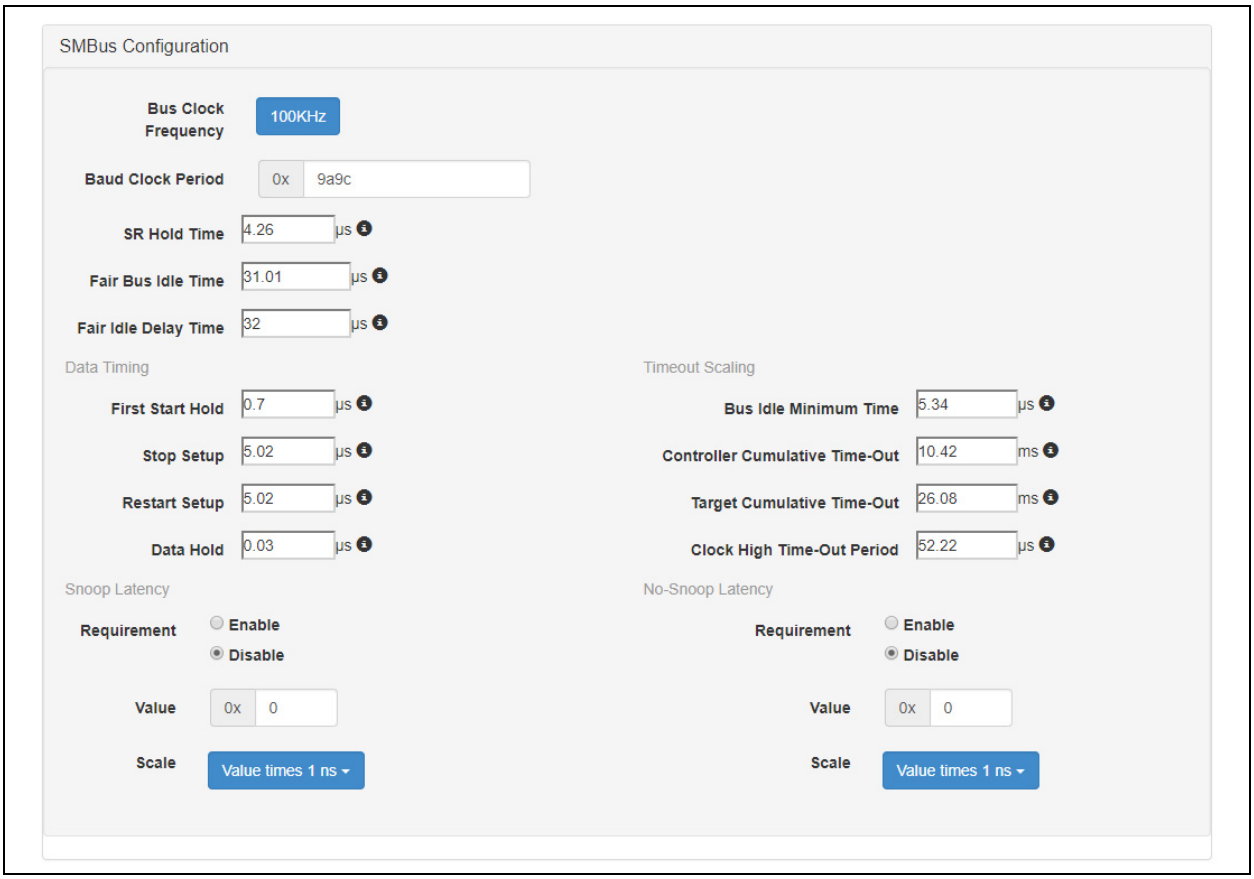


2.9.2.2 SMBus Configuration

SMBus Configuration has many variables that can be defined using the following:

- Bus Clock Frequency: The PCI1xxxx controller supports SMBus clock frequencies of 100 kHz, 400 kHz, and 1 MHz.
- Baud Clock Period: The upper byte defines the number of baud clock periods that make up the high phase of SCK. The lower byte defines the number of baud clock periods that make up the low phase of SCK.
- SR Hold Time: Holds the clock until the Hold time for the repeated start bit is satisfied.
- Fair Bus Idle Time: Delay before the start of a transaction.
- Fair Idle Delay Time: Delay required to satisfy the fairness protocol.
- First Start Hold: Determines the amount of time SCLK is held following the first start bit.
- Bus Idle Minimum Time: Sets the minimum amount of time between a stop condition and a start condition.
- Stop Setup: Determines the SDAT setup time from the rising edge of SCLK for a STOP condition.
- Controller Cumulative Time-Out: If SCK is held low for this time after a transaction with PCI1xxxx as the controller, the CCTO bit in the COMPLETION_REG register is asserted.
- Restart Setup: Determines the SDAT setup time from the rising edge of SCLK for a repeated START condition.
- Target Cumulative Time-Out: If SCK is held low for this time after a transaction with PCI1xxxx in SMBus target mode, the TCTO bit in the COMPLETION_REG register is asserted.
- Data Hold: Allows the user to set how long data is kept on the SDA line following SCK pulled low.
- Clock High Time-Out Period: Sets the timeout time when SCLK is 1. If SDAT is 1 when the timeout is reached, COMPLETION_REG.CHDH is asserted. If SDAT is 0 when the timeout is reached, COMPLETION_REG.CHDL is asserted.
- Snoop Latency Requirement: Snoop latency is the time it takes a processor to access data in a cache in one of the peripherals. For more information on Snoop and no-Snoop, refer to PCI Express Base Specification Revision 4.0.

FIGURE 21: SMBUS CONFIGURATION



2.9.3 PERIPHERAL: SPI CONTROLLER

2.9.3.1 SPI Controller Pad Control

SPI Alert is an input that can be used by an SPI peripheral to signal the PCI1xxxx.

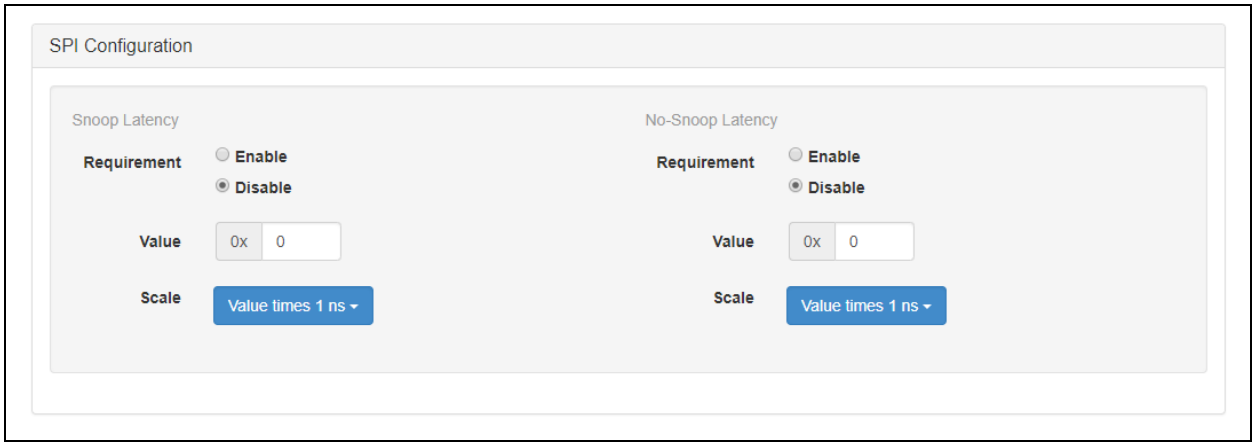
- **SPI Alert Control Debounce:** Enables an internal debouncer on the SPI Alert pin. This debouncer will pass the signal through to the host once the signal is stable for a certain period of time.
- **SPI Alert Control Pull-down:** Enables an internal pull down resistor on the SPI Alert pin.
- **SPI Alert Control Pull-up:** Enables an internal pull up resistor on the SPI Alert pin.
- **MOSI Pull-down:** Enables an internal pull down resistor on the SPI Data Out pin.

FIGURE 22: SPI CONTROLLER PAD CONTROL

2.9.3.2 SPI Configuration

Snoop Latency Requirement: Snoop latency is the time it takes a processor to access data in a cache in one of the peripherals. For more information on Snoop and no-Snoop, refer to PCI Express Base Specification Revision 4.0.

FIGURE 23: SPI CONFIGURATION



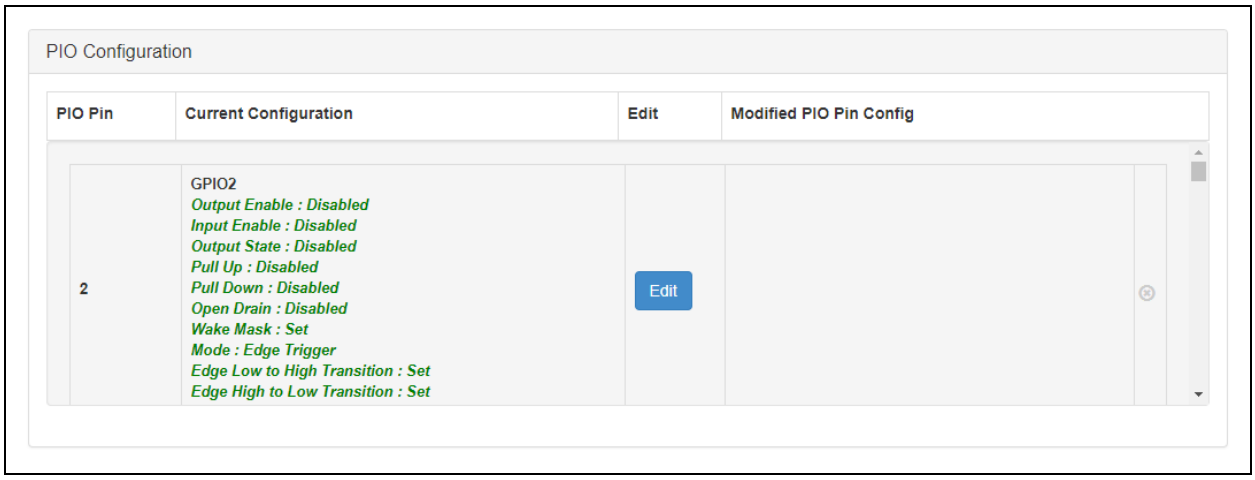
2.9.4 PERIPHERAL: GENERAL

2.9.4.1 PIO Configuration

Only PROG*X* pins that were configured as GPIO in *System Configuration>PF Pin Management* will appear in this list. Upon clicking *Edit,* the user is able to configure the following settings per pin:

- **Output:** This allows the user to set the GPIO pin as an output. Enabling Output will disable Input. Output must be enabled in order to be able to set the state of the GPIO pin during runtime.
- **Output State:** This option is only available when Output is enabled. Enable will pull the pin high once PCI1xxxx finishes configuration, Disable will keep the pin low once PCI1xxxx finishes configuration.
- **Input:** This allows the user to set the GPIO pin as an input. Enabling Input will disable Output.
- **Low to High Transition:** This option is only available when Input is enabled. This option allows for event triggers when the pin transitions from a low state to a high state. Set will allow event triggers to occur, Clear will prevent event triggers from occurring.
- **High to Low Transition:** This option is only available when Input is enabled. This option allows for event triggers when the pin transitions from a high state to a low state. Set will allow event triggers to occur, Clear will prevent event triggers from occurring.
- **Pull Up:** Enable configures the internal pull up resistor for the PROG*X* pin. Disable prevents the internal pull up resistor for the PROG*X* pin.
- **Pull Down:** Enable configures the internal pull down resistor for the PROG*X* pin. Disable prevents the internal pull down resistor for the PROG*X* pin.
- **Open Drain:** Enable sets the PROG*X* pin to open drain mode. Disable prevents open drain mode on the PROG*X* pin.
- **Wake mask:** Set enables an event to generate a wake event on the PROG*X* pin. Clear prevents an event from generating a wake event.

FIGURE 24: PIO CONFIGURATION



APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005104B (12-03-24)	All	Removed the “Advance Information” marking from the document. Updated heading format.
DS00005104A (08-16-23)	Initial release	

NOTES:

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Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.