PolarFire FPGA Wireless Radio Digital Front-End Design Application Note

AN5616

Introduction (Ask a Question)

This document describes the Microchip PolarFire® wireless radio Digital Front-End (DFE) design and how to run the demo using the PolarFire Evaluation Board, Microchip Wireless MIMO Daughter Card and a Remote Radio Head (RRH) Tester.

The demo design features:

- Baseband interface using the CPRI IP
- Signal processing, Digital Up-Conversion (DUC) and Digital Down-Conversion (DDC)
- RFIC interface using the JESD204B IP
- Mi-V soft processor and its peripheral interfaces — SPI, GPIO and UART. Microchip offers the Mi-V processor IP core and software tool chain to support RISC-V processor based designs.

This fully integrated demo design is created using Microchip Libero® SoC PolarFire to help customers build prototypes quickly.

The PolarFire Evaluation Board features:

- A 300K LE FPGA (MPF300TS, FCG1152) with 12.7 Gbps transceiver interface.
- DDR3 and DDR4 interfaces
- A high pin count FMC connector for plugging in expansion boards.

For more information, see the PolarFire Evaluation Kit page.

The wireless MIMO daughter card features:

- Two AD9371 RFIC chips for four transmit and four receive paths. Each chip supports:
  - 300 MHz to 6 GHz frequency range
  - Dual transmit and Dual receive paths
  - JESD204B digital interface
- AD9528, a two stage PLL with a JESD204B sysref generator.
- A high pin count (HPC) FMC connector to connect to an FPGA base board.

The RRH tester features:

- One-box solution including a Common Public Radio Interface (CPRI) and TX/RX paths.
- Send and receive digital IQ data to and from the RRH using CPRI optical connection.
- Software options for LTE FDD & TDD signal generation and analysis.

For more information, see www.keysight.com/find/E6610A.

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1. Design Requirements (Ask a Question)

The following table lists the design requirements for running the demo.

Table 1-1. Design Requirements

Requirements	Description
Hardware and Accessories	
PolarFire® Evaluation kit	MPF300-EVAL-KIT Kit Contents: • PolarFire Evaluation Kit Board with MPF300TS-1FCG1152I Device • 12V Power Pack/AC Adapter • USB 2.0 A male to Mini-B • QuickStart Card
MIMO Daughter Card	For details regarding MIMO Daughter Card, contact FPGA_marketing@microchip.com.
SFP+ Transceiver modules	Wavelength: 1310 nm Class 1 DFB laser Connector: LC duplex Max Link Length: 10 KM Max Data Rate: 10.5 Gbps Temperature Range: -40 °C to +85 °C
Fiber patch	Cable Type: single mode fiber with yellow 2 mm jacket Length: 3 M Connector: LC duplex
RF SMA cables	PASTERNACK SMA Female to SMA Female Cables
Host PC	Windows 10 OS
Serial Terminal Emulation Program	PuTTY
Software	
SoftConsole®	v2022.2
Test Hardware and Software	
Remote Radio Head Tester	E6610A (700 MHz to 2.7 GHz)
E6610A User Interface	v2.9.5 (2x2 LTE)

2. Prerequisites (Ask a Question)

Before you start, ensure that the following components are in place:

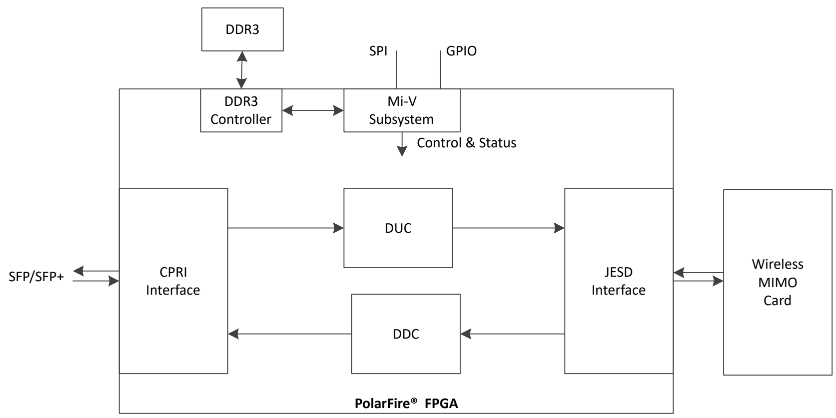
- Download the design files from: www.microchip.com/en-us/application-notes/an5616
- Download and install Libero SoC Design Suite from Libero SoC Software Downloads
- Download and install SoftConsole from: www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/soc-fpga/softconsole#downloads
- Download and install Microchip Power Monitor from the following link: ww1.microchip.com/downloads/aemDocuments/documents/FPGA/SOCDesignFiles/Polarfire_Eval_Kit_Power_Monitor.zip
- Download and install KEYSIGHT E6610A user interface from: http://www.keysight.com/find/E6610A_Software

3. Demo Design Architecture (Ask a Question)

The demo design supports a 4x4 MIMO, single carrier LTE 20 MHz bandwidth in the FDD mode. The basic system architecture consists of three main data modules— the CPRI IP, DUC and DDC blocks and the JESD204B IP. The Mi-V soft processor is used for controlling and monitoring functions.

The following figure shows the system architecture of the demo design.

Figure 3-1. PolarFire Wireless Radio DFE Design Architecture



The following points describe the high-level data flow in the design:

1. The transmit IQ data from the baseband module is received on the RX port of the CPRI IP and is de-mapped to four antenna carriers. This data is time-division multiplexed in the format required by the DUC chain.
2. The DUC block up-samples and up-converts the received data and then sends it to the JESD204B transmit interface.
3. Similarly, the JESD204B receive interface receives the data from the RFIC module and sends it to DDC for down-conversion and down-sampling.
4. The down-sampled data is then mapped to the four antenna carriers and sent to the TX port of the CPRI IP.

3.1 Subsystem Components (Ask a Question)

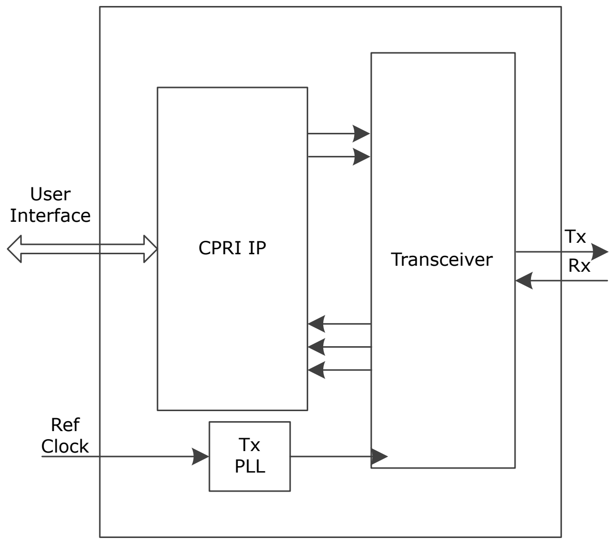
The following sections describe the subsystems used in the design.

3.1.1 CPRI Interface (Ask a Question)

The CPRI IP is configured as a slave at 4.9 Gbps line rate with four antenna carriers (AxC), each carrying 20 MHz LTE bandwidth.

The following figure shows the CPRI interface.

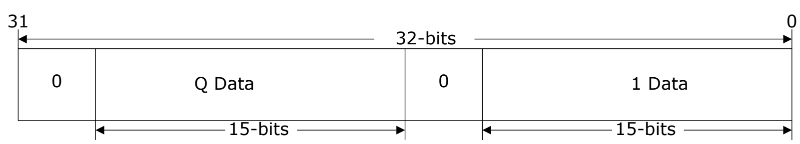
Figure 3-2. CPRI Interface



The following points lists the port configurations of the CPRI IP:

- The TX and RX AxC data plane ports are enabled
- The Ethernet TX and RX ports are disabled
- The vendor specific data and AxC control data ports are looped back
- The I and Q samples of each AxC are fixed at 15 bits
- The user interface width is fixed at 32-bits. With zero appending on MSB, 15-bit wide I and Q samples are bit-stuffed in the 32-bit user interface width as shown in the following figure.

Figure 3-3. I and Q Patterns

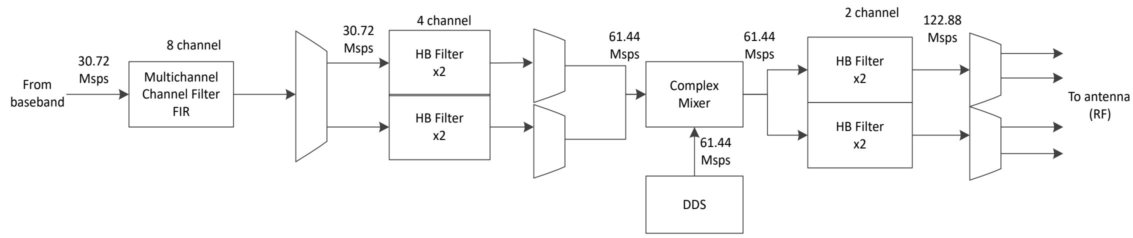


The transceiver data rate is set to 4.9 Gbps. For more information about the CPRI IP, see UG0822: CPRI IP User Guide.

3.1.2 DUC and DDC (Ask a Question)

The DUC and DDC blocks are designed to support a single carrier LTE with 20 MHz bandwidth. These blocks are clocked at 245.76 MHz. The following figure shows the DUC structure for two antenna carriers. The same structure is replicated for the other two antenna carriers.

Figure 3-4. DUC

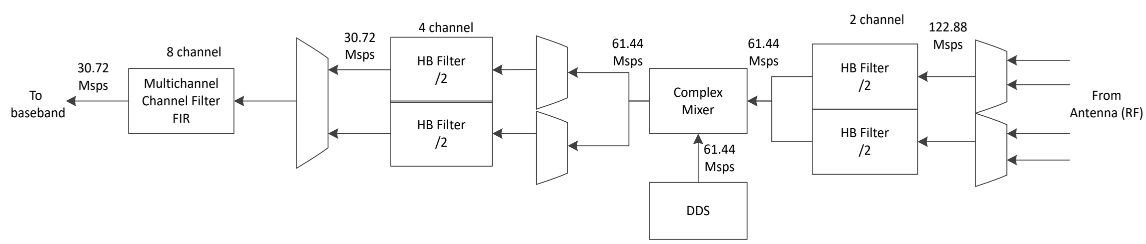


DUC contains a cascaded series of filters, which up-convert a 30.72 Msps sample rate to 122.88 Msps as per the following process.

1. The channel filter is a multi-channel FIR structure with 8 channels sampled at 30.72 Msps.
2. The two 4-channel half-band interpolation filters double the sample rate to 61.44 Msps.
3. The complex mixer and Direct Digital Synthesizer (DDS) are used for up-conversion.
4. The output of the complex mixer is passed to the two 2-channel half-band interpolation filters to increase the sample rate to 122.88 Msps.

The following figure shows the DDC structure.

Figure 3-5. DDC



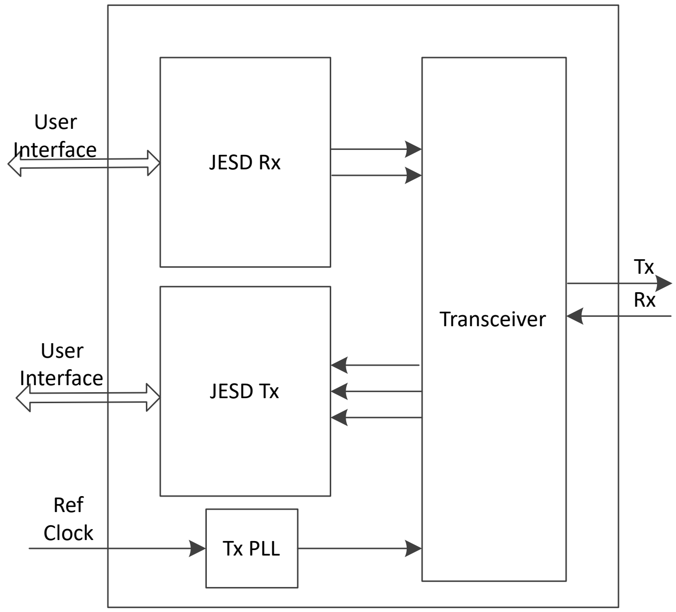
The DDC contains a cascaded series of filters, which down-convert a 122.88 Msps sample rate to 30.72 Msps as per the following process:

1. The two 2-channel half-band decimation filters convert the sample rate from 122.88 Msps to 61.44 Msps.
2. The complex mixer and DDS blocks are used for down-conversion.
3. The output of the complex mixer is passed to the next two 4-channel half-band decimation filters to reduce the sample rate to 30.72 Msps.
4. The output of the decimation filters is passed to the multi-channel FIR structure with 8 channels sampled at 30.72 Msps.

3.1.3 JESD204B Interface (Ask a Question)

The JESD204B subclass 1 transmit and receive IPs are used at 4.9 Gbps rate. The JESD204B interface is configured to interface with the AD9371 RFIC. The following figure shows the JESD204B blocks.

Figure 3-6. JESD204B Interface



For each AD9371, the design includes a pair of JESD204B TX and RX blocks. The transceiver is configured for:

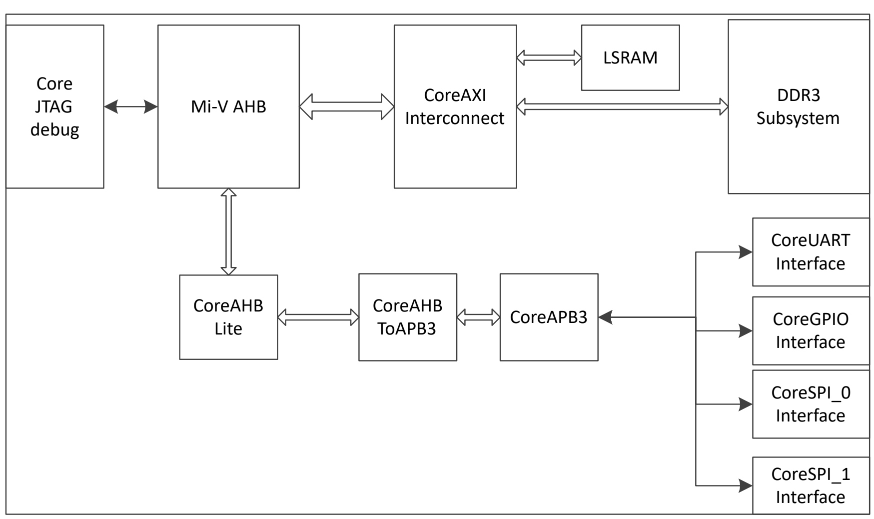
- Two lanes at 122.88 MHz clock—each lane carries 32-bit IQ data for a mixed signal converter.
- A 32-bit PCS interface.

For more information about the JESD204B TX and RX IPs, see CoreJESD204BTX Handbook and CoreJESD204BRX Handbook.

3.1.4 Processor Subsystem (Ask a Question)

The Mi-V soft processor operates at 111.111 MHz and executes the user application code from an external DDR3. The following figure shows the Mi-V based processor system and its interfaces.

Figure 3-7. Mi-V Processor Subsystem



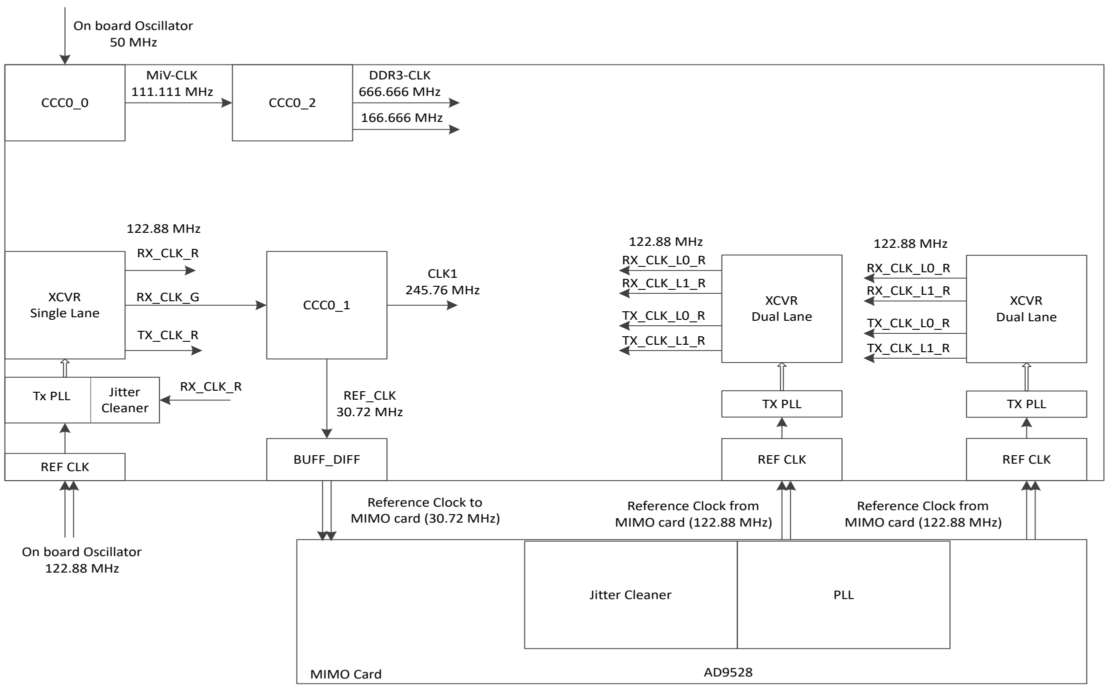
As shown in preceding figure, the Mi-V subsystem is used to initialize and monitor the CPRI IP through the AHB bus, and the external RFICs via the SPI interface. CoreSPI_0 is used to configure AD9528 and one RFIC chip (AD9371). CoreSPI_1 is used to configure the other RFIC chip. The CoreGPIO interface is used for the soft reset of the JESD204B interface. The CoreUART interface is reserved for internal design debugging.

For more information about how to build the Mi-V subsystem, see AN4997: PolarFire FPGA Building a Mi-V Processor Subsystem.

3.2 Clocking Structure (Ask a Question)

The clocking structure in the demo design is shown in the following figure.

Figure 3-8. Clocking Structure



As shown in the preceding figure, the following points summarize the clocking structure:

- In the CPRI interface, the transceiver clock settings are as follows:
  - TX clock is set to Regional (TX_CLK_R) and the RX clock is set to Global (shared). As a result, both the RX regional (RX_CLK_R) and RX global (RX_CLK_G) clocks are enabled.
  - The jitter cleaner feature is enabled in the TX PLL. The jitter cleaner derives its reference from the transceiver recovered clock to synchronize the TX_CLK clock.
- The global RX clock serves as the reference to all the data modules in the system
- The CPRI interface uses the RX_CLK_R and TX_CLK_R (122.88 MHz) clocks
- The DUC and DDC blocks use the 245.76 MHz clock generated from the CCC0_1
- CCC0_1 also generates a 30.72 MHz fabric clock that is used as the reference clock by AD9528
- Using the 30.72 MHz reference clock, AD9528 generates the 122.88 MHz reference clock for JESD204B
- The Mi-V subsystem uses the 111.111 MHz clock generated from CCC0_0
- Using 111.111 MHz as the reference, the CCC0_2 block generates 666.666 MHz and 166.666 MHz clocks for the DDR3 block.

The following table lists all of the clocks used in the design, their source, frequency and purpose.

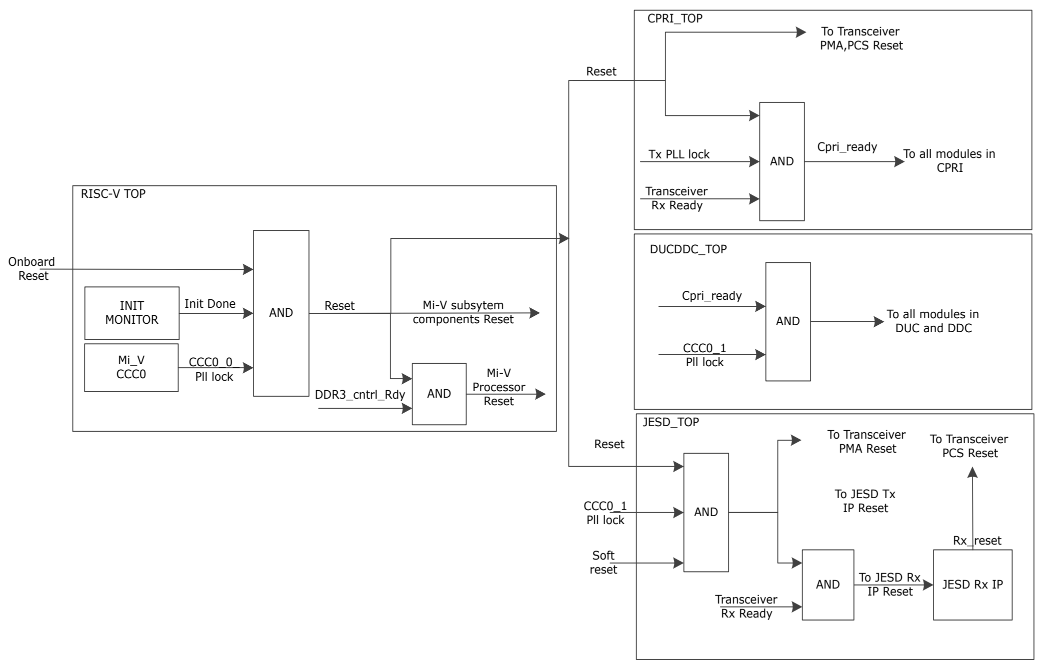
Table 3-1. Clocks

Clock Name	Source	Frequency	Purpose
Mi-V_CLK	CCC0_0	111.111 MHz	Mi-V processor clock
DDR3-CLK	CCC0_2	666.666 MHz 166.666 MHz	DDR3 clocks
RX_CLK_G	Transceiver RX recovered clock	122.88 MHz	CPRI RX
TX_CLK_G	Transceiver TX PLL	122.88 MHz	CPRI TX
RX_CLK_R	Transceiver RX recovered clock	122.88 MHz	CPRI RX
CLK1	CCC0_1	245.76 MHz	DUC and DDC
REF_CLK	CCC0_1	30.72 MHz	Reference clock to the MIMO card
RX_CLK_L0_R	Transceiver RX recovered clock (Lane 0)	122.88 MHz	JESD204B RX
RX_CLK_L1_R	Transceiver RX recovered clock (Lane 1)	122.88 MHz	JESD204B RX
TX_CLK_L0_R	Transceiver TX PLL (Lane 0)	122.88 MHz	JESD204B TX
TX_CLK_L1_R	Transceiver TX PLL (Lane 1)	122.88 MHz	JESD204B TX

3.3 Reset Structure (Ask a Question)

The reset structure in the demo design is shown in the following figure.

Figure 3-9. Reset Structure



As shown in the preceding figure, the following points summarize the reset structure of the design:

- The reset signal from the RISC-V top module drives the reset of all the other modules in the design
- The onboard push button reset, device initialization init_done and the PLL lock signals generate the reset signal (Reset) for all the components of the Mi-V subsystem.
- TX_PLL and transceiver RX_Ready signals in CPRI are ANDed with the Mi-V Reset to generate the reset signal (Cpri_ready) for all of the components of the CPRI top module.
- The Mi-V reset signal also resets the CPRI transceiver
- Cpri_ready and PLL lock signals generate the reset signal for the DDCDUC_TOP module

- Mi-V reset, PLL lock and soft reset signals generate the reset for all the components in the JESD_TOP module.

3.4 Resource Utilization (Ask a Question)

The following table lists the resource utilization of the design on the MPF300TS device (FCG1152, speed grade -1).

Table 3-2. Resource Utilization

Type	Used	Total	Percentage (%)
4LUT	79298	299544	26.47
DFF	73655	299544	24.59
µSRAM	1315	2772	47.44
LSRAM	116	952	12.18
Math	326	924	35.28
PLL	3	8	37.5
Transceiver Lanes	5	16	31.25

3.5 Timing Closure in Libero (Ask a Question)

In Libero® SoC PolarFire, the timing constraints are derived for the top module of the design from **Design Flow** > **Constraint Manager**. The generated SDC file includes clock definitions based on the PLLs used in the design and constraints specific to IP cores. Timing issues can be analyzed and cross-probed using SmartTime and ChipPlanner. These applications are integrated in Libero SoC PolarFire.

To close the timing of the wireless radio DFE design at 245 MHz, the following options and guidelines were followed:

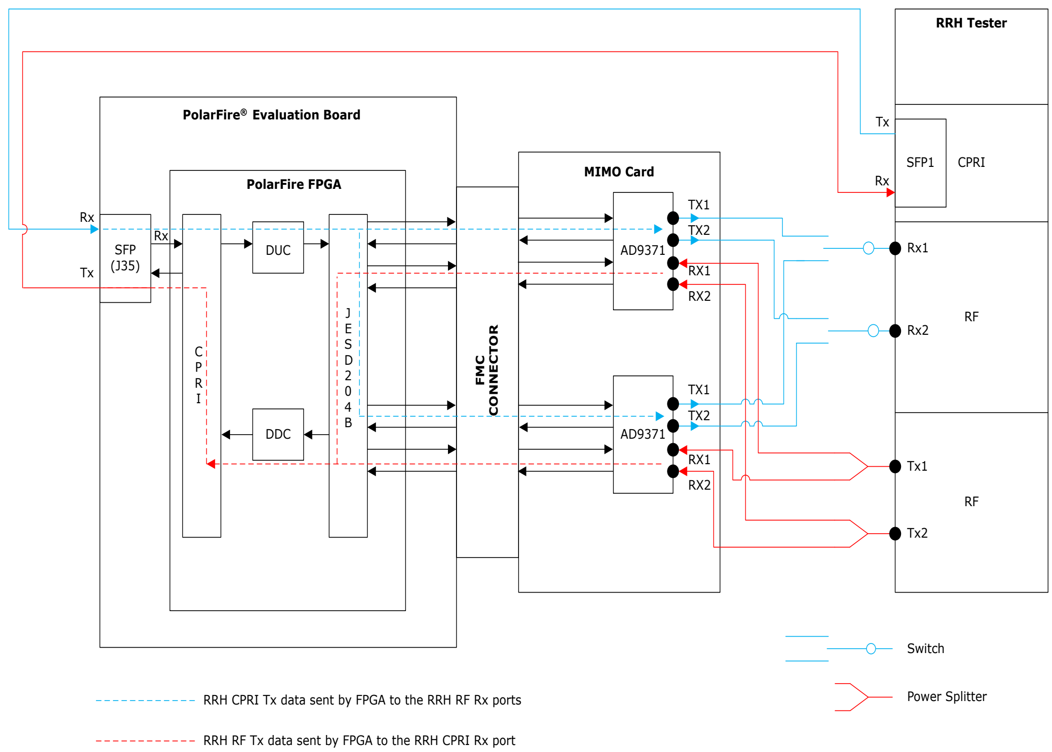
- The input and output data registers of hard blocks such as MACC and RAM were enabled in the RTL. Also, used dedicated CDIN and CDOUT lines for the MACC blocks.
- The syn_preserve directive was used in the RTL of repetitive modules inside DUC and DDC subsystems. This directive avoids the usage of shared nets across modules and duplicates nets for each module to give better timing.
- Asynchronous resets were used in the design
- The required synchronizer circuitry was used for clock domain crossings. And then, all of the asynchronous clock groups were defined (set_clock_groups) in an SDC file for faster place and route cycles.
- Using SmartTime results, the maximum fanout limit was set on individual nets instead of setting the fanout for the overall design.

Important: The **Place and Route** configuration options, **High Effort Layout** and **Repair Minimum Delay Violations** must be enabled only when the timing paths have a lower negative slack with respect to the clock timing constraint. The smart time analysis must be done with these options disabled during initial runs.

4. Hardware Data Flow (Ask a Question)

The following figure shows the high-level data flow between the RRH tester, MIMO card and the PolarFire evaluation board.

Figure 4-1. Data Flow



5. Setting up the Demo (Ask a Question)

This section describes steps to successfully program the FPGA, its Non-volatile memory (sNVM), and run scripts to configure Jitter attenuator PLLs. Setting up the demo involves the following steps:

- Setting up the Hardware
- Programming the PolarFire Device
- Enabling Jitter Cleaner on CPRI TX PLL

5.1 Setting up the Hardware (Ask a Question)

This section describes how to connect all of the components required to run the demo. To setup the hardware, perform the following steps:

1. Connect the USB cable from the Host PC to **J5** (FTDI port) on the evaluation board.
2. Connect the Host PC and the RRH tester to the same LAN using RJ45 cables.
   On the evaluation board, DS15, DS24, DS23, DS25 and DS26 LEDs glow.
3. Plug in one SFP module into the SFP1 port of the RRH tester and the other SFP module into **J35** (SFP case) on the evaluation board. Connect both these SFP modules using the fiber patch.
4. Connect the MIMO card to the evaluation board using the **J34** FMC connector.
5. Connect the two RRH RF TX ports to the 4 RF RX ports of the MIMO using power splitters as listed in the following table.

Table 5-1. RRH RF TX to MIMO RF RX Connections

RRH TX Port	MIMO Card RX Port
TX1	J500 (RX1 of U12) and J522 (RX1 of U15)
TX2	J501 (RX2 of U12), J519 (RX2 of U15)

6. Connect the two RF TX ports of the MIMO card to the two RX ports of the RRH tester as listed in the following table.

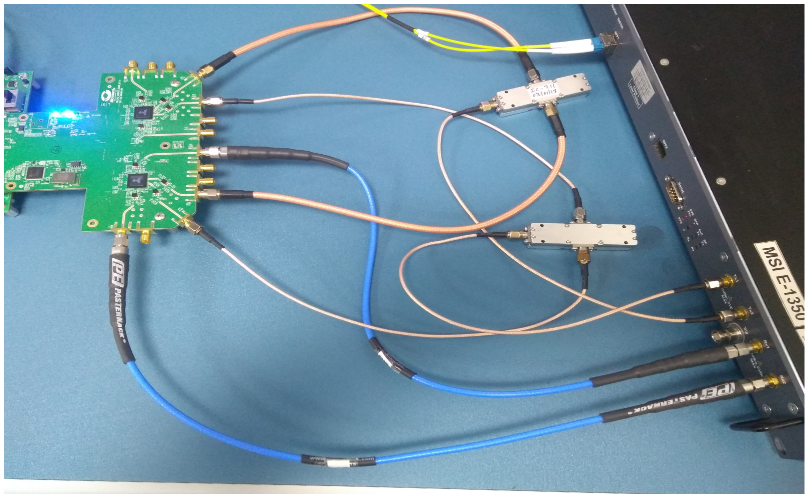
Table 5-2. MIMO RF TX to RRH RF RX Connections

MIMO Card TX Port	RRH RX Port
TX1 (J508) of U12	RX1
TX2 (J509) of U12	RX2

Important: To see the RF output from the TX1 and TX2 ports U15 of the MIMO card, connect TX1 (J524) and TX2 (J526) to RX1 and RX2 ports.

The following shows the complete SMA connections.

Figure 5-1. SMA Connections



7. Ensure that the following jumper settings listed are made on the evaluation board.

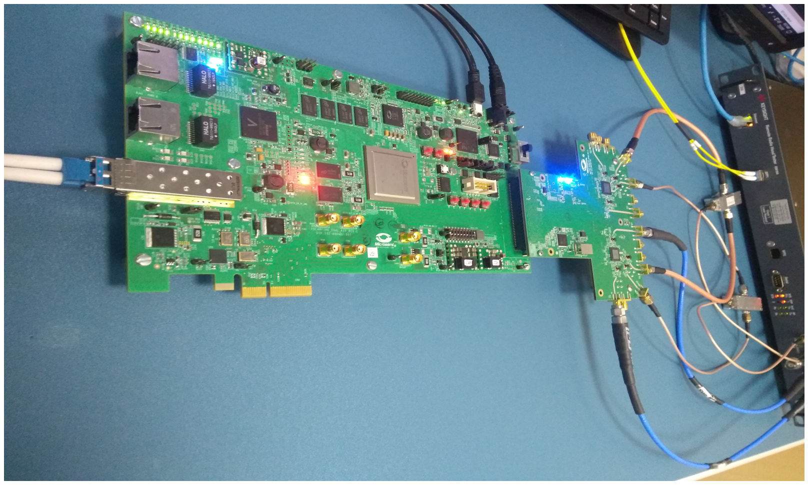
Table 5-3. Jumper Settings

Jumper	Setting
J39	Short 1 and 2 for enabling the TX port of the SFP
J46	Open 1 and 2 for enabling the 122.88 MHz oscillator
J47	Open 1 and 2
J12	short 5 and 6 for 1.8V

8. Connect the power supply cable to the **J9** connector on the evaluation board.
9. Connect the RRH tester to the power supply using the power adapter.
10. Power-up the evaluation board using the **SW3** slide switch.
    On the evaluation board, the power regulator LEDs (DS3 - DS14) glow. And, LEDs DS4 and DS8 on the MIMO card also glow.
11. Power-up the RRH tester using the **POWER** switch at the back chassis.
    After the RRH tester initialization, LEDs SYS PLL, AxC TX and RX glow, RF TX and RX glow and STS blinks.

The complete setup is shown in the following figure.

Figure 5-2. Hardware Setup



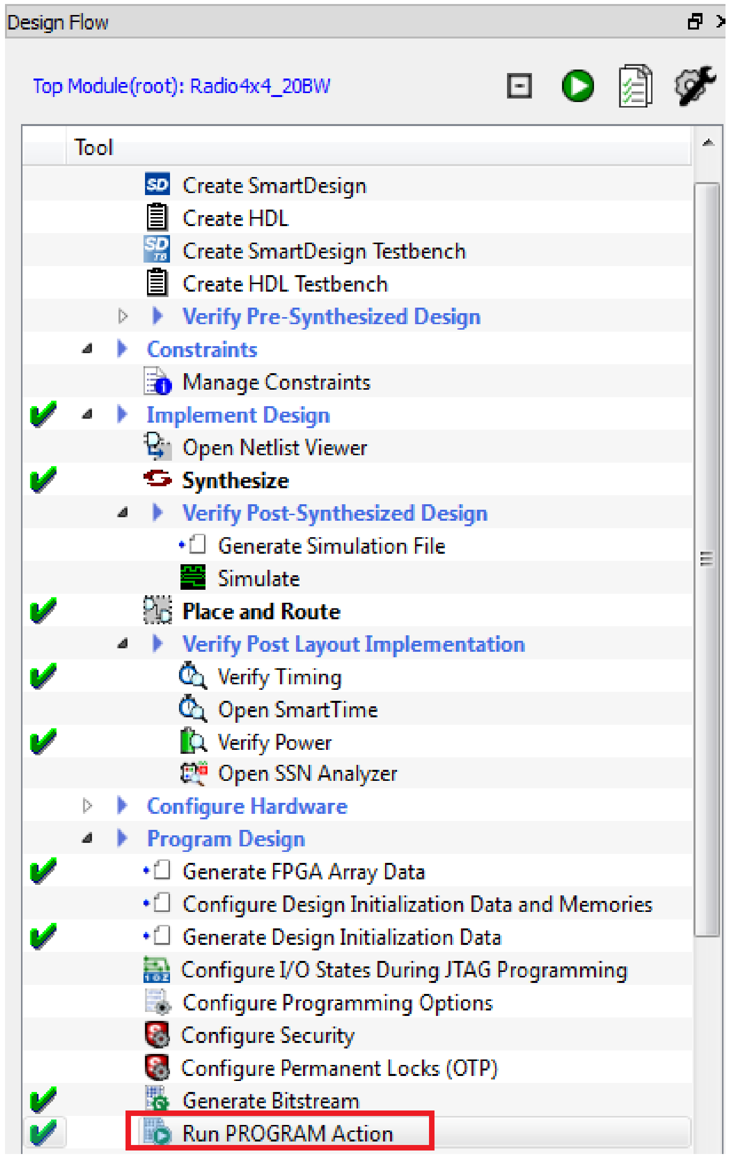
5.2 Programming the PolarFire Device (Ask a Question)

After setting up the hardware, you must program the device.

To program the device, perform the following steps:

1. Once the design is created through TCL scripts as mentioned in Appendix A: Running the TCL Script, open the design in the Libero SoC software.
2. Double-click Run PROGRAM Action option from the Libero Design Flow, as shown in the following figure. The following message appears after the device is successfully programmed.

Figure 5-3. Design Flow



LED 10 glows and LED 11 blinks after the device is successfully programmed.

Important:
Keep Libero SoC PolarFire open to enable jitter cleaner as described in the following section.

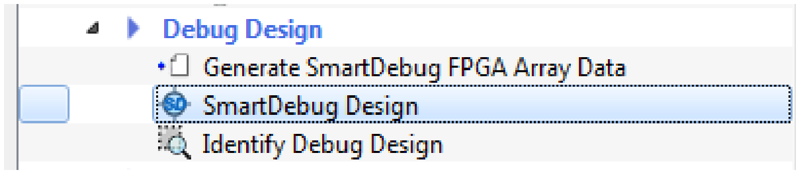
5.3 Enabling Jitter Cleaner on CPRI TX PLL (Ask a Question)

The design files includes a TCL script file, which enables jitter cleaner on CPRI TX PLL. The script must be executed using SmartDebug.

To execute the script, perform the following steps:

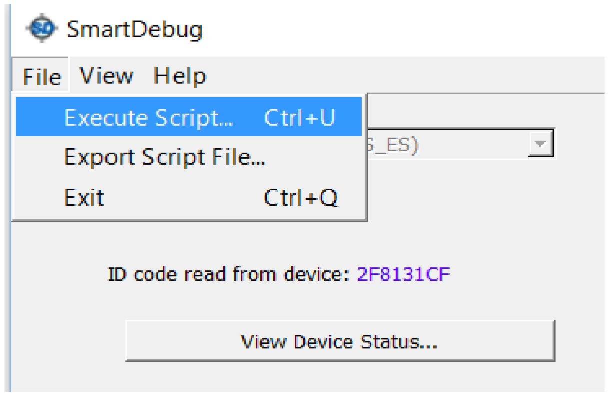
1. From the Libero design flow, double-click the **SmartDebug Design** option.

Figure 5-4. Starting SmartDebug



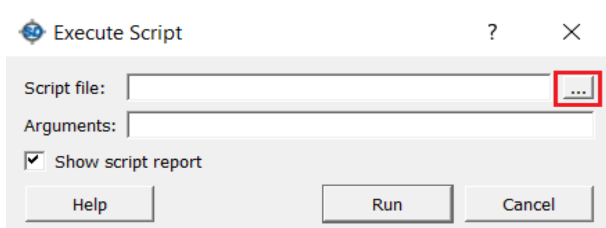
2. Select **FileExecute Script** as shown in the following figure.

Figure 5-5. Execute Script



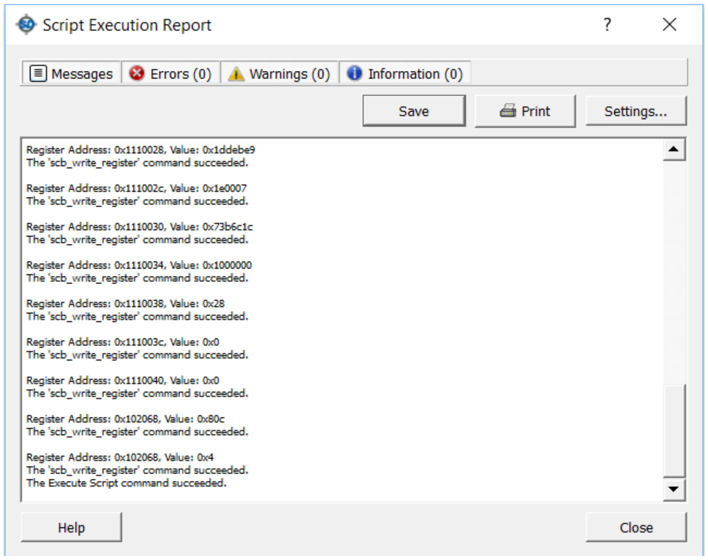
3. Click the **Import** button to import the TCL file, as shown in the following figure.

Figure 5-6. Import Button



4. Double-click the `CPRI_JA_Enable.tcl` file from the following location `mpf_an5616_df\HW\src\cfg`, and click **Run**.
After the successful execution of the script, the log window shows the following report.

Figure 5-7. Execution Report



5. Close SmartDebug.

Important: Run the script every time the evaluation board is power cycled.

6. Running the Demo (Ask a Question)

This section describes steps to successfully run the demo and observe the 64 QAM constellation of a 2x2 20 MHz MIMO system.

Running the demo involves the following steps:

- Configuring and Monitoring the RRH Tester
- Executing the User Application
- Monitoring the Performance

6.1 Configuring and Monitoring the RRH Tester (Ask a Question)

The E6610A user interface is used to configure the carrier technology and bandwidth, CPRI parameters like line rate, bit width and IQ mapping, and to configure the RF parameters like frequency, waveform and power levels (for TX and RX). The user interface is also used to monitor the RRH tester. Monitoring the tester involves observing the analog and digital data at RF RX and CPRI RX respectively.

This section is divided into the following steps:

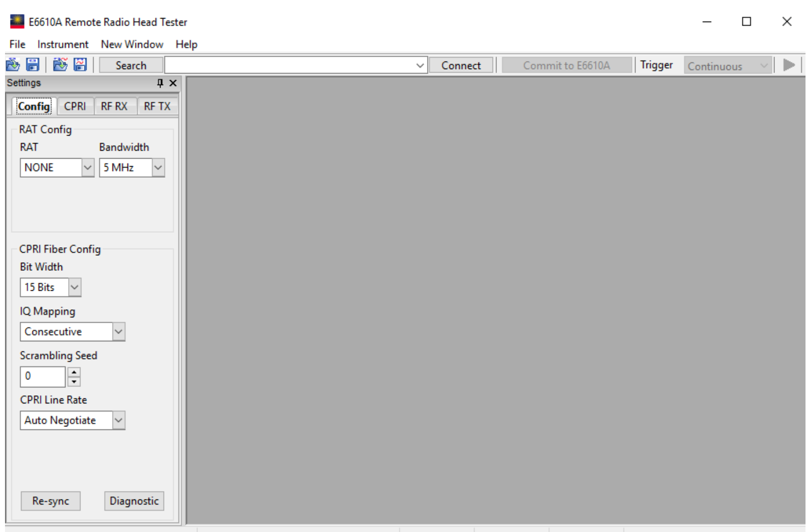
- Configuring the Tester
- Monitoring the Tester
- Enabling Multicast on CPRI

6.1.1 Configuring the Tester (Ask a Question)

To configure the RRH tester, perform the following steps:

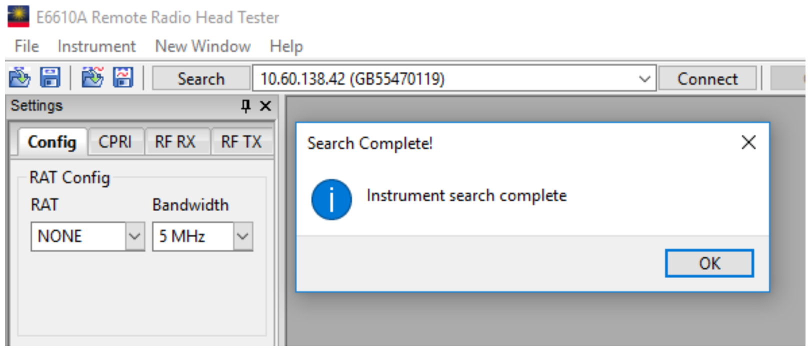
1. From the host PC desktop, start the E6610A user interface.
   The main window of the user interface is displayed as shown in the following figure.

   Figure 6-1. User Interface

2. Click Search to detect the RRH tester connected to the LAN.
   The IP address of the RRH tester and the following message is displayed as shown in the following figure.

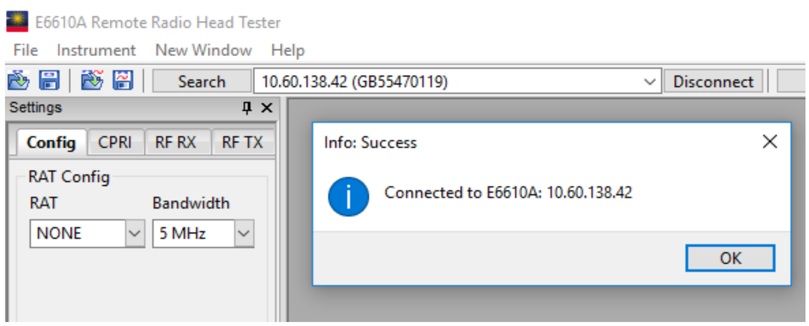
Figure 6-2. Instrument Detected



Important: The IP address of the RRH tester varies from one LAN to the other.

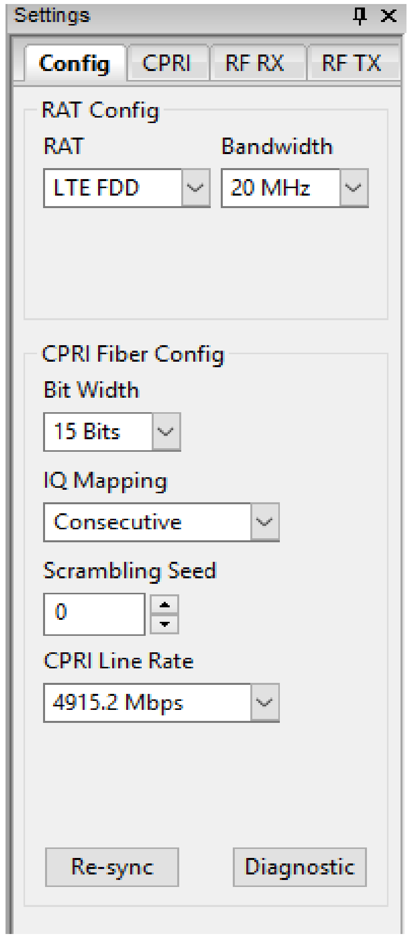
3. Click Connect to connect to the RRH tester. The following message is displayed after a successful connection.

Figure 6-3. Connection Established



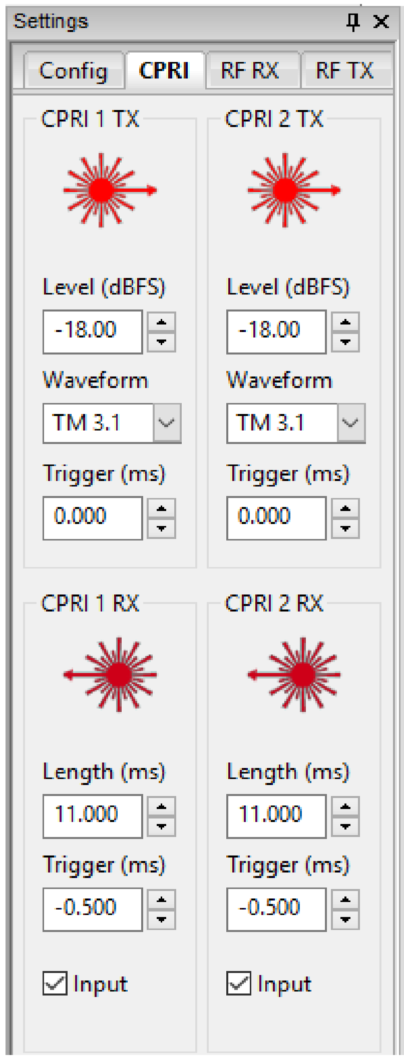
4. Configure the carrier technology, bandwidth and CPRI parameters as shown in the following figure.

Figure 6-4. Config Window



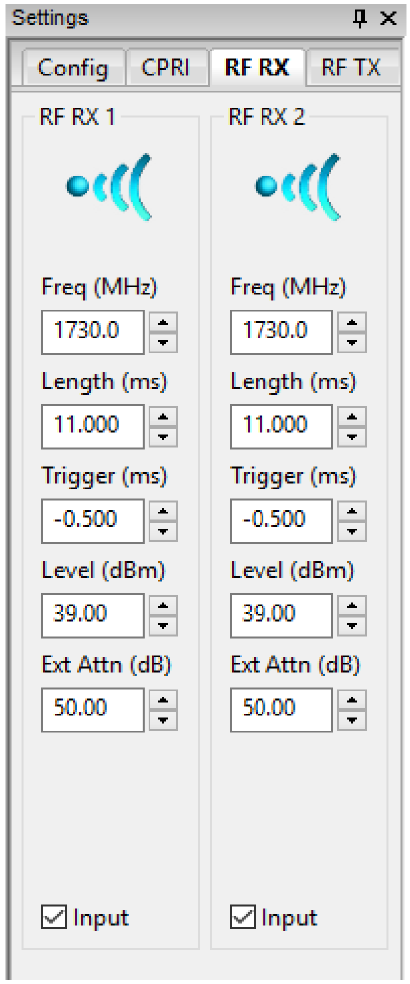
5. Configure the CPRI TX and RX parameters as shown in the following figure.

Figure 6-5. CPRI TX and RX Config Screen



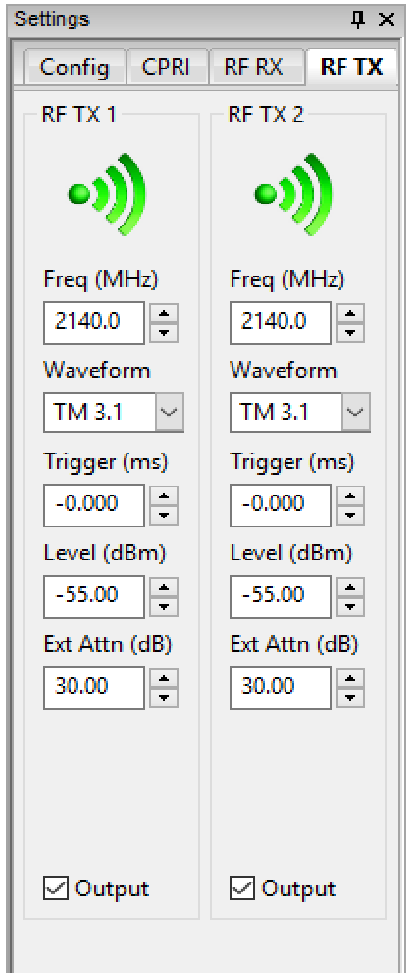
6. Configure the RF RX parameters as shown in the following figure.

Figure 6-6. RF RX Config Screen



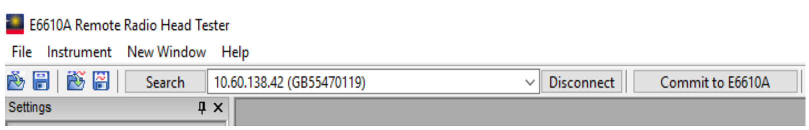
7. Configure the RF TX parameters as shown in the following figure.

Figure 6-7. RF TX Config Screen



8. To commit the configuration, click **Commit to E6610A**.

Figure 6-8. Commit Configuration



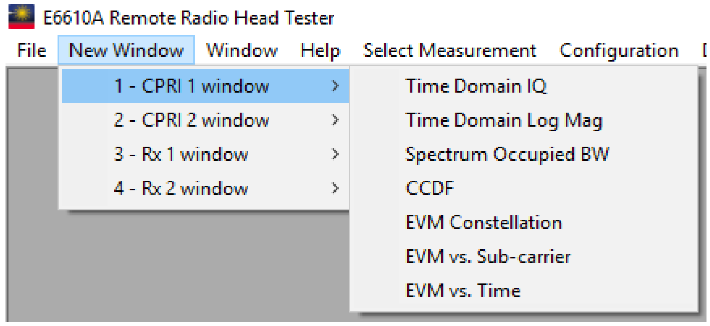
6.1.2 Monitoring the Tester (Ask a Question)

The time domain, frequency domain, and the EVM constellation plots of the data received at the CPRI RX and RF RX ports must be observed. These windows must be opened to view the various plots.

Follow these steps:

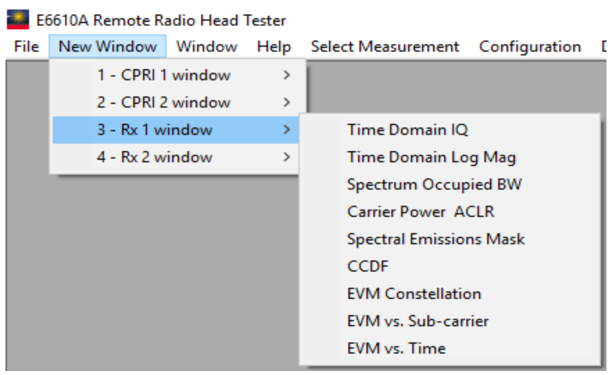
1. Select **New Window** > **CPRI 1** > **Time Domain IQ**, as shown in the following figure.

Figure 6-9. CPRI 1 RX Plot Window



2. Similarly, open the CPRI 1 RX frequency domain, and EVM constellation plot windows.
3. Similarly, open the CPRI 2 RX time and frequency domain, and EVM constellation plot windows
4. Select **New Window** > **RX 1** > **Time Domain IQ**, as shown in the following figure.

Figure 6-10. RF RX Plot Window



5. Similarly, open the RF RX1 frequency domain, and EVM constellation plot windows.
6. Similarly, open the RF RX2 time and frequency domain, and EVM constellation plot windows.
7. Select **New Window** > **CPRI Diagnostics** to monitor the CPRI link.

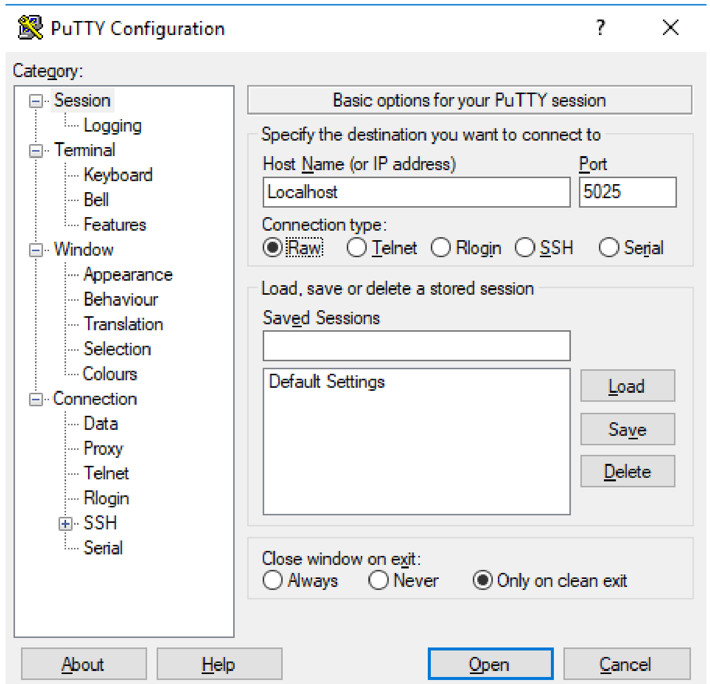
6.1.3 Enabling Multicast on CPRI (Ask a Question)

The RRH tester supports Multicast in the down link. The multicast feature creates copies of the CPRI 1 and CPRI 2 IQ data streams and places them in the additional antenna containers that the RRH can use to map to other antenna ports. Multicast is used in the demo to get the CPRI 1 and 2 IQ data on the other 2 antennas.

From the host PC, PuTTY must be used to connect to the tester. After connecting, multicast must be enabled on CPRI. To enable multicast, perform the following steps:

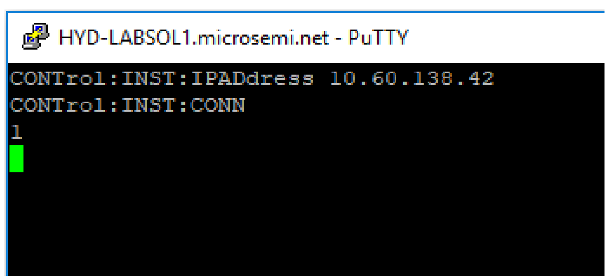
1. From the host PC desktop, start PuTTY.
2. Enter the hostname, port number and select the **Connection Type** as shown in the following figure.

Figure 6-11. PuTTY Connection Config



3. Type the commands shown in the following figure and click **Enter** to connect to the Tester. After connecting, the return code 1 is displayed as shown in the following figure.

Figure 6-12. Connection Established



4. Copy multicast commands as shown in the following figure and paste it on PuTTY.

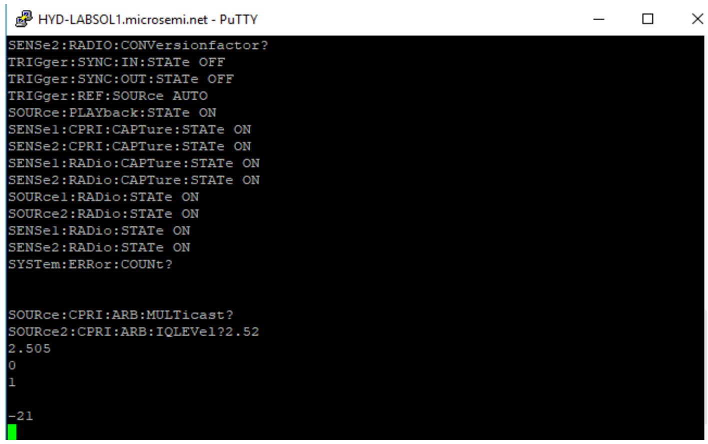
Figure 6-13. Multicast Commands

```
*CLS
SOURce:PLAYback:STATe OFF
CONFigure:RAT:TYPE LTE
CONFigure:RAT:MODE FDD
CONFigure:RAT:BW  20,consecutive
CONFigure:CPRI:BITwidth 15
SOURce:CPRI:MODe consecutive
SOURce:CPRI:ARB:MULTicast ON
SOURce1:RADio:ARB:TMODel TM31
SOURce1:RADio:MODe modulated
SOURce1:RADio:ARB:STATe ON
CONFigure:SEMask CATBOPT2
SOURce1:RADio:ARB:TRIGger -0.000000
SOURce1:RADio:CORRection 30.000000
SOURce1:RADio:FREQuency 2140000
SOURce1:RADio:POWer -55.000000
CONFigure:TXSpurious1:RBW 1
SENSe1:RADio:FREQuency 1730000
SENSe1:RADio:CORRection 50.000000
SENSe1:RADio:LEVel 39.000000
SENSe1:RADio:CAPTure:DEPth 11.000000
SENSe1:RADio:CAPTure:TRIGger -0.500000
SENSe1:RADIO:CAPTure:TMODEL TM31
SOURce1:CPRI:ARB:IQLEVel -21.000000
SOURce1:CPRI:ARB:TRIGger 0.000000
SOURce1:CPRI:ARB:TMODel TM31
SOURce1:CPRI:ARB:STATe ON
SENSe1:CPRI:CAPTure:DEPth 11.000000
SENSe1:CPRI:CAPTure:TRIGger -0.500000
SENSe1:RADIO:CONVersionfactor?
SOURce2:RADio:ARB:TMODel TM31
SOURce2:RADio:MODe modulated
SOURce2:RADio:ARB:STATe ON
CONFigure:SEMask CATBOPT2
SOURce2:RADio:ARB:TRIGger -0.000000
SOURce2:RADio:CORRection 30.000000
SOURce2:RADio:FREQuency 2140000
SOURce2:RADio:POWer -55.000000
CONFigure:TXSpurious2:RBW 1
SENSe2:RADio:FREQuency 1730000
SENSe2:RADio:CORRection 50.000000
SENSe2:RADio:LEVel 39.000000
SENSe2:RADio:CAPTure:DEPth 11.000000
SENSe2:RADio:CAPTure:TRIGger -0.500000
SENSe2:RADIO:CAPTure:TMODEL TM31
SOURce2:CPRI:ARB:IQLEVel -21.000000
SOURce2:CPRI:ARB:TRIGger 0.000000
SOURce2:CPRI:ARB:TMODEL TM31
SOURce2:CPRI:ARB:STATe ON
SENSe2:CPRI:CAPTure:DEPth 11.000000
SENSe2:CPRI:CAPTure:TRIGger -0.500000
SENSe2:RADIO:CONVersionfactor?
TRIGger:SYNC:IN:STATe OFF
TRIGger:SYNC:OUT:STATe OFF
TRIGger:REF:SOURCE AUTO
SOURce:PLAYback:STATe ON
SENSe1:CPRI:CAPTure:STATe ON
SENSe2:CPRI:CAPTure:STATe ON
SENSe1:RADio:CAPTure:STATe ON
SENSe2:RADio:CAPTure:STATe ON
SOURce1:RADio:STATe ON
SOURce2:RADio:STATe ON
SENSe1:RADio:STATe ON
SENSe2:RADio:STATe ON
SYSTem:ERRor:COUNt?


SOURce:CPRI:ARB:MULTicast?
SOURce2:CPRI:ARB:IQLEVel?
```

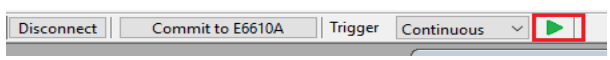
The following figure shows the status and return codes displayed after multicast is successfully enabled.

Figure 6-14. Multicast Enabled



5. To start the CPRI and RF traffic from the tester, click **Run** icon as shown in the following figure.

Figure 6-15. Start Tester Traffic



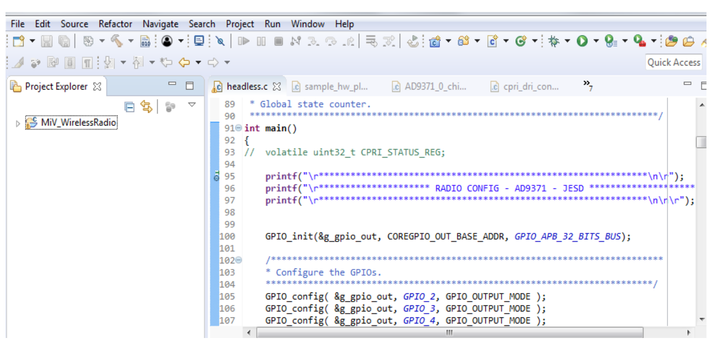
6.2 Executing the User Application (Ask a Question)

Using SoftConsole, the user application must be launched in the debug mode. CPRI registers and devices on the MIMO card are initialized after the debugger executes the main function. The main function also monitors the CPRI link.

To execute the user application, perform the following steps:

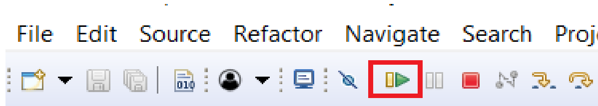
1. From the host PC desktop, start SoftConsole v2022.2.
2. In the workspace launch window, enter the following location and click **Launch**.
   `mpf_an5616_df\FW\softconsole`
3. The user application is launched in the debug mode.
4. Click the debug option, as shown in the following figure.

Figure 6-16. Launch Debugger



5. In the debug window, click the **Resume** icon to execute the main function as shown in the following figure.

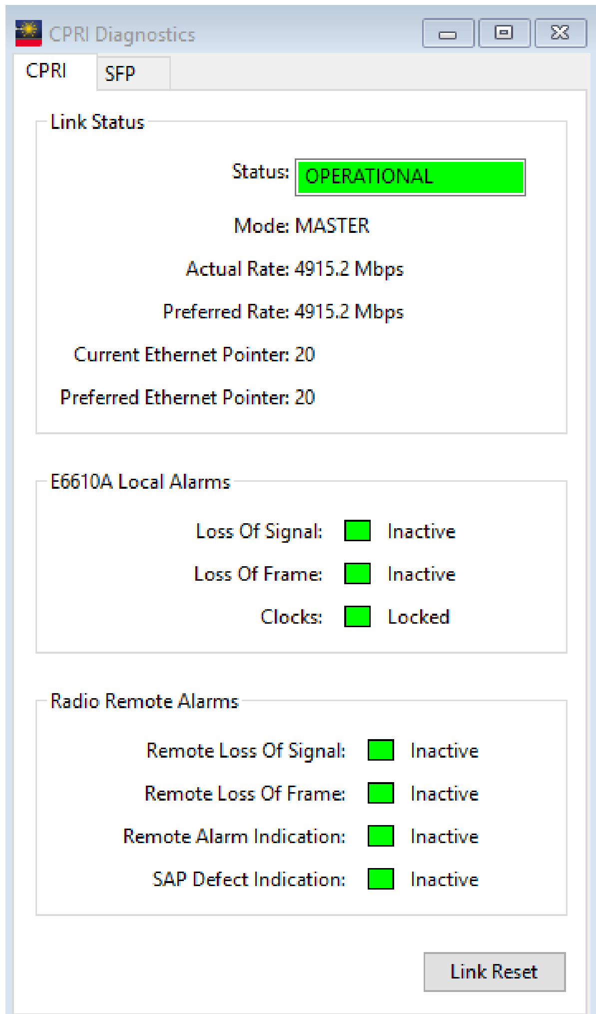
Figure 6-17. Resume Application Execution



The application is executed and LED 4, 5, 6, 7, 8 and 9 on the evaluation board glow. On the MIMO card LEDs, DS6 and DS7 glow. This indicates that the wireless radio DFE design is up and running.

The CPRI diagnostics window shows the link up status as shown in the following figure.

Figure 6-18. CPRI Diagnostics



6.3 Monitoring the Performance (Ask a Question)

After the wireless design is up and running, the RF and baseband plot windows display the data as shown in the following figures.

The plots show the 20 MHz occupied bandwidth data correctly decoded for the 64 QAM constellation on LTE TM3.1.

Figure 6-19. CPRI 1 and 2 Windows

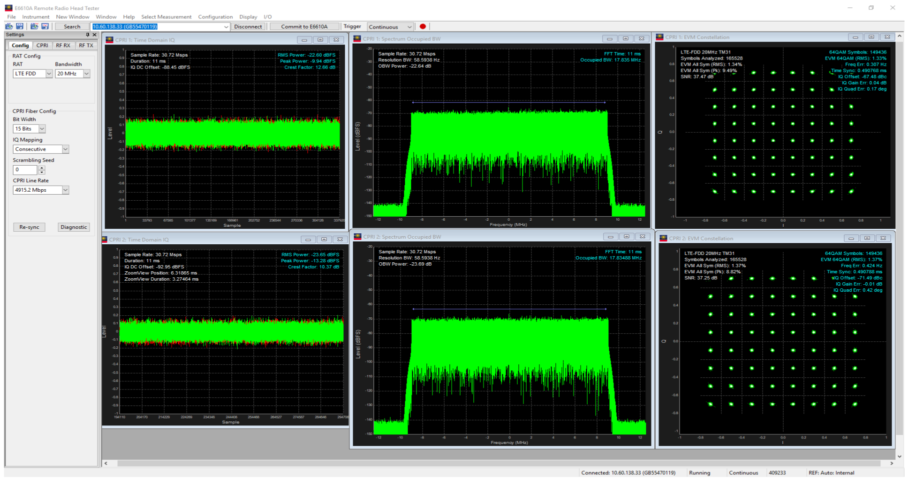
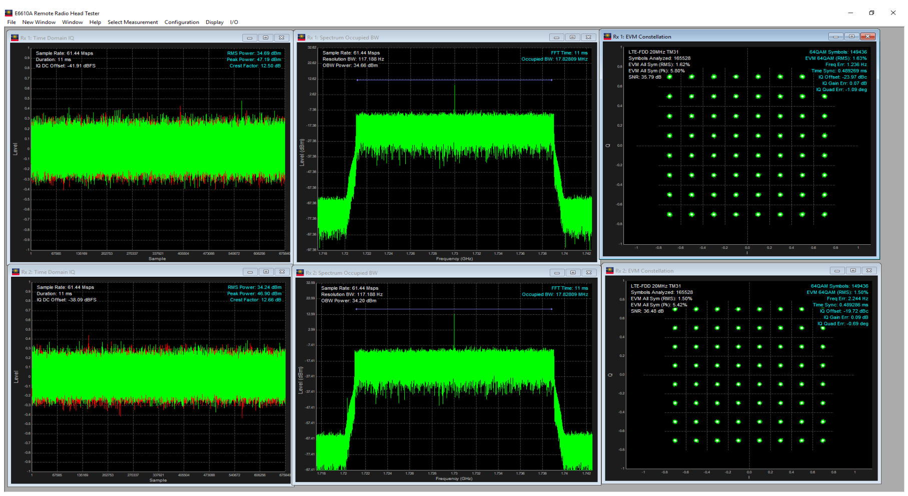


Figure 6-20. RF RX1 and RX2 Windows



7. Power Measurements (Ask a Question)

This section describes how to monitor the real-time power consumption of the wireless radio DFE design using PowerMonitor.

PolarFire Evaluation Board comes with a power monitoring solution implemented using the on-board SmartFusion A2F 200 device and the PowerMonitor application. The PowerMonitor application connects to the power monitoring program running on the A2F 200 device to measure power.

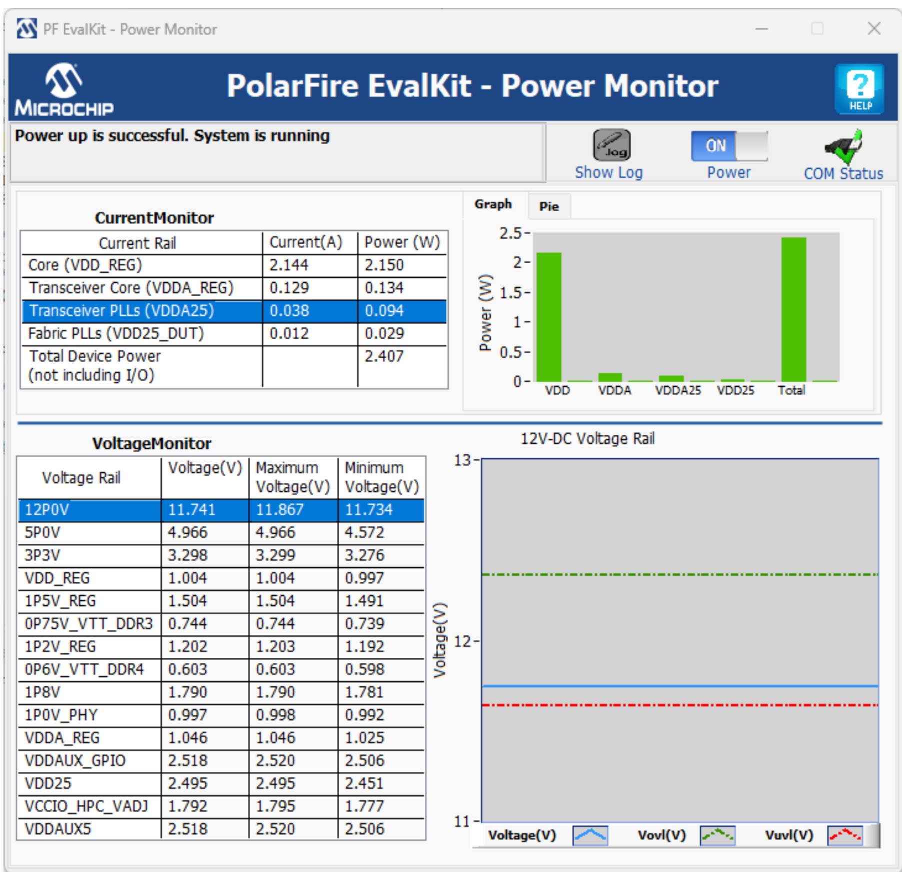
For more information about PowerMonitor, see UG0747: PolarFire FPGA Evaluation Kit User Guide.

Follow these steps:

1. On the host PC desktop, click Start and select **PowerMonitor**.
2. In the **COMPort SetUp** dialog box, select the highest COM port from the drop-down and click **Connect**.

   The PowerMonitor application successfully connects to the board and starts displaying the Core Fabric (VDD) power, Fabric PLL (VDD25) power, Transceiver Core (VDDA) power and Transceiver PLL (VDDA25) power as shown in the following figure.

Figure 7-1. Power Consumption of the DFE Wireless Radio



As shown in the preceding figure, the power consumed by a 2x2 20 MHz MIMO application running on a PolarFire device is only 2.407 W.

7.1 Conclusion (Ask a Question)

This demo shows that PolarFire FPGA designs can be successfully used in wireless communication applications such as small cell and RRH. The demo also demonstrates the low power advantages of using PolarFire FPGAs in such applications.

8. Appendix: Running the TCL Script (Ask a Question)

TCL scripts are provided in the design files folder under directory `HW`. If required, the design flow can be reproduced from Design Implementation till generation of job file.

To run the TCL, perform the following steps:

1. Launch the Libero® software.
2. Select **Project** > **Execute Script.....**
3. Click **Browse** and select `script.tcl` from the downloaded `HW` directory.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within `HW` directory.

For more information about TCL scripts, see `mpf_an5616_df/HW/TCL_Script_readme.txt`. For more information on TCL commands, see Tcl Commands Reference Guide. Contact Microchip Technical Support for any queries encountered, while running the TCL script.

9. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	12/2024	The following is the list of changes in revision A of the document: • The document was migrated to Microchip template. • The document ID was updated to AN5616 from DG0839.
1.0	07/2018	Initial Revision

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