
Robustness on tinyAVR® 0- and 1-series and megaAVR® 0-series

Introduction

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In the *IEEE Standard 610.12-1990 Glossary of Software Engineering Terminology* robustness is defined as “*The degree to which a system or component can function correctly in the presence of invalid inputs or stressful environmental conditions.*” This document is a guide to peripherals available in tinyAVR® 0- and 1-series and megaAVR® 0-series that can be used in robustness applications.

Table of Contents

Introduction.....	1
1. Relevant Devices.....	3
1.1. tinyAVR® 0-series.....	3
1.2. tinyAVR® 1-series.....	3
1.3. megaAVR® 0-series.....	4
2. Power-on Reset.....	5
3. Brown-out Detector.....	6
3.1. Voltage Level Monitor.....	7
4. Watchdog Timer.....	8
5. CRCSCAN.....	9
6. Class B.....	10
7. Configuration Change Protection.....	11
8. Flash Sections.....	12
9. Fuses.....	13
10. Events and Fault Handling.....	14
11. Revision History.....	15
The Microchip Website.....	16
Product Change Notification Service.....	16
Customer Support.....	16
Microchip Devices Code Protection Feature.....	16
Legal Notice.....	16
Trademarks.....	17
Quality Management System.....	17
Worldwide Sales and Service.....	18

1. Relevant Devices

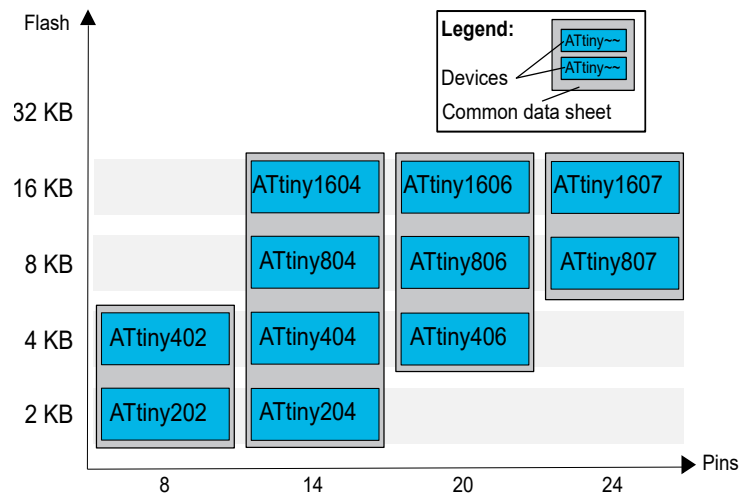
This chapter lists the relevant devices for this document.

1.1 tinyAVR® 0-series

The figure below shows the tinyAVR® 0-series devices, laying out pin count variants and memory sizes:

- Vertical migration upwards is possible without code modification, as these devices are pin-compatible and provide the same or more features
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1-1. tinyAVR® 0-series Overview



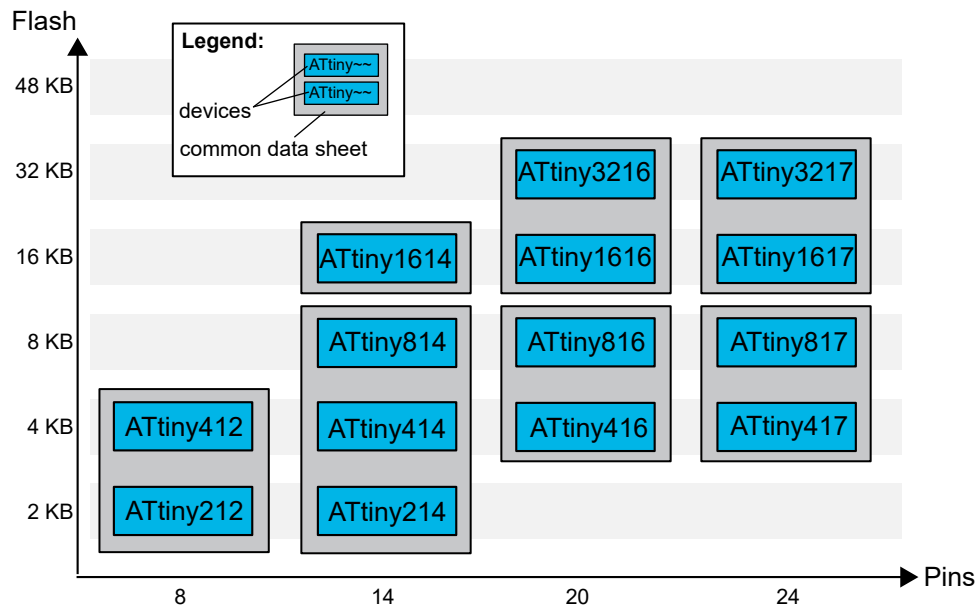
Devices with different Flash memory sizes typically also have different SRAM and EEPROM.

1.2 tinyAVR® 1-series

The following figure shows the tinyAVR 1-series devices, laying out pin count variants and memory sizes:

- Vertical migration upwards is possible without code modification, as these devices are pin-compatible and provide the same or more features. Downward migration may require code modification due to fewer available instances of some peripherals.
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1-2. tinyAVR® 1-series Overview



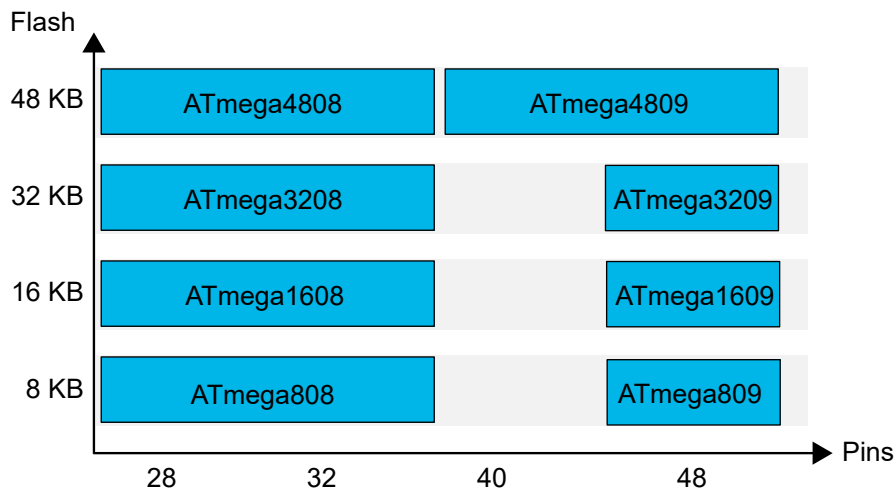
Devices with different Flash memory sizes typically also have different SRAM and EEPROM.

1.3 megaAVR® 0-series

The figure below shows the megaAVR® 0-series devices, laying out pin count variants and memory sizes:

- Vertical migration is possible without code modification, as these devices are fully pin and feature compatible
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1-3. megaAVR® 0-series Overview



Devices with different Flash memory sizes typically also have different SRAM and EEPROM.

2. Power-on Reset

The Power-on Reset (POR) circuit is a non-configurable circuit that ensures the device is reset when powered on, with what is called a Power-on Reset. During POR, all logic is reset, and all registers are initialized, including registers that are loaded from fuses. This procedure ensures that the MCU starts execution in a known good state.

The POR circuit is always active and works by comparing the supply voltage with fixed threshold levels, either rising or falling. These threshold levels are not configurable, unlike the BOD level. See section 3. [Brown-out Detector](#).

Both POR rising threshold level and POR falling threshold level are specified in the electrical characteristics section of the [Relevant Devices](#) data sheet.

When the supply voltage is below the rising threshold, the POR circuit will assert the internal Reset. When the supply voltage rises above the threshold, the device will be allowed to start-up.

In the case of a power dip, the POR circuit compares the supply voltage to a POR falling threshold level. If the supply voltage dips below this threshold, the internal Reset will be reasserted, until the supply voltage again rises above the POR rising threshold level.

If the device is reset by POR, the POR flag in the Reset Flag (RSTCTRL.RSTFR) register is set. After a POR, only the POR flag is set, all other flags are cleared.

3. Brown-out Detector

For the CPU to successfully decode and execute instructions, the supplied voltage must always stay above the minimum voltage level. This level is defined by the chosen operating frequency. For example, an operating frequency of 10 MHz on the [Relevant Devices](#), an operating voltage of minimum 2.7V, must be supplied. If the voltage drops below this threshold, unexpected behavior of the microcontroller (MCU) might occur. This can include incorrect execution of instructions, corruption of CPU registers, Flash corruption, and unexpected toggling of pins. Also, it can cause logic to latch up, possibly entering into incorrect states.

To avoid the above issues, a Brown-out Detector (BOD) can be used. The [Relevant Devices](#) includes an on-board, configurable BOD, which monitors the power supply and compares the voltage with a programmable brown-out threshold level. When the BOD detects that the supply voltage crosses the configured threshold, it will assert the internal Reset. As long as the supply voltage remains below the configured threshold level, the device will be kept in Reset. When the supply voltage is above the threshold level, and normal operation can safely continue, the BOD will deassert the internal Reset, allowing the device to execute instructions.

After a Reset, the BOD settings are loaded from fuses. There are two fuses to control the BOD functionality, which are found in the BOD Configuration (BODCFG) under Fuses in the device data sheet.

The first fuse, ACTIVE, defines the operation mode while in Active or in Idle sleep mode. These bits can not be altered by software.

The second fuse, SLEEP, defines the operation mode while in Standby or Power-down sleep mode. These bits may be altered by software and are under the Configuration Change Protection (CCP).

The ACTIVE and SLEEP fuses can be configured in the following ways:

- *Disabled mode* - BOD is deactivated
- *Enabled mode* - means that BOD is continuously active
- *Sampled mode* - BOD is activated briefly at a given period to check the supply voltage level. Frequency is set to either 125 Hz or 1 kHz in Sample Frequency (BODCFG.SAMPFREQ) fuse

Also, ACTIVE has a fourth option:

- *Enabled with wake-up halted until BOD is ready* - BOD is not active during sleep. On wake-up, the code execution is halted until BOD is ready. This ensures the correct supply voltage whenever the code is executed. The wake-up time may be extended.

Sample Frequency (SAMPLEFREQ) and BOD Level (LVL) are also found in BODCFG. These control how the BOD behaves.

BOD Levels

The BOD compares the supply voltage to a threshold level. This threshold is programmable, and the user can select from 8 different levels. [Table 3-1](#) shows the BOD levels from the ATtiny3217 data sheet. Always check the [Relevant Devices](#) data sheet for correct BOD levels.

Table 3-1. BOD Threshold Level Examples

Name	Description
BODLEVEL0	1.80V
BODLEVEL2	2.60V
BODLEVEL7	4.30V

When setting the BOD level, several things come into consideration. As already mentioned, the BOD can protect the system from an unsafe operation. Also, the BOD can be used to ensure voltage levels, e.g., when using the ADC. If the ADC is set to sample using the 4.3V internal reference, and the supply voltage drops below this level, the ADC results will be incorrect.

If the BOD is unused, it will be set to the minimum level to ensure safe operation during an internal Reset and chip erase.

3.1 Voltage Level Monitor

The Voltage Level Monitor (VLM) acts as an early warning and generates an interrupt request if the supply voltage is about to drop below a given threshold level. This can allow the system to do a safe shutdown.

Being a part of the [BOD peripheral](#), the VLM threshold level can be configured to either 5%, 15% or 25% above the BOD level. The VLM follows BOD functionality. If the BOD is in Sampled mode, the VLM will also be sampled. If the BOD is disabled, the VLM is disabled.

The VLM interrupt can be triggered when the supply voltage crosses from above, from below, or either direction of the threshold level.

4. Watchdog Timer

Many issues can cause a system to enter an illegal or frozen state, e.g., software bugs or electrical noise. One safety measure available on the [Relevant Devices](#) is the Watchdog Timer (WDT). This is a timer that runs independently from the rest of the system, with a separate clock source. When the timer overflows, it will cause a Reset. The system firmware must periodically clear the WDT using the dedicated instruction Watchdog Timer Reset (`WDR`). If the firmware is not able to do so, e.g., due to a system hang or run-away code, the system will be Reset.

Normal mode

In Normal mode, the watchdog counts from 0 to the MAX value and can be cleared at any time. The period in Normal mode can be configured with a duration from 8 ms to 8s.

Window mode

For increased robustness, Window mode is available. In Window mode, both a closed and an open window are configured, with the closed window being at the start of the period. While in the closed window, clearing the WDT is an illegal operation, resulting in a Reset. Once the closed window is over, the open window starts and the WDT can now be cleared. Using Window mode puts more requirements on the firmware, as it must clear the watchdog in the open window only. Both windows can be configured with a duration of 8 ms to 8s. This gives a total WDT period of 16 ms to 16s.

The WDT period and window timeouts can be configured by fuses so that it is active immediately after Reset. Should there be any issue with the firmware, causing it to not start properly, the WDT will reset the system. The WDT will start to count from 0 after Reset, regardless of the Reset source.

As one of the goals of implementing a watchdog timer is to be able to recover from the run-away code, there are a few things the software engineer may consider. The run-away code does not influence the execution of an interrupt. Any interrupt vector will be correctly loaded, even when the system for some reason is executing the wrong code. Therefore, do not clear the WDT from an interrupt handler. Also, try to limit the amount of `WDR` instructions. If clearing the WDT is done in many parts of the firmware, it becomes more likely that one of these is executed when the run-away code is being executed. Ideally, only one `WDR` instruction may be implemented. This can be hard to achieve, but it is important to try to limit the amount of `WDR` instructions. Using the Window mode can also help catch erroneously executed `WDR` instructions.

5. CRCSCAN

A Cyclic Redundancy Check (CRC) creates a checksum for a block of data, enabling error detection of the data block. The [Relevant Devices](#) feature the CRCSCAN peripheral, which can check a [Flash section](#) and compare it to a checksum stored at the end of the section. If the Flash section is accidentally changed, i.e., because of corruption or an unintended write, the CRCSCAN will detect this and signal to the CPU that Flash has been corrupted.

In a bootloader application, CRCSCAN can be used to verify the application image before starting execution. This to make sure that corrupted software is not executed, which could have catastrophic consequences. If the check fails, the bootloader can either choose not to start the application, it can do a firmware update, or it can signal the error to an external system.

CRCSCAN can be run at start-up, or specific intervals controlled by the application. When running at start-up, the Flash is checked for errors before any instruction is executed. This allows the integrity of the application to be verified before execution. CRCSCAN on start-up is configured using fuses.

When CRCSCAN is controlled by the application, it can be started by register access. When started, the CPU is halted while the check is being done, as CRCSCAN has priority access to Flash, thus blocking the CPU.

For more information, refer to the [CRCSCAN on *tinyAVR*® 0- and 1-series and *megaAVR*® 0-series](#) application note.

6. Class B

Modern appliances are mostly electronically controlled. Electronic controls enable higher efficiencies, additional functionality, and improved user experience. But what happens if something goes wrong? IEC 60730 addresses the safety of electronic controls in appliances. This standard is also referred to by other standards for safety-critical devices, for example, IEC 60335. Currently, IEC 60730 is mandatory for appliances sold in Europe.

IEC 60730 Annex H defines three classes of control software for appliances:

- Class A - control functions that are not intended to be relied upon for the safety of the equipment
- Class B - software that includes code intended to prevent hazards if a fault, other than a software fault, occurs in the appliance
- Class C - software that includes code intended to prevent hazards without the use of other protective devices

For an appliance to comply with the Class B requirements, the control software must detect and handle faults for system components. For a customer wishing to certify a product following Class B requirements, Microchip offers a Class B library for tinyAVR® 1-series. This library implements the tests needed to comply with Class B and can reduce development time and certification cost.

Tests are done on CPU registers, program counter, frequency, CRC, interrupt handling and execution, clock, SRAM, Flash, EEPROM, and peripherals such as ADC, DAC, and WDT.

For more information, refer to [Guide to IEC 60730 Class B Compliance with tinyAVR® 1-series](#).

7. Configuration Change Protection

System critical registers are protected from accidental modification, and Flash self-programming is protected from accidental execution. This is handled globally by the Configuration Change Protection (CPU.CCP) register. Execution of either of these actions is only possible after a signature has been written to the CCP register. After writing the correct signature to the CCP register, the desired action must be executed within four instructions. Interrupts are kept pending during these four cycles.

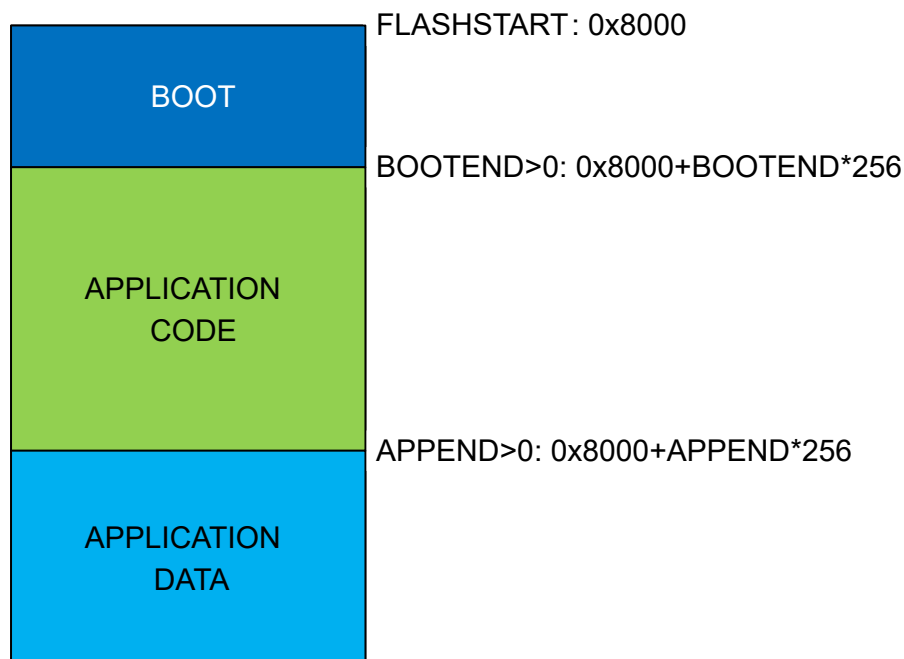
Refer to the CPU section in the [Relevant Devices](#) data sheet for details on CCP.

8. Flash Sections

Flash of the [Relevant Devices](#) can be split into three separate sections: BOOT, application code (APPCODE) and application data (APPDATA). This scheme allows for the protection and safe storage of several individual segments of code or data. The granularity of the division is 256 bytes.

The size of the three sections is set using the fuses Boot Section End (BOOTEND) and Application Code Section End (APPEND). BOOTEND determines the size of the BOOT. APPEND determines the size of the APPCODE. APPCODE will be placed immediately after the BOOT. The remaining pages will be part of APPDATA, placed immediately after APPCODE. If both fuses are set to zero, all pages are allocated to the BOOT. This is the normal procedure if only an application is written to Flash, with no bootloader.

Figure 8-1. Flash Sections



If FUSE.BOOTEND is written to 0x04 and FUSE.APPEND is written to 0x08, the first 4*256 bytes will be BOOT, the next 4*256 bytes will be APPCODE, and the remaining Flash will be APPDATA.

To protect the data in the three sections, directional write protection is implemented:

- Code in the BOOT section can write to APPCODE and APPDATA
- Code in APPCODE can write to APPDATA
- Code in APPDATA cannot write to Flash or EEPROM

In addition to the directional write protection, two register bits can be used to increase restrictions.

By writing a 1 to the Application Code Section Write Protection (APCWP) bit, the application code section is protected from further writes. The bit can be found in the Control B (CTRLB) register of the Nonvolatile Memory Controller (NVMCTRL) peripheral. This bit is cleared on Reset.

As the BOOT section can never be written by the CPU, there is no need to protect BOOT from writes in the same manner. But by writing a 1 to the Boot Section Lock (BOOTLOCK) bit in CTRLB register of the NVMCTRL peripheral, reading and executing code from BOOT can be prevented. This bit is cleared on Reset.

Refer to the Nonvolatile Memory Controller (NVMCTRL) chapter in the [Relevant Devices](#) data sheet for more details.

9. Fuses

Fuses are part of the nonvolatile memory and are used to configure system settings such as clock source, start-up time, Flash sections, etc. Fuses can be read by both the CPU and an external programmer, but only programmed or cleared by an external programmer. Some registers are reset to a value stored in the fuses, such as oscillator calibration. These values are written at the end of the start-up sequence. Thus, when such a fuse is changed, the device must be reset before the change takes effect.

Fuses for peripheral configuration include:

- **Watchdog Timer**: Used to set the WDT window and timeout period upon start-up, thus not requiring any code execution to operate.
- **Brown-out Detector**: Used to set the BOD level, sample frequency, Active and Standby operating mode, thus not requiring any code execution to operate.
- **16/20 MHz Oscillator**: Configures whether the operating frequency should be 16 or 20 MHz. It is also possible to lock the calibration registers after they are loaded with factory calibration values.
- **Timer/Counter D**: Used to enable or disable TCD output pins, and also to set the default state of the pins. This fuse is only available for devices in the tinyAVR® 1-series.
- **System Configuration 0**: Used to configure the CRCSCAN to run on start-up, and to select which Flash section to check.
- **System Configuration 1**: Used to configure additional start-up time of the device.
- **Application Code End**: Used to configure the size of the application code section.
- **Boot End**: Used to configure the size of the boot section.
- **Lockbits**: Used to lock the device and prevent an external programmer from accessing the fuses, Flash, SRAM and EEPROM. Regular memory access from within the application still is enabled. A chip erase must be executed to unlock a device.

Using fuses to set up, e.g., a WDT before any code is executed increases the robustness of the system. This because corrupt Flash could cause a software-driven configuration of the WDT to fail. Imagine that the instruction enabling the WDT is corrupt and is not properly executed. The result is a system that misbehaves, and the mechanisms to detect erroneous behavior is disabled. Therefore, enabling security features using fuses is an advantage.

Enabling **CRCSCAN** using fuses allows the Flash to be scanned for errors before any instruction has been fetched from Flash.

For more information, refer to the Fuses sub-section in the Memories chapter in the [Relevant Devices](#) data sheet.

10. Events and Fault Handling

This section is relevant only for devices in the tinyAVR® 1-series. The Timer/Counter type D (TCD) is a timer/counter specifically designed for controlling power applications like driving LEDs, motor control, H-Bridge and power converters. An important safety feature of TCD is the built-in fault handler. The fault handler allows the output of TCD to be clamped to predefined levels upon a fault. The fault is an incoming event, and some other internal or external peripheral must be present to discover the condition.

Imagine the TCD driving an motor for a fan. The Analog Comparator (AC) is also connected to the fan and monitors the current consumption. If the current consumption rises above a predefined threshold, e.g., due to something being stuck in the fan, the AC sends an event to the TCD. Upon receiving the event, TCD immediately clamps all outputs to a predefined level, and the motor stops. This way, the motor is stopped safely before overheating or destroying the object that caused the blockage.

When using an external circuit instead of an internal peripheral, the event is generated by an edge or change in the level of the pin connected to the external circuit. Again, this event is sent to the TCD, which immediately clamps all output to a predefined state.

The event is sent via the Event System (EVSYS). The EVSYS enables direct peripheral to peripheral signaling. One peripheral (Event Generator) can signal to one or several other peripherals (Event Users), without using the CPU.

All parts of the described examples are core independent (CIP), meaning that even if the CPU is deadlocked, this safety feature will work like intended.

11. Revision History

Doc. Rev.	Date	Comments
C	11/2019	Changed title to reflect that the application note is also relevant for tinyAVR® 0-series and megaAVR® 0-series. Removed unsupported BOD levels in Table 3-1 . Clarified tinyAVR® 1-series specific features in the Class B, Fuses and Events and Fault Handling section.
B	10/2018	The chapter on relevant devices has been updated to include 8/16 KB megaAVR 0-series devices.
A	06/2018	Initial document release

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