APPLICATION NOTE

Discrete Power Supply Solution for Atmel eMPUs

Atmel | SMART SAMA5D3 - SAM9G15/25/35/45/46 SAM9M10/11 - SAM9N12 - SAM9CN11/12 - SAM9X25/35 Series

Scope

A wide variety of applications based on Atmel® | SMART SAMA5D3x and several SAM9x [1] series embedded MPUs (eMPU) can be powered from a low-cost power supply solution based on discrete components.

This application note provides developers with a recommended application schematic with associated functional descriptions.

Reference Documents

Type	Title	Atmel Lit. No.
Datasheet	SAM9G15 Datasheet	11152
Datasheet	SAM9G25 Datasheet	11032
Datasheet	SAM9G35 Datasheet	11053
Datasheet	SAM9G45 Datasheet	6438
Datasheet	SAM9G46 Datasheet	11028
Datasheet	SAM9M10 Datasheet	6355
Datasheet	SAM9M11 Datasheet	6437
Datasheet	SAM9N12/SAM9CN11/SAM9CN12 Datasheet	11063
Datasheet	SAM9X25 Datasheet	11054
Datasheet	SAM9X35 Datasheet	11055
Datasheet	SAMA5D3 Series Datasheet	11121

1. In this application note, “SAM9x” represents exclusively the Atmel eMPUs SAM9G15, SAM9G25, SAM9G35, SAM9G45, SAM9G46, SAM9M10, SAM9M11, SAM9N12, SAM9CN11, SAM9CN12, SAM9X25, and SAM9X35.

Table of Contents

1. Power Supply Overview of Atmel eMPU Systems

1.1 Atmel eMPU Power Rails

Atmel eMPUs of both the SAMA5D3x and SAM9x [1] series have multiple supply rails corresponding to the operating voltages of their internal circuits (e.g., CORE logic = 1.2V or 1.0V) and to the operating voltages of the external components connected to them (e.g., DDR2 power supply = 1.8V).

These rails and their respective operating ranges are listed in Table 1-1. An approximate current consumption is provided for each rail in order to size the corresponding regulator. Accurate numbers and descriptions are provided in the device datasheet.

In most non-secure applications, the eMPU subsystem (device + external memories) can be operated from three primary rails:

- 3.3V, 1.8V and 1.2V (SAMA5D3x)
- 3.3V, 1.8V and 1.0V (SAM9x)

In secure applications of the SAMA5D3x device, or any application that requires writing into the fuse box of SAMA5D3x, an additional power rail at 2.5V is needed to supply the VDDFUSE input pin.

Additionally, Atmel eMPUs have a specific VDDBU pin to power their backup domain (e.g., 32 kHz crystal oscillator, RTC, System Controller). When needed, and because of its ultra-low power consumption, this power domain can be maintained during powerdown periods with a storage element such as a 3.0V lithium coin cell battery or a super-capacitor. Otherwise, applications can operate VDDBU on the main 3.3V power rail.

Table 1-1. SAMA5D3x and SAM9x Series Power Supply Inputs

Power Rail	Description	SAMA5D3x		SAM9x	
		Range	Consumption	Range	Consumption
VDDCORE	Core Logic	1.10–1.32V, 1.20V	0.2A	0.90–1.10V, 1.00V	0.2A
VDDUTMIC	USB Device and host UTMI+ core logic	1.10–1.32V, 1.20V	0.02A	0.90–1.10V, 1.00V	0.02A
VDDPLLUTMI	UTMI PLL on SAM9	–	–	0.90–1.10V, 1.00V	0.02A
VDDPLLA	PLLA cell	1.10–1.32V, 1.20V	0.02A	0.90–1.10V, 1.00V	0.02A
VDDIODDR	External Memory Interface I/O lines	1.70–1.90V, 1.80V 1.14–1.32V, 1.20V	0.05A 0.03A	–	–
VDDIOM0		–	–	1.70–1.90V, 1.80V	0.05A
VDDIOM or VDDIOM1/VDDNF	NAND and HSMC Interface I/O lines	1.65–1.95V, 1.80V 3.00–3.60V, 3.30V	0.03A	1.65–1.95V, 1.80V 3.00–3.60V, 3.30V	0.03A
VDDIOP0	Peripheral I/O lines	1.65–3.60V	0.03A	1.65–3.60V	0.03A
VDDIOP1	Peripheral I/O lines	1.65–3.60V	0.03A	1.65–3.60V	0.03A
VDDIOP2	Peripheral I/O lines	–	–	1.65–3.60V	0.03A
VDDUTMII	USB Device and host UTMI+ interface	3.00–3.60V, 3.30V	0.02A	3.00–3.60V, 3.30V	0.02A

1. In this application note, “SAM9x” represents exclusively the Atmel eMPUs SAM9G15, SAM9G25, SAM9G35, SAM9G45, SAM9G46, SAM9M10, SAM9M11, SAM9N12, SAM9CN11, SAM9CN12, SAM9X25, and SAM9X35.

Table 1-1. SAMA5D3x and SAM9x Series Power Supply Inputs (Continued)

Power Rail	Description	SAMA5D3x		SAM9x	
		Range	Consumption	Range	Consumption
VDDOSC	Main oscillator UTMI PLL on SAMA5	1.65–3.60V, 3.30V 3.00–3.60V, 3.30V	0.001A	1.65–3.60V, 3.30V	0.001
VDDANA	Analog-to-Digital Converter	2.40–3.60V, 3.30V	0.01A	3.00–3.60V, 3.30V	0.01A
VDDFUSE	Programmable Fuse Box	2.25–2.75V, 2.50V	0.05A	–	–
VDDBU	Backup domain	1.65–3.60V	0.0001A	1.80–3.60V	0.0001A

In all modes other than Backup mode, each power supply input must be powered to operate the device. The only exception is the VDDFUSE input which can be left unpowered if the fuse box of SAMA5D3x is not used in Write mode.

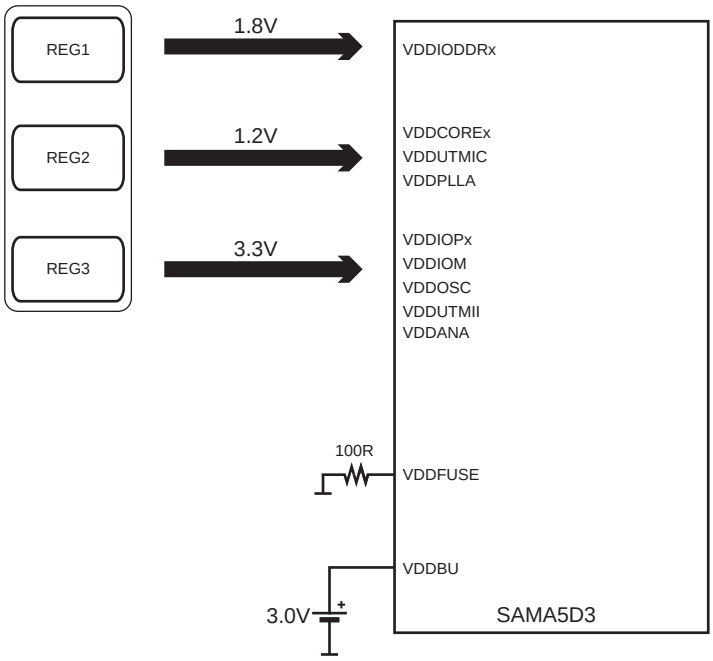
1.2 Power Supply Topologies and Power Distribution

The lowest cost power supply of systems based on Atmel eMPUs is achieved by implementing, a 3-rail power supply topology (3.3V / 1.8V / 1.2V or 1.0V) as shown in Figure 1-1. However, this topology has the following limitations:

- The fuse box cannot be accessed in Write mode because VDDFUSE = 0V.
- The analog section of the device (VDDANA) is powered from the digital 3.3V rail that may be too noisy in some applications.

These limitations can be overcome by adding one or two regulators for VDDANA and VDDFUSE. Note that both VDDANA and VDDFUSE supply is possible at 2.5V from the same regulator output. In this case, the regulators must be enabled and disabled along with the main 3.3V regulator.

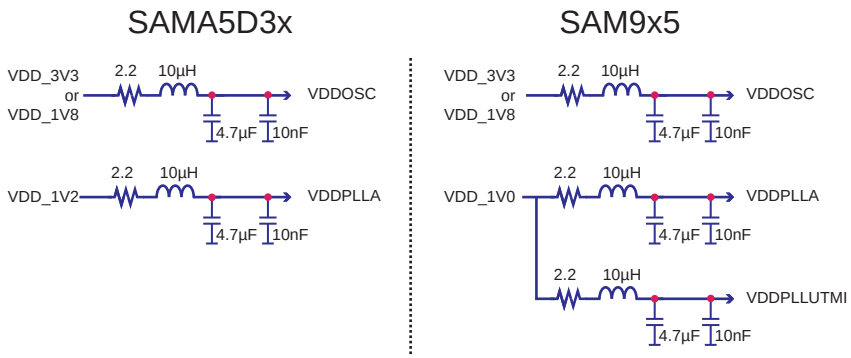
Figure 1-1. 3-channel Power Distribution Example on SAMA5D3x Series Equipped with an 1.8V External Memory



1.3 Clock Circuits Power Supply

Atmel eMPUs have separate power supply inputs for their oscillators and PLL circuits. This allows to decouple these analog circuits from the digital (core and I/Os) activity of the device and thus generate less jittered clocks. Atmel highly recommends feeding these power supply inputs with low noise sources for applications where clock jitter is important (e.g., high-speed USB). The simplest way to do this is to filter the digital rails with an LC network as shown in Figure 1-2. Choosing a 20 kHz corner frequency is a good trade-off between component size/cost and the necessary high-frequency attenuation for clock circuits. The inductors must be sized for low DC resistance and good DC superimposition characteristics (TDK MLZ series and Taiyo Yuden CBM series are possible choices). The serial resistor in the filter schematic must be adjusted to take the inductor DCR into account. Example of inductors: Taiyo Yuden CBMF1608T100K (10 µH, 0.36 Ω, 115 mA, 0603) and TDK MLZ1608N100L (10 µH, 0.6 Ω, 60 mA, 0603).

Figure 1-2. Recommended Filter on Clock Circuits Power Supply



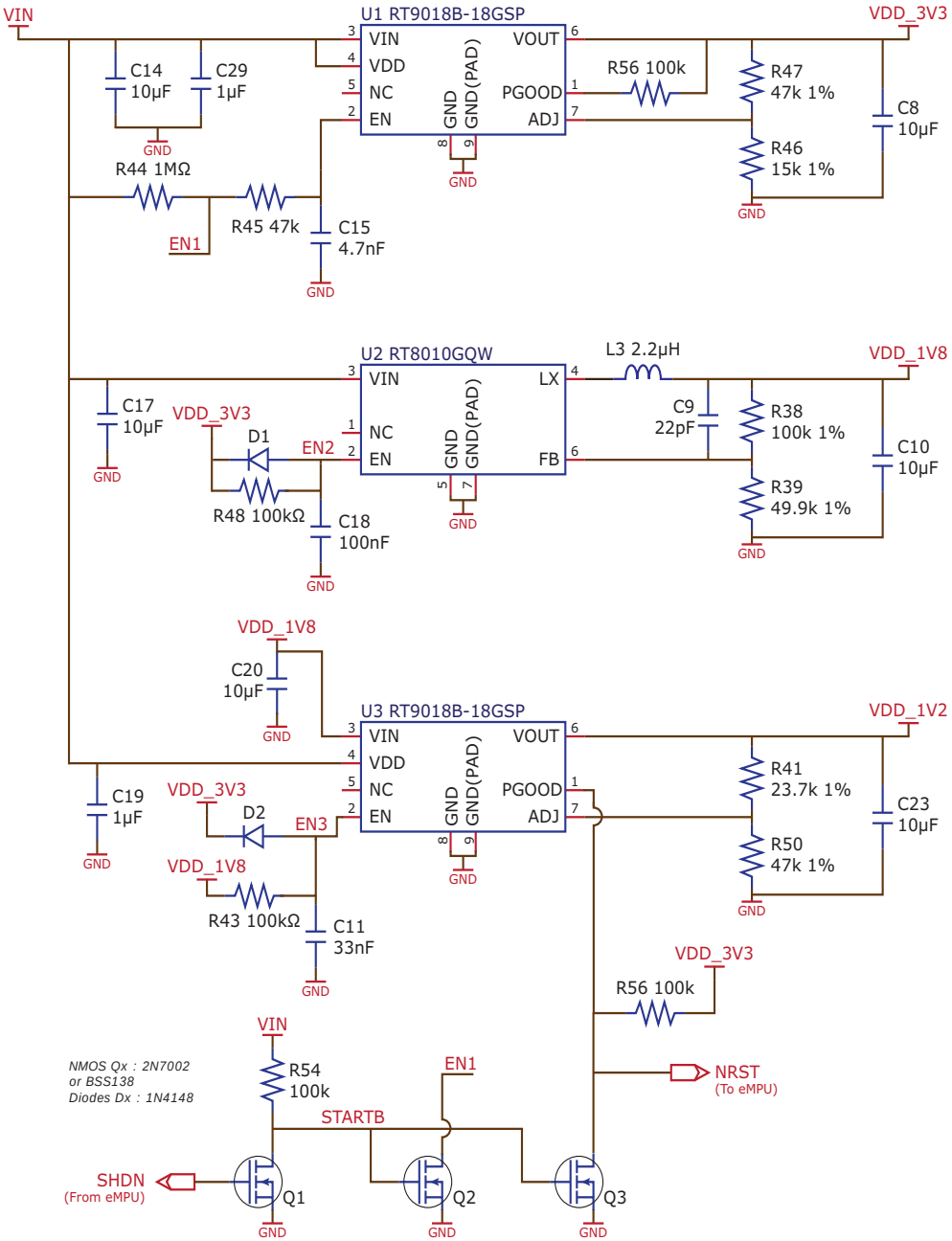
1.4 Power Supplies Monitoring

Atmel eMPU power rails are not internally monitored. In low-cost systems, when the input power can be removed without advising the application, it is recommended to monitor the input voltage to detect the input power loss. In this case of power-fail, the application should start a power-off sequence. This is particularly relevant in SAMA5D3 systems equipped with LPDDR2 memories for which uncontrolled power-off conditions may lead to damage to the memory IC.

2. Reference Schematic and Description

2.1 Basic Reference Schematic

Figure 2-1. Basic Reference Schematic



In this schematic, the power input VIN ranges from 3.5V to 5.5V. The lower limit (3.5V) is set by the need to generate a 3.3V voltage (VDD_3V3) to feed some of the eMPU rails. In some applications, VIN may run at a lower voltage (e.g., 3.0V) if the maximum voltage applied to the eMPU power inputs is also limited (e.g., 2.8V, 2.5V or 1.8V).

VIN feeds a low dropout regulator (U1) to make the VDD_3V3 voltage and a DCDC buck regulator (U2) to make the VDD_1V8 voltage. The core voltage VDD_1V2 is built from the VDD_1V8 rail by the low input voltage low

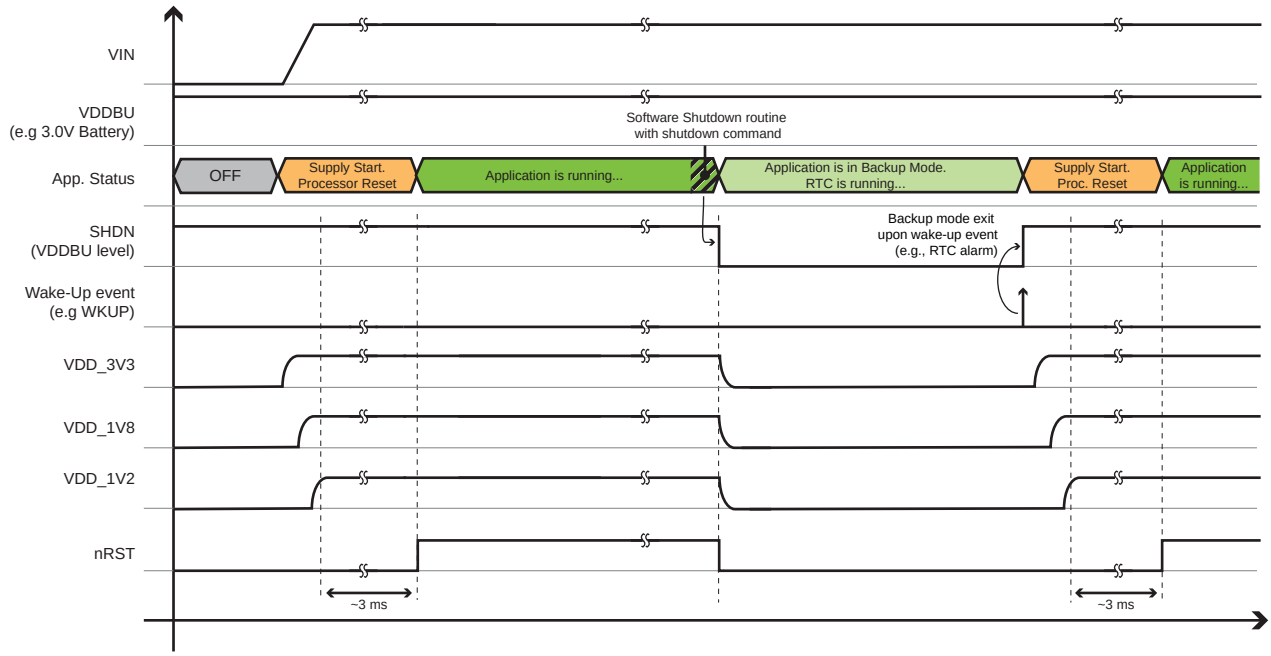
dropout regulator (U3). Note that R41 must be changed to 11.8k 1% to generate a 1.0V voltage (SAM9x) instead of 1.2V.

The topology with only one DCDC regulator is intended for low-cost systems where LDO regulators offer some cost advantages over DCDC regulators. However, the principles described in this application note about the regulators' control are still applicable if the user replaces one or two LDO regulators by one or two DCDCs regulators.

Low-cost discretes are used to control the regulators' enable pins (EN) and the NRST signal of the eMPU. As demonstrated in the following, this schematic ensures proper supply sequencing and reset assertion during power-up and power-down phases.

This power supply is designed to be controlled by the eMPU Shutdown Controller (SHDWC) and its SHDN pin. Refer to the section "Shutdown Controller (SHDWC)" in the device datasheet for a complete description. In summary, SHDN is high when the eMPU is running, whereas SHDN is low when the eMPU goes to Backup mode or to OFF mode. The SHDN pin defaults to '1' (VDDBU level) when VDDBU is first applied. Figure 2-2 shows a typical application timing diagram and the use of the Shutdown Controller.

Figure 2-2. Typical Application Timing Diagram

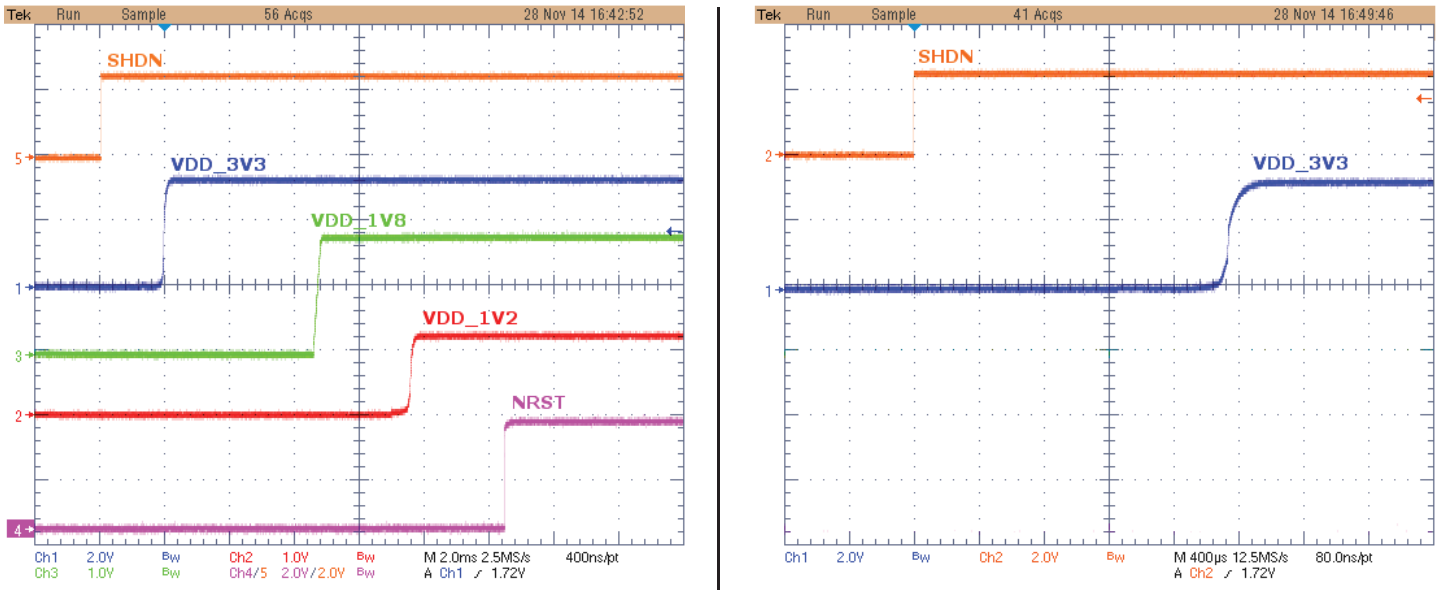


2.2 Wake-Up and Shutdown Description

2.2.1 Wake-Up Description

Figure 2-3 shows the typical wake-up waveforms of the basic reference schematic power supply. In the left-hand image, upon a wake-up event (not shown here), the processor pulls the SHDN pin high (VDDBU level, here 2.5V) and exits the Backup mode. SHDN is applied through Q1 and Q2 to the enable pin of U1. The delay between SHDN and the start of regulator U1 is tuned with the (R44 + R45) / C15 network (here about 2ms, shown in the right-hand image). U1 starts regulating the VDD_3V3 output to 3.3V which enables the U2 regulator through the R48 / C18 delay network (here about 5ms). When U2 starts regulating VDD_1V8 at 1.8V, it enables the regulator U3 through the R43 / C11 delay network (here about 3ms). During this start-up phase, the processor is held in reset with its NRST pin driven by the PGOOD (power-good) output of U3. U3 releases this output about 3ms after VDD_1V2 has reached 90% of its final value.

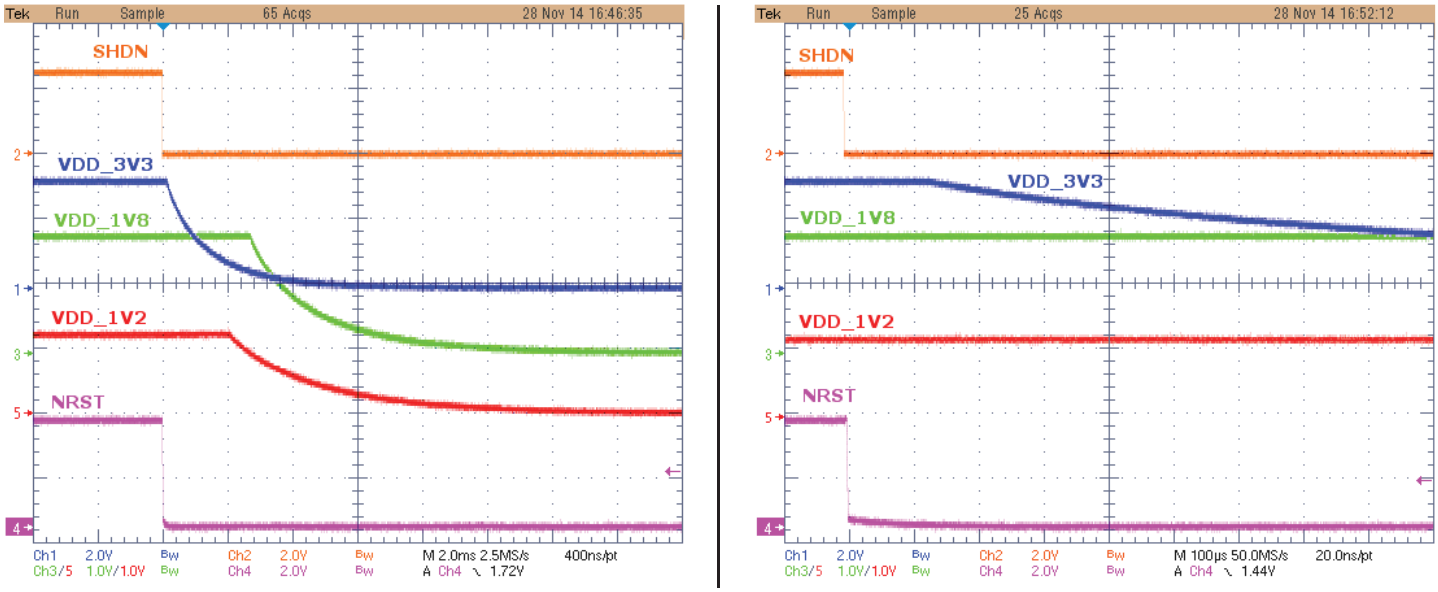
Figure 2-3. Wake-up Waveforms



2.2.2 Shutdown Description

Figure 2-4 shows the typical shutdown waveforms of the reference schematic power supply. In the left-hand image, upon a shutdown request in the Shutdown Control register (SHDW_CR), the processor pulls the SHDN pin low and enters Backup mode. NRST is almost immediately pulled low through Q1, Q2 and Q3. The delay between the SHDN falling edge and the NRST signal assertion is less than 10 µs and depends on the R54-C_{STARTB} delay. C_{STARTB} is a sum of parasitic capacitances at node STARTB (Q1's drain capacitance, Q2 and Q3's gates capacitances). After the R45 / C15 delay (about 100µs as depicted in the right-hand image), the enable pin of U1 falls. U1 stops and discharges its output capacitor through its internal discharge resistor. When VDD_3V3 falls, it discharges C18 and C11 through D1 and D2. The enable pins of U2 and U3 are pulled low, thus stopping these regulators.

Figure 2-4. Shutdown Waveforms

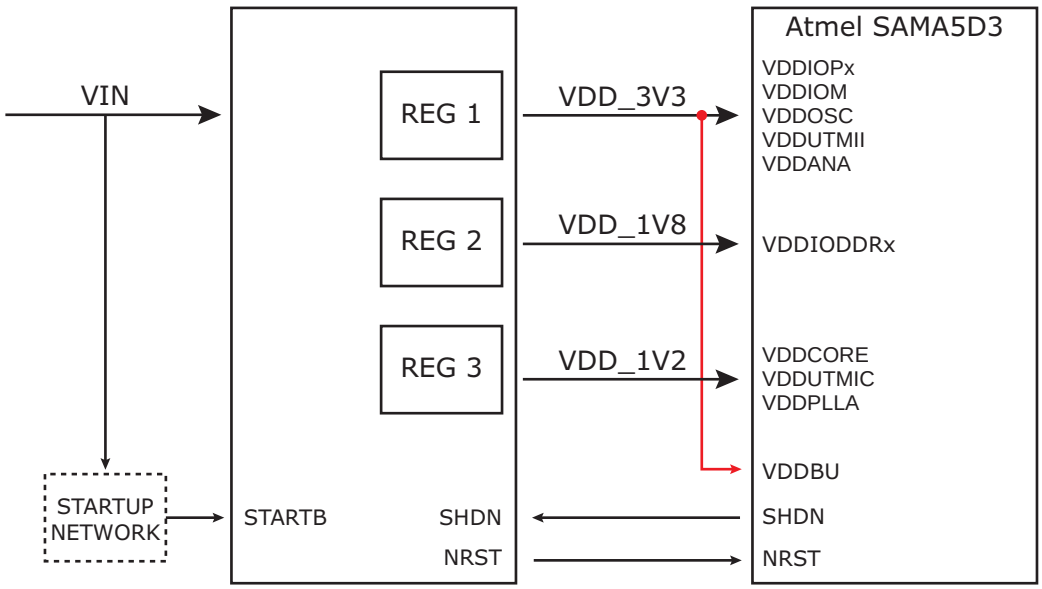


3. Variations from the Reference Schematic

3.1 Applications Without Backup Battery

When no backup functionality is required in an application, VDDBU can be fed by one regulator output instead of a storage element (e.g., a battery), as shown in Figure 3-1. In this case, VDDBU is 0V before the power supply starts and SHDN, powered from the VDDBU rail, is also 0V. For this reason, the power supply of the reference schematic must be modified to start even when VDDBU = 0V. This is the purpose of the start-up network box of Figure 3-1.

Figure 3-1. Applications Without Storage Element on VDDBU



Each application has specific start-up event needs. Some examples of start-up events are:

- a start at VIN rise
- a mechanical action, e.g., a push-button
- internal signals to trigger a power supply start

From a generic usage perspective, it is wise to note that forcing low the STARTB node (refer to Figure 2-1) for a minimum of 5ms is enough to start the power supply. Indeed, when STARTB is set to 0V, the U1 regulator starts after about 2ms. As VDDBU is powered from VDD_3V3, VDDBU gets powered and the SHDN pin defaults to '1' (VDD_3V3 in this case). Q1 now forces STARTB to 0V and the power supply does not need any further external intervention to keep working. A few examples of start-up networks are given in the following section.

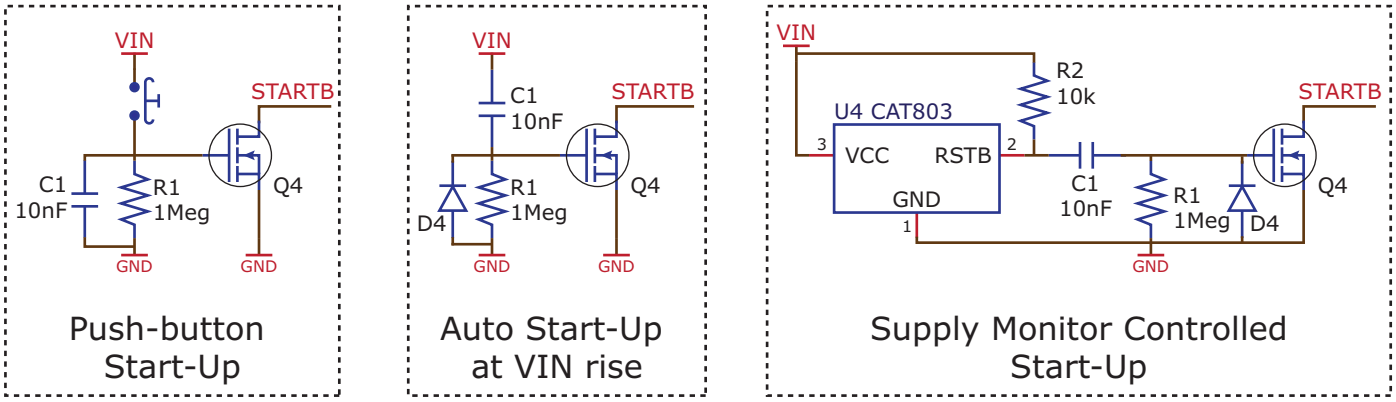
3.2 Start-up Circuit Examples

Figure 3-2 shows three examples of start-up circuits.

- In the first example, a push button start-up is implemented. As soon the button is pressed, STARTB is pulled low, thus enabling the power supply to start.
- The second circuit is designed to start the power supply when VIN rises. The C1 / R1 network keeps Q4 in its ON state for about 10ms. The disadvantage of this circuit is that it is not protected against out-of range VIN, i.e., it starts the power supply even with lower than acceptable VIN. For applications where VIN has a minimum guaranteed value, this circuit is suitable.
- The third start-up circuit is based on a supply monitor, thus ensuring safe VIN conditions to start the power supply. When VIN is above its internal threshold, the supply monitor releases its RSTB output after a

specified delay (about 140ms for CAT803 devices). Through C1, this transition is transmitted to Q4 which pulls STARTB low for about 10ms and thus enables the power supply start-up.

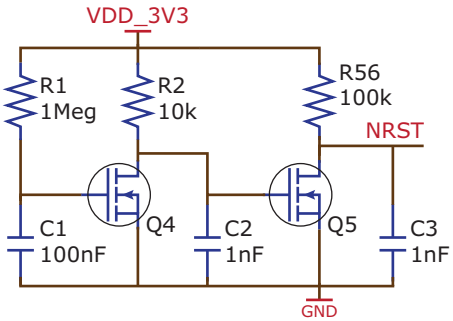
Figure 3-2. Examples of Start-up Networks



3.3 NRST Signal Generation at Power-Up

In Figure 2-1, at power-up, the NRST signal is held low using the PGOOD (power-good) output of regulator U3. In the case where the application does not use a regulator with a power-good output, it is possible to generate the NRST signal based on a delay circuit. An example is shown in Figure 3-3. This type of circuit is not as effective as the one based on a voltage comparison with a voltage reference; however, it brings a low-cost solution that may be acceptable in many systems. The delay between the rise of VDD_3V3 and the release of NRST is adjusted with R1/C1. With the component values shown in Figure 3-3, this delay between NRST and VDD_3V3 is 25ms in typical conditions.

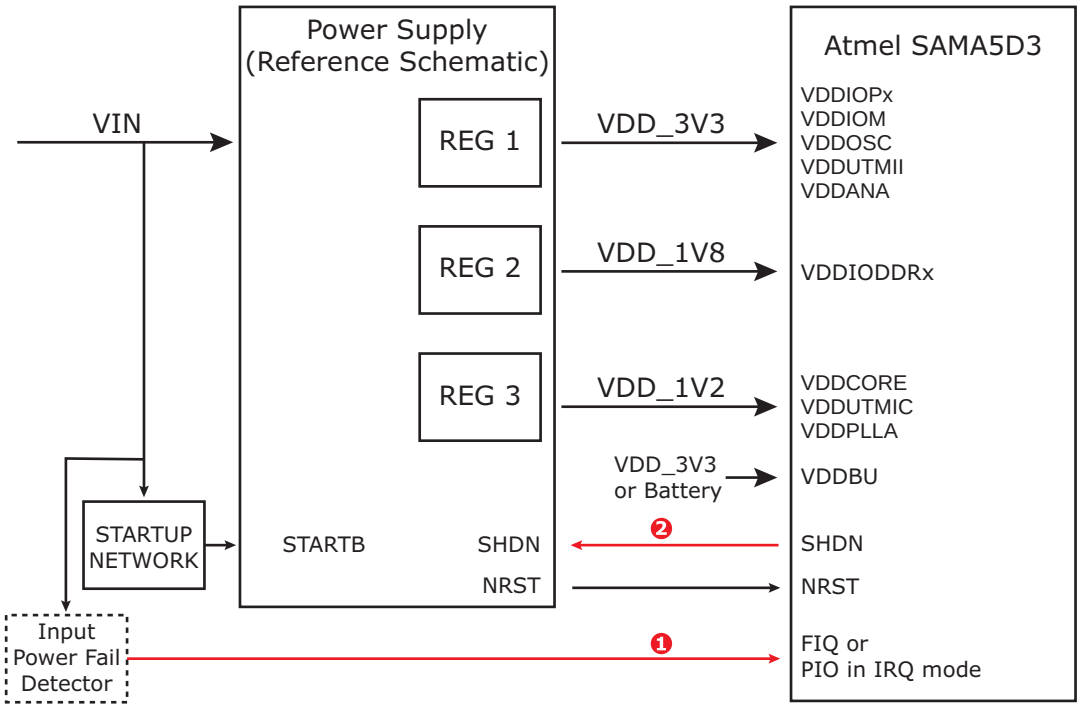
Figure 3-3. Delay-Based Reset Generation Circuit



3.4 Input Power-Fail Detection

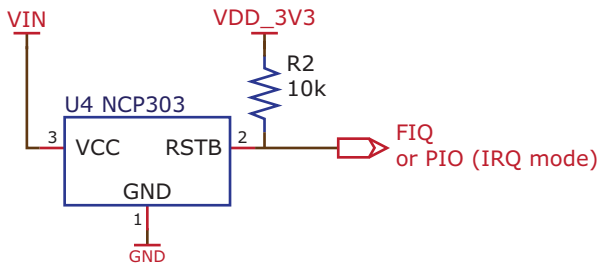
It is possible to add an input power-fail detection circuit to the basic reference schematic depicted in Figure 2-1.The principle, described in Figure 3-4, is to monitor the input voltage VIN and to warn the processor with an interrupt in case of power loss. The Fast Interrupt (FIQ) input or any I/O configured as an interrupt input may be used. Upon this interrupt request, a software power-off sequence is started during which some data storage and/or service shutdown may be performed depending on the remaining ”ON” time. This power-off sequence then ends by setting the bit SHDW in SHDW_CR. The SHDN pin falls down to 0 which turns off the power supply, as described in Section 2.2.2 “Shutdown Description”.

Figure 3-4. Power Loss Management Principle



To monitor the input voltage VIN, several solutions are possible depending on available resources at system level. (e.g., a system with a voltage reference on-board requires a voltage comparator). Figure 3-5 shows one possible implementation using an integrated voltage monitor circuit.

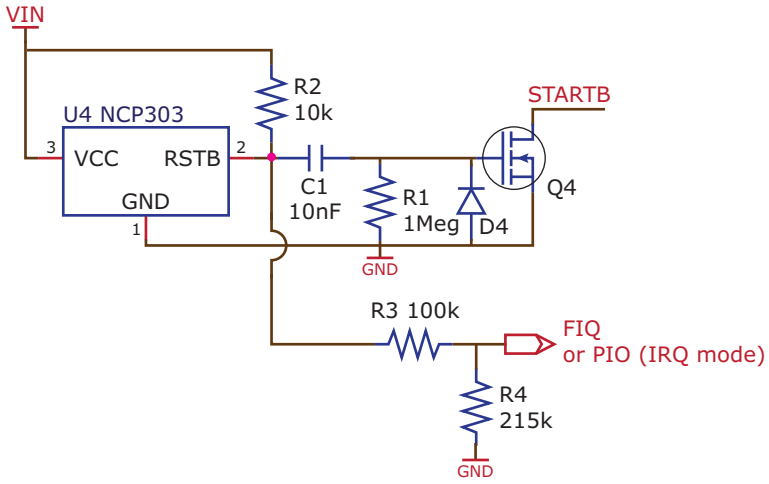
Figure 3-5. Input Power-Fail Detection Example



In some applications, the input voltage monitor circuit may be used to generate both the STARTB signal as well as the interrupt signal. In this case, the voltage monitor output must not be directly connected to the eMPU I/O. It must be isolated by a series resistor as shown in Figure 3-6. When VDD_3V3 is not started, if the R3 resistor is not inserted, the internal protection diodes of the eMPU I/O will stick the output signal of the voltage detector U4. The R4 resistor is inserted to scale down the VIN level of the monitor output to the VDD_3V3 level of the eMPU I/O

used as interrupt source. Due to the insertion of R3, the eMPU I/O is forced with relatively high impedance. For this reason, the integrated pull-up and pull-down resistors of this I/O must be disabled.

Figure 3-6. Voltage Monitor at Start-Up and Shutdown



3.5 Discrete Components Selection

The discrete components listed in this application note are given as implementation examples. They are not strong recommendations. The reader may adapt the presented schematics to his specific needs and while respecting the basic principles described in the previous sections. As the focus of this application note is the solution cost, only low-cost components are selected. This may lead to “over-sized” components compared to the application need because they give the best price in this particular case. While cost and ease of procurement were the primary criteria for component selection, other criteria have been used to select other types of components:

- Regulators: Devices should feature an enable input and a power-good output as they ease the design of the power sequencing and reset generation circuits.
- NMOS transistors: Low threshold voltage (< 2V) devices are used to ensure safe commutation in all cases (VDDBU may be as low as 1.8V in some applications).
- Diodes: General-purpose, small signal devices with a low reverse current specification (<20nA at 20V and 25°C) are suitable.

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