AVR 8-bit Microcontrollers

AVR42769: Differences Between ATmega324 and ATmega324PB

APPLICATION NOTE

Introduction

This application note assists users of Atmel® ATmega324 variants to understand the differences and use of the Atmel ATmega324PB.

ATmega324PB is not a drop-in replacement for ATmega324 variants, but a new device. However, the functions are backward compatible with the existing ATmega324 functions. Existing code for these devices will work with the new devices without changing existing configuration or enabling new functions. The code that is available for your existing ATmega324 variants will continue to work with the new ATmega324PB device.

The ATmega324PB features the successful Atmel QTouch® Peripheral Touch Controller (PTC).

For differences in errata, typical, and electrical characteristics between ATmega324 variants and ATmega324PB, refer to the specific device datasheets.

For complete device details, refer to the latest version of the ATmega324PB datasheet available at www.atmel.com.

Features

- Pin functionality difference
- Code compatibility
- Enhancement and added features
- Updated features

Note: Code compiled for ATmega324 variants are compatible and can be executed in the ATmega324PB device (exception, see this application note). Whereas, reverse code compatibility is not guaranteed.

Table of Contents

1. Pin Functionality Difference

1.1. Additional Pin Functionalities

ATmega324PB supports seven additional GPIOs on PORTE [6:0].

The GPIO pins PE0, PE1, and PE4 are assigned to Pin7, Pin8, and Pin29. PE0, PE1, and PE4 are multiplexed with XTAL2, XTAL1, and AREF.

The GPIO pin PC5 is multiplexed with ACO, the Analog Comparator output.

Pin17(VCC), Pin18(GND), Pin38 (VCC), and Pin39 (GND) are replaced by PE2, PE3, PE5, and PE6 respectively.

Table 1-1. Pin Functionality Difference between ATmega324 Variants and ATmega324PB

44-pin TQFP/MLF package	ATmega324 variants	ATmega324PB
Pin 7	XTAL2	PE0 (XTAL2)
Pin 8	XTAL1	PE1 (XTAL1)
Pin 17	VCC	PE2
Pin 18	GND	PE3
Pin 29	AREF	PE4 (AREF)
Pin 38	VCC	PE5
Pin 39	GND	PE6

1.2. Alternate Pin Configuration

The alternate pin configurations are:

- **XTAL2 - Port E Bit 0**

PE0 can also be multiplexed with XTAL2 input.

- **XTAL1 - Port E Bit 1**

PE1 can also be multiplexed with XTAL1 input.

- **AREF Port E Bit 4**

PE4 can be multiplexed with AREF for the A/D Converter.

2. Enhancement and Additional Features in ATmega324PB

Compared to existing ATmega324 variants, the following enhancements or additional features are available in ATmega324PB:

- PTC - Peripheral Touch Controller
- CFD - Clock Failure Detection mechanism
- OCM1C2 - Output Compare Modulator
- USART start frame detection is available in all sleep modes
- Analog Comparator output is available on a pin. This pin is multiplexed with PC5
- Unique device ID to identify the device
- Additional SPI
- Additional TWI
- Additional Timer/Counters

2.1. PTC - Peripheral Touch Controller

The ATmega324PB features the successful Atmel QTouch Peripheral Touch Controller (PTC). The Peripheral Touch Controller (PTC) acquires signals in order to detect touch on capacitive sensors. The external capacitive touch sensor is typically formed on a PCB, and the sensor electrodes are connected to the analog front-end of the PTC through the I/O pins in the device. The PTC supports both self- and mutual-capacitance sensors.

The PTC supports 32 buttons in self-capacitance mode and up to 256 buttons in mutual-capacitance mode. It is possible to mix and match self- and mutual-capacitance sensors. Only one pin is required per electrode — no external components are required providing considerable savings on the BOM cost compared to competing solutions.

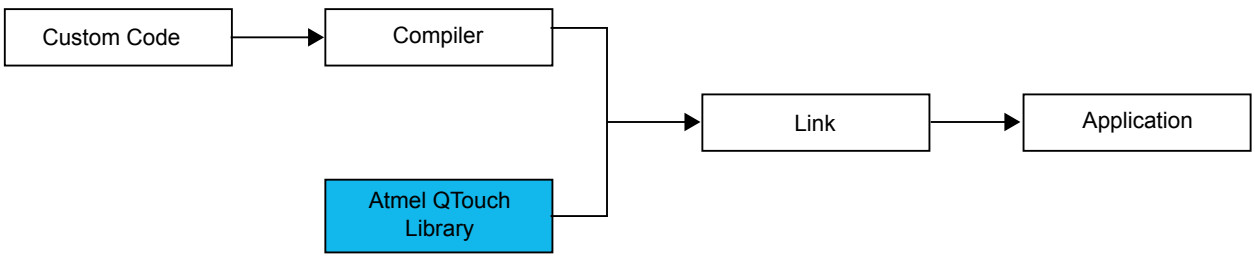
In mutual-capacitance mode, sensing is performed using capacitive touch matrices in various X-Y configurations. Whereas in self-capacitance mode, the PTC requires only one pin (Y-line) for each touch sensor.

Refer to the chapter I/O Multiplexing in the ATmega324PB device datasheet for details on the pin mapping for this peripheral. A signal can be mapped on several pins.

2.1.1. PTC Functional Description

To access the PTC, the user must use the QTouch Composer tool to configure and link the QTouch Library firmware with the application code. QTouch Library can be used to implement buttons, sliders, wheels, and proximity sensor in a variety of combinations on a single interface.

Figure 2-1. QTouch Library Usage



2.2. CFD - Clock Failure Detection Mechanism

Clock Failure Detection and Switching Mechanism is a new feature introduced in ATmega324PB. This digital logic detects the failure of the low-power crystal oscillator and external clocks. If a failure is detected, this logic will automatically switch the clock to 1MHz internal RC system clock.

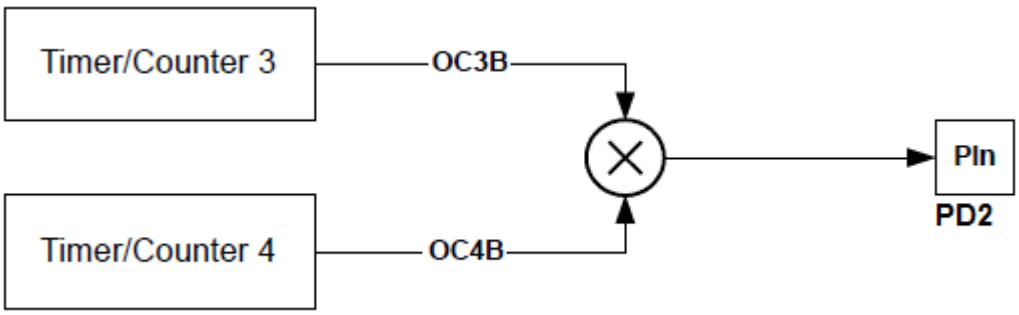
The Clock Failure Detection mechanism for the device is enabled by an active high fuse. When the CFD fuse is enabled, the 128kHz oscillator will be enabled and the CFD circuit works using that clock.

CFD will be automatically disabled when the chip enters power save/down sleep mode. It will be enabled by itself when the chip returns to active mode. CFD will be enabled only when the system frequency is higher than 256kHz.

2.3. OCM1C2 - Output Compare Modulator

The Output Compare Modulator (OCM) allows generation of waveforms modulated with a carrier frequency. The modulator uses the outputs from the Output Compare Unit B of the 16-bit Timer/Counter3 and the Output Compare Unit of the 16-bit Timer/Counter4. When the modulator is enabled, the two output compare channels are modulated together as shown in the block diagram.

Figure 2-2. Output Compare Modulator - Block Diagram



The Output Comparator unit 3B and Output compare unit 4B shares the PD2 port pin for output. The outputs of the Output Compare units (OC3B and OC4B) overrides the normal PORTD2 bit when one of them is enabled (that is, when COMnx1:0 is not equal to zero). When both OC3B and OC4B are enabled simultaneously, the modulator is automatically enabled.

2.4. USART

ATmega324PB has one additional USART with start-of-frame detection, which can wake up the MCU from all sleep modes when a start bit is detected. Two USART modules are available in the ATmega324PB with individual configuration registers, refer ***Register Description*** section under the USART module in the ATmega324PB device datasheet for detailed description of these registers. They also have separate TX, RX, and XCK pins. For details on the pin mapping for this peripheral, refer to the I/O Multiplexing section in the ATmega324PB device datasheet.

When a high-to-low transition is detected on RxDn, the internal 8MHz oscillator is powered up and the USART clock is enabled. After start-up the rest of the data frame can be received, provided that the baud rate is slow enough to allow the internal 8MHz oscillator to start. Start-up time of the internal 8MHz oscillator varies with supply voltage and temperature.

The USART start frame detection works both in asynchronous and synchronous modes. It is enabled by writing the Start Frame Detection Enable bit (SFDEn). If the USART Start Interrupt Enable (RXSIE) bit is set, the USART Receive Start Interrupt is generated immediately when a start is detected.

When using the feature without the Receive Start Interrupt, the start detection logic activates the internal 8MHz oscillator and the USART clock while the frame is being received only. Other clocks remain stopped until the Receive Complete Interrupt optionally wakes up the MCU.

The maximum baud rate depends on the sleep mode the device is woken up from.

In synchronous mode:

- **Idle sleep mode:** system clock frequency divided by four
- **Standby or Power-down:** 500kbps

In asynchronous mode:

- **Idle sleep mode:**the same as in active mode

2.5. Analog Comparator

Analog Comparator output is available on a pin. The analog comparator output is tied to PC5 when the AC output is enabled by writing a one to the Analog Comparator Output Enable bit (ACOE) in “ACSR0 – Analog Comparator Output Control Register”.

2.6. Unique Device ID

In Atmel ATmega324PB, each individual part has a specific and unique device ID. This can be used to identify a specific part while it is in the field. The Unique Device ID consists of nine serial number bytes in which the user can access directly from registers. The register address locations are located at 0xF0 to 0xF8.

2.7. Additional SPI

ATmega324PB has one Additional SPI. There are two SPIs with individual configuration registers. Refer to the ***Register Description*** section in the SPI peripheral in the ATmega324PB device datasheet for detailed description of these registers. They also have a separate MOSI, MISO, SCK, and SS pins. Refer to the ***I/O Multiplexing*** section in the ATmega324PB device datasheet for details about the pin mapping for this peripheral.

2.8. Additional TWI

ATmega324PB has one additional byte-oriented 2-wire serial interface (TWI). There are two TWI peripherals with individual configuration registers. Refer the ***Register Description*** section under the TWI 2-wire Serial Interface module in the ATmega324PB device datasheet for detailed description of these registers. Separate SDA and SDL pins are also available. Refer to the section I/O ***Multiplexing*** in the ATmega324PB device datasheet for details on the pin mapping for this peripheral.

2.9. Additional Timer/Counters

ATmega324PB has two additional 16-bit Timer/Counters(**TC3** and **TC4**) with separate Prescaler, Compare Mode, and Capture Mode. There are three 16-bit Timer/Counters (**TC1**, **TC3**, and **TC4**) and ten

PWM channels available in ATmega324PB. Refer to the ***I/O Multiplexing*** section in the ATmega324PB device datasheet for details about the pin mapping for this peripheral.

3. Updated Features

3.1. Full Swing Oscillator

Clock source options of the ATmega324 variants include full swing crystal oscillator, which can be selected by configuring the flash fuse. However, in the new ATmega324PB, the full swing crystal oscillator is removed. Refer to the ***Clock Sources*** in the respective datasheet.

Table 3-1. Full Swing Oscillator Removed from ATmega324PB

Device function	ATmega324PB	ATmega324PA	ATmega324P	ATmega324A
Full swing crystal oscillator	No	Yes	Yes	Yes

3.2. NVM

Write wait delay for NVM in ATmega324PB is increased when compared to ATmega324 variants.

Table 3-2. Minimum Wait Delay for NVM

Symbol	ATmega324PB	ATmega324 PA variants	ATmega324P variants	ATmega324 A variants	Unit
t_{WD_FLASH}	4.5	2.6	2.6	2.6	ms
t_{WD_ERASE}	9.0	10.5	10.5	10.5	ms

3.3. Signature

All Atmel microcontrollers have a three-byte signature code, which identifies the device. This code can be read in both serial and parallel mode, also when the device is locked. The three bytes reside in a separate address space. For the device ID, namely the device signature bytes, there are differences between ATmega324PB and ATmega324 variants. See below table for more detail.

Table 3-3. Device ID Differences

Part	Signature Bytes Address		
	0x000	0x001	0x002
ATmega324A	0x1E	0x95	0x15
ATmega324P	0x1E	0x95	0x08
ATmega324PA	0x1E	0x95	0x11
ATmega324PB	0x1E	0x95	0x17

4. Register Description

4.1. PINE – Port E Input Pins Address

Name: PINE
Offset: 0x2C
Reset: N/A
Property: When addressing as I/O Register: address offset is 0x0C

Bit	7	6	5	4	3	2	1	0
					PINE3	PINE2	PINE1	PINE0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – PINE3: Port E Input Pin Address 3
Writing to the pin register provides toggle functionality for I/O.

Bit 2 – PINE2: Port E Input Pin Address 2
Writing to the pin register provides toggle functionality for I/O.

Bit 1 – PINE1: Port E Input Pin Address 1
Writing to the pin register provides toggle functionality for I/O.

Bit 0 – PINE0: Port E Input Pin Address 0
Writing to the pin register provides toggle functionality for I/O.

4.2. DDRE – Port E Data Direction Register

Name: DDRE
Offset: 0x2D
Reset: 0x00
Property: When addressing I/O Registers as data space the offset address is 0x0D

Bit	7	6	5	4	3	2	1	0
					DDRE3	DDRE2	DDRE1	DDRE0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – DDRE3: Port E Data Direction 3

Bit 2 – DDRE2: Port E Data Direction 2

Bit 1 – DDRE1: Port E Data Direction 1

Bit 0 – DDRE0: Port E Data Direction 0

4.3. PORTE – Port E Data Register

Name: PORTE
Offset: 0x2E
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x0E

Bit	7	6	5	4	3	2	1	0
					PORTE3	PORTE2	PORTE1	PORTE0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – PORTE3: Port E Data 3

Bit 2 – PORTE2: Port E Data 2

Bit 1 – PORTE1: Port E Data 1

Bit 0 – PORTE0: Port E Data 0

4.4. XFDCSR – XOSC Failure Detection Control and Status Register

Name: ACSRB
Offset: 0x62
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
							XFDIF	XFDIE
Access							R	R/W
Reset							0	0

Bit 1 – XFDIF: Failure Detection Interrupt Flag
This bit is set when a failure is detected. It serves as status bit for CFD.

Note: This bit is read only.

Bit 0 – XFDIE: Failure Detection Interrupt Enable
Setting this bit will enable the interrupt, which will be issued when XFDIF is set. This bit is enable only. Once enabled, it is not possible for the user to disable.

4.5. UCSRD – USART Control and Status Register D

When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these offset addresses. The device is a complex microcontroller with more peripheral units than can be supported within the 64 locations reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

Name: UCSRD
Offset: 0xC3
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	RXSIE		SFDE					
Access	R/W	R/W	R/W					
Reset	0	0	0					

Bit 7 – RXSIE: USART RX Start Interrupt Enable
Writing this bit to one enables the interrupt on the RXS flag. In sleep modes this bit enables start frame detector that can wake up the MCU when a start condition is detected on the RxD line. The USART RX Start Interrupt is generated only if the RXSIE bit, the Global Interrupt Enable flag, and RXS are set.

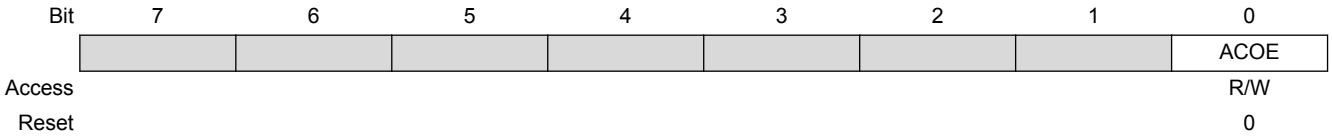
Bit 5 – SFDE: Start Frame Detection Enable
Writing this bit to one enables the USART Start Frame Detection mode. The start frame detector is able to wake up the MCU from sleep mode when a start condition, i.e. a high (IDLE) to low (START) transition, is detected on the RxD line.

Table 4-1. USART Start Frame Detection Modes

SFDE	RXSIE	RXSIE (RX complete interrupt enable)	Description
0	x	x	Start frame detection disabled
1	0	0	Reserved
1	0	1	Start frame detector enabled. The RXC flag will wake up the MCU from all sleep mode.
1	1	0	Start of frame detector enabled. The RXS flag will wake up the MCU from all sleep mode.

4.6. ACSRB – Analog Comparator Control and Status Register

Name: ACSRB
Offset: 0x4F
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x2F



Bit 0 – ACOE: Analog Comparator Output Enable
Setting this bit makes the output of AC available on PE0. If this bit is not set, PE0 can be used as general I/O pin.

4.7. Serial Number Byte 8 to 0

Name: Serial Number Byte 8 to 0
Offset: 0xF0 + n*0x01 [n=0..8]
Reset: 0x00
Property: R/W

Bit	7	6	5	4	3	2	1	0
	SNOBR[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – SNOBR[7:0]: Device ID byte 0

5. Revision History

Doc. Rev.	Date	Comments
42769A	09/2016	Initial document release

Atmel | Enabling Unlimited Possibilities®

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**