Section 24. Programming and Diagnostics

HIGHLIGHTS

This section of the manual contains the following major topics:

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Programming and Diagnostics

> **Note:** This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices.
>
> Please consult the note at the beginning of the **"Special Features"** chapter in the current device data sheet to check whether this document supports the device you are using.
>
> Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

24.1   INTRODUCTION

dsPIC33F/PIC24H devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application. These features allow system designers to include:

- Simplified field programmability using two-wire interfaces
- Enhanced debugging capabilities
- Boundary Scan Testing (BST) for device and board diagnostics

dsPIC33F/PIC24H devices incorporate three different programming and diagnostic modalities that provide a range of functions to the user. Table 24-1 summarizes these functions.

Table 24-1:   Comparison of dsPIC33F/PIC24H Programming and Diagnostic Features

Feature	Interface	Device Integration	Functions
In-Circuit Serial Programming™ (ICSP™) Programming Method	PGCx and PGDx pins	Integrated with device core	Programming, Debugging
Enhanced ICSP Programming Method	PGCx and PGDx pins	Hardware integrated with device core; firmware based control	Programming
Joint Test Action Group (JTAG)	TDI, TDO, TMS and TCK pins	Peripheral to device core; partly integrated with I/O logic	Programming, BST diagnostics

24.2   IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

The ICSP capability is Microchip's proprietary process for device programming in the user application. ICSP is the most direct method to program the device, whether the controller is embedded in a system or loaded into a device programmer.
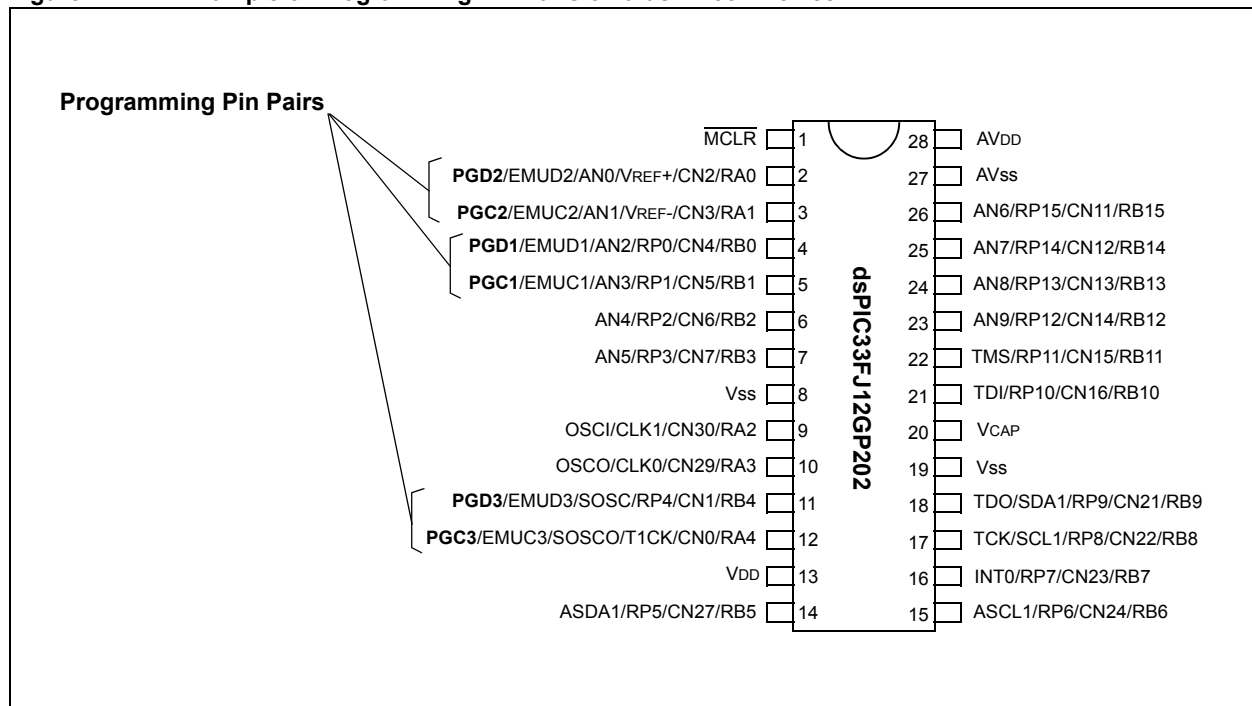
24.2.1   ICSP Interface

The ICSP interface uses a two-pin communication interface. Individual ICSP pin pairs are indicated by number (for example, PGC1/PGD1), and are generally referred to as PGCx and PGDx. The programming data (PGDx) pins functions as both input and output, allowing programming data to be read in and device information to be read out on command. The programming clock (PGCx) pins clock data in and control the overall process.

Most dsPIC33F/PIC24H devices have more than one pair of PGCx and PGDx pins, which are multiplexed with other I/O or peripheral functions, as illustrated in Figure 24-1. The multiple PGCx/PGDx pin pairs provide additional flexibility in system design by allowing the user to incorporate ICSP on the pair of pins that are least constrained by the circuit design. All PGCx and PGDx pins are functionally attached together and behave identically. Any one pair can be used for successful device programming. The only limitation is that both pins from the same pair must be used.

In addition to the PGCx and PGDx pins, the ICSP requires that all voltage supply and ground pins on the device must be connected. The MCLR pin, which is used with PGCx to enter and control the programming process, must also be connected to the programming device.

Figure 24-1:   Example of Programming Pin Pairs on a dsPIC33F Device

24.2.2   ICSP Operation

ICSP mode uses a combination of internal hardware and external control to program the specific device. Programming data and instructions are provided on the PGDx pin. A special set of 4-bit commands, combined with the standard dsPIC33F/PIC24H instructions, control the overall process of writing to the program memory. The PGDx pin also returns data to the external programmer in response to queries.

The device programming process is controlled by manipulating the PGCx and $\overline{MCLR}$ pins. Entry into and exit from ICSP mode involves applying (or removing) voltage to $\overline{MCLR}$, while supplying a code sequence to the PGDx pin and a clock to the PGCx pin.

Any one of the PGCx/PGDx pairs can be used for device programming. During device programming, the clock train on the PGCx pin is also used to indicate the difference between 4-bit commands, programming control commands and payload data to be programmed.

The internal process is regulated by a state machine built into the dsPIC33F/PIC24H core logic; however, overall control of the internal process must be provided by the external programming device. Microchip programming devices, such as MPLAB® PM3 (used with MPLAB® IDE development software), include the necessary hardware and algorithms to manage the programming process for dsPIC33F/PIC24H devices. For more information on designing an individual programming interface for a dsPIC33F/PIC24H device, refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152).

24.2.3   ICSP and In-Circuit Debugging

The ICSP method also provides a hardware channel for in-circuit debugging, which allows external control of user software debugging. Using the hardware interface and software environment, you can force the device to single step through its code, track the actual content of multiple registers, and set software breakpoints.

To use the in-circuit debugging, an external system must load a debugger executive program into the device. This task is handled automatically by many debugging tools, such as MPLAB REAL ICE™ and MPLAB ICD 3. For dsPIC33F/PIC24H devices, the program is loaded into the executive program memory in the Configuration memory space. Although memory is implemented and code can be executed from these locations, the executive memory space is not available to the user-assigned application during normal operating modes. For more information, refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152).

Because of the memory location, use of the debug executive has no impact on the size of the user-assigned application being examined. The executive memory space allows use of the entire program memory for program code, without leaving reserve space for application debugging. In addition, the use of entire program memory for program code means that the program memory content in the normal and debug states is identical, which simplifies troubleshooting.

Depending on the specific dsPIC33F/PIC24H device, one or more ICSP ports can be used for device programming. However, only one of these ICSP ports can be used for in-circuit debugging. Use the following process to select which part to activate for debugging through your MPLAB IDE setup:

1. In the MPLAB IDE, select *Configure > Configuration Bits* to display the Configurations Bits window.
2. In the Configuration Bits window, select the specific debug pair setting under the Comm Channel Select category.

> **Note:**   For more details on the configuration memory space, refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152).

24.3   ENHANCED ICSP

The enhanced ICSP protocol is an extension of the standard ICSP method. Enhanced ICSP uses the same physical interface as the original ICSP, but changes the location and execution of programming control.

ICSP mode uses a simple state machine to control each step of the programming process; however, the state machine is controlled by an external programmer. In contrast with ICSP, the enhanced ICSP uses an on-board bootloader, known as the program executive, to manage the programming process. While overall device programming is still overseen by an external programmer, the program executive manages most of the tasks that must be directly controlled by the programmer in standard ICSP.

The program executive implements its own command set, wider in range than the original ICSP, that can directly erase, program and verify the microcontroller's program memory. This avoids the need to repeatedly run ICSP command sequences to perform simple tasks. As a result, enhanced ICSP mode can program or reprogram a device more quickly than ICSP mode.

Similar to the in-circuit debugger executive, the program executive does not reside in the user-assigned application program memory space. It is also loaded into the executive program memory. Since the debugger and enhanced ICSP executives both use this memory space, in-circuit debugging is not available while enhanced ICSP mode is being used for programming.

The program executive is not preprogrammed into dsPIC33F/PIC24H devices. If you need enhanced ICSP, you must use standard ICSP to program the executive to the executive memory space. You can setup the enhanced ICSP directly in your user software, or automatically using a compatible Microchip programming system.

For more information on enhanced ICSP and the program executive, refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152).

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Programming and Diagnostics

24.4   JTAG BOUNDARY SCAN

As the complexity and density of board designs increase, testing electrical connections between the components on completely assembled circuit boards provides many challenges. To address these challenges, the Joint Test Action Group (JTAG) developed a method for the BST that has been standardized as IEEE 1149.1-2001, *"IEEE Standard Test Access Port and Boundary Scan Architecture"*. Since its adoption, many microcontroller manufacturers have added device programming to the capabilities of the test port.
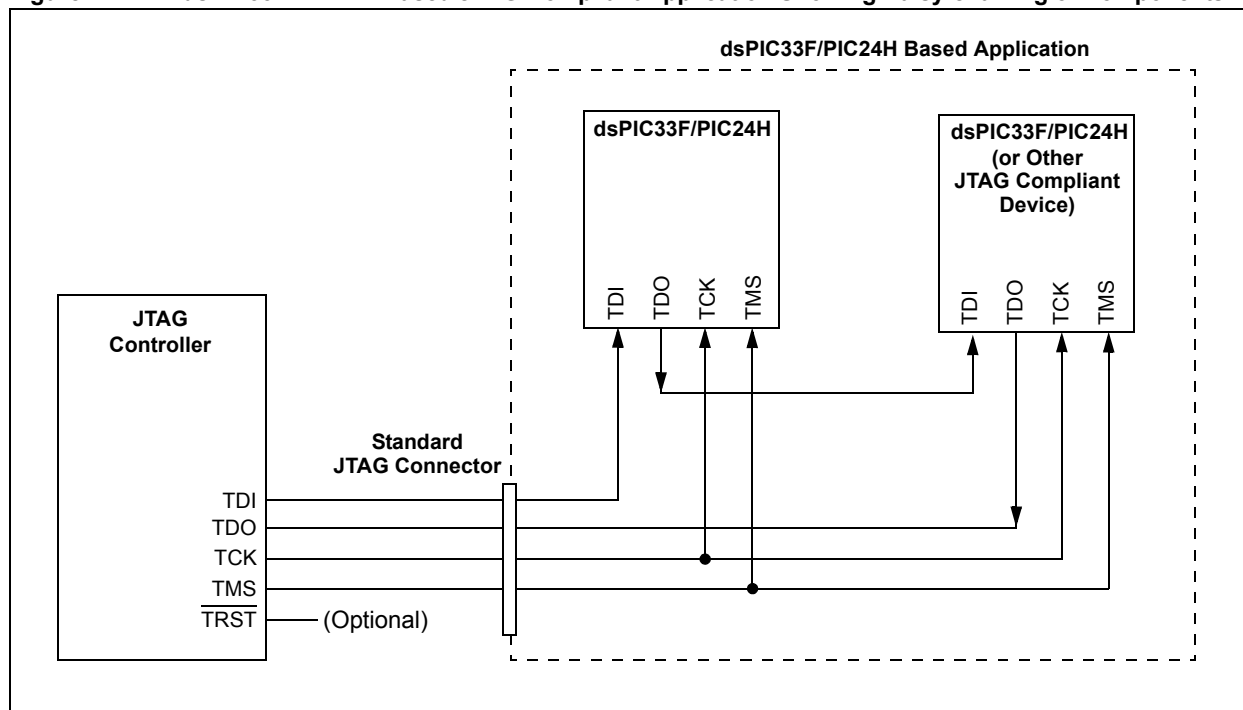
The JTAG boundary scan method adds a shift register stage adjacent to each of the component's I/O pins, which permits signals at the component boundaries to be controlled and observed using a defined set of scan test principles. An external tester or controller provides instructions and reads the results serially. The external device also provides common clock and control signals. Depending on the implementation, access to all test signals is provided through a standardized 4-pin or 5-pin interface.

In system level applications, individual JTAG enabled components are connected through individual testing interfaces (in addition to their more standard application specific connections). Devices are connected in a series or daisy-chained fashion, with the test output of one device connected exclusively to the test input of the next device in the chain. Instructions in the JTAG boundary scan protocol allow the testing of any one device in the chain, or any combination of devices, without testing the entire chain. In the JTAG boundary scan method, connections between components, as well as connections at the boundary of the application, can be tested.

Figure 24-2 illustrates a typical application incorporating the JTAG boundary scan interface. In this figure, a dsPIC33F/PIC24H device is daisy-chained to a second JTAG compliant device. The Test Data Input (TDI) line from the external tester supplies data to the TDI pin of the first device in the chain (in this case, the dsPIC33F/PIC24H device). The resulting test data for this two-device chain is provided from the Test Data Output (TDO) pin of the second device to the TDO line of the tester.

This section describes the JTAG module and its general use. For more information on using the JTAG interface for device programming, refer to **24.4.6 "JTAG Device Programming"**.

Figure 24-2:   dsPIC33F/PIC24H Based JTAG Compliant Application Showing Daisy-chaining of Components

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In dsPIC33F/PIC24H devices, the hardware for the JTAG boundary scan is implemented as a peripheral module (that is, outside of the CPU core) with additional integrated logic in all I/O ports. The dsPIC33F/PIC24H devices implement a 4-pin JTAG interface, as provided in Table 24-2.
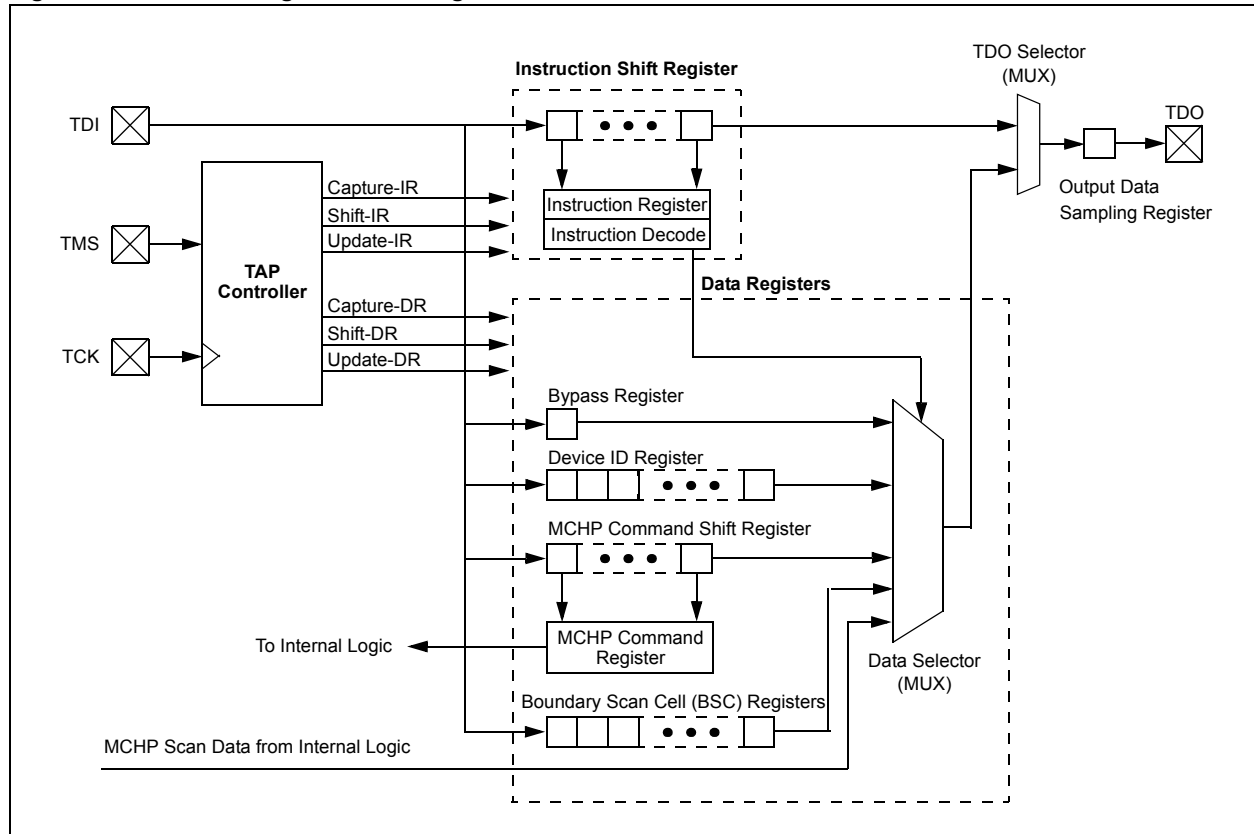
Table 24-2:   4-pin JTAG Interface

Interface Pin	Function
Test Clock Input (TCK)	Provides the clock for test logic.
Test Mode Select Input (TMS)	Used by the Test Access Port (TAP) to control test operations.
Test Data Input (TDI)	Serial input for test instructions and data.
Test Data Output (TDO)	Serial output for test instructions and data.

A logical block diagram of the JTAG module illustrated in Figure 24-3 consists of the following key elements:

- Test Access Port (TAP) interface pins (TDI, TMS, TCK and TDO)
- TAP controller
- Instruction Shift Register (ISR) and Instruction Register (IR)
- Data registers

Figure 24-3:   JTAG Logical Block Diagram

24.4.1 Test Access Port (TAP) and TAP Controller

The Test Access Port (TAP) on the dsPIC33F/PIC24H device family, is a general purpose port that provides test access to many built-in support functions and test logic defined in IEEE Standard 1149.1. The TAP controller and the associated boundary scan pins are disabled by programming the JTAG Enable bit (JTAGEN) to '0' in the Configuration register (FICD). The TAP controller, by default, is enabled in unprogrammed state of the JTAGEN bit. While enabled, the designated I/O pins become dedicated TAP pins.

Use the following process to enable/disable the JTAG port through your MPLAB IDE setup:
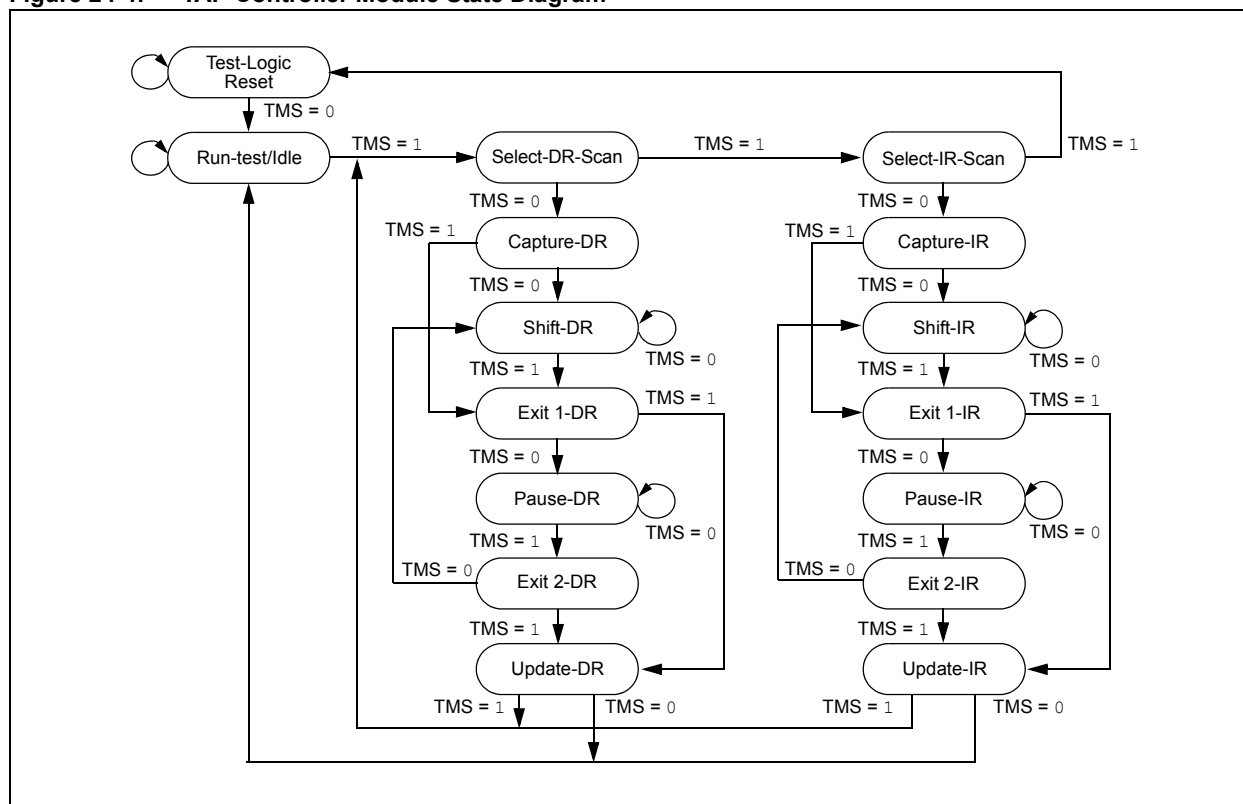
1. In the MPLAB IDE, click *Configure > Configuration Bits* to display the Configurations Bits window.
2. In the Configuration Bits window, select the Enable/Disable setting under the JTAG Port Enable category.

> **Note:** For more details on the FICD register, refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152).

To minimize I/O loss due to JTAG scans, the optional TAP Reset ($\overline{\text{TRST}}$) input pin, specified in the IEEE Standard 1149.1, is not implemented on dsPIC33F/PIC24H devices. For convenience purpose, a "soft" TAP Reset is included in the TAP controller, using the TMS and TCK pins. To force a port Reset, apply a logic high to the TMS pin for at least five rising edges of TCK. Device resets including Power-on Reset (POR), do not automatically result in a TAP Reset. This must be done by the external JTAG controller using the soft TAP Reset.

The TAP controller on the dsPIC33F/PIC24H device family is a synchronous finite state machine that implements the standard 16 states for JTAG scans. Figure 24-4 illustrates all module states of the TAP controller. All BST instructions and test results are communicated through the TAP controller through the TDI pin in a serial format, with the Least Significant bit (LSb) first.

Figure 24-4: TAP Controller Module State Diagram

By manipulating the state of the TMS and the clock pulses on the TCK, the TAP controller can be moved through all of the defined module states to capture, shift and update various instruction and/or data registers. Figure 24-4 illustrates the state changes on TMS as the controller cycles through its state machine. Figure 24-5 illustrates the timing of the TMS and TCK, while transitioning the controller through the appropriate module states for shifting in an instruction. In Figure 24-5, the sequence demonstrates how a TAP controller reads an instruction.
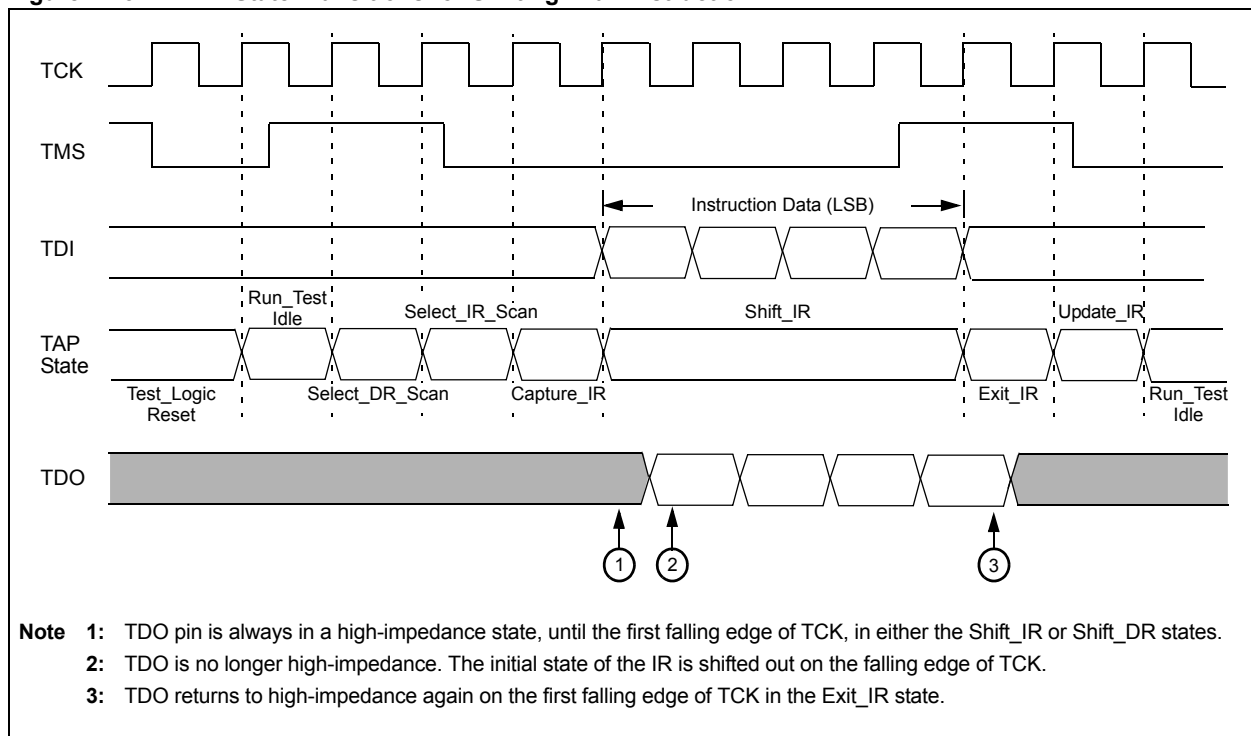
All TAP controller states are entered on the rising edge of the signal on the TCK pin. The TAP controller starts in the Test-Logic Reset state. As the state of the TAP controller is dependent on the previous instruction, and therefore could be unknown, it is a good programming practice to begin in the Test-Logic Reset state.

When TMS is asserted low on the next rising edge of the TCK, the TAP controller moves into the Run-test/Idle state. On the next two rising edges of the TCK, TMS is high, which moves the TAP controller to the Select-IR-Scan state.

On the next two rising edges of TCK, TMS is held low, which moves the TAP controller into the Shift-IR state. An instruction is shifted in to the Instruction Shift register through the TDI on the next four rising edges of TCK. After the TAP controller enters this state, the TDO pin goes from a high-impedance state to active. The controller shifts out the initial state of the IR on the TDO pin, on the falling edges of TCK, and continues to shift out the contents of the IR while in the Shift-IR state. The TDO returns to the high-impedance state on the first falling edge of TCK upon exiting the shift state.

On the next three rising edges of TCK, the TAP controller exits the Shift-IR state, updates the IR and then moves back to the Run-test/Idle state. Data, or another instruction, can now be shifted in to the appropriate data or IR.

Figure 24-5: TAP State Transitions for Shifting in an Instruction

Note 1: TDO pin is always in a high-impedance state, until the first falling edge of TCK, in either the Shift_IR or Shift_DR states.
2: TDO is no longer high-impedance. The initial state of the IR is shifted out on the falling edge of TCK.
3: TDO returns to high-impedance again on the first falling edge of TCK in the Exit_IR state.

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24.4.2   JTAG Registers

The JTAG module uses a number of registers of various sizes as part of its operation. None of the JTAG registers are located within the device data memory space. They cannot be directly accessed by the user-assigned application in normal operating modes.

24.4.2.1   INSTRUCTION SHIFT REGISTER AND INSTRUCTION REGISTER

The 4-bit IR allows an instruction to be shifted into the device. The instruction selects the data register to access. The parallel output from the IR is latched to protect from the transient data patterns that occur in its shift register stages as the new instruction data is entered. The latched parallel output is controlled, so that it can change state only in the Update-IR and Test-Logic Reset controller states. A list and description of the implemented instructions are provided in **24.4.4 "JTAG Instructions"**.

24.4.2.2   DATA REGISTERS

The dsPIC33F/PIC24H device family supports the JTAG data registers listed in Table 24-3.

Table 24-3:   JTAG Data Registers

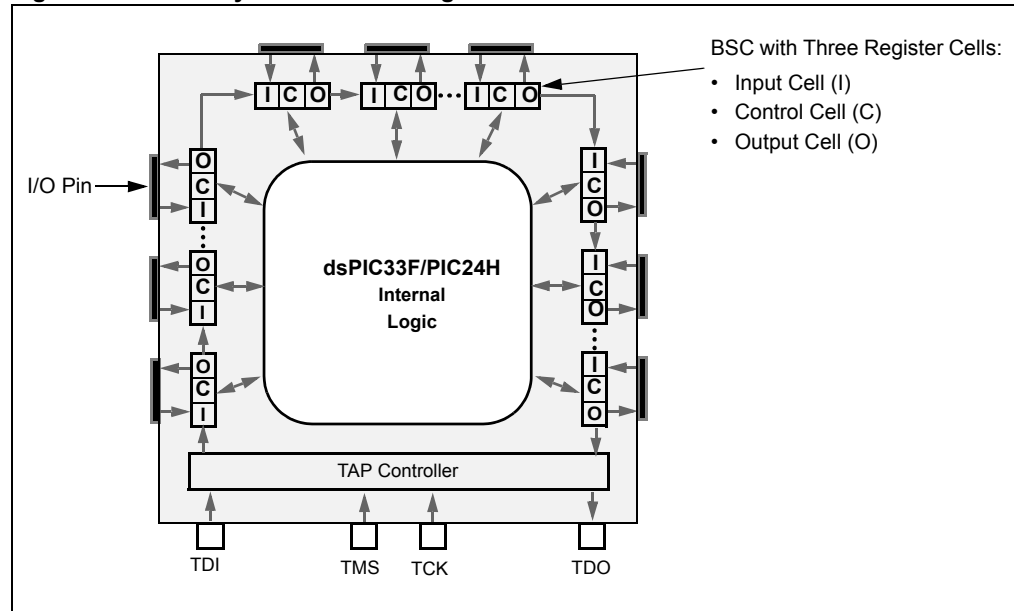| Register	Function
Bypass Register	Provides a minimum length serial path for the movement of test data between TDI and TDO. This path can be selected when no other test data register needs to be accessed during a board-level test operation.
	Use of the Bypass register in a component speeds access to test data registers in other components on a board-level test data path.
Microchip Command Shift Register	This 8-bit shift register shifts in Microchip device-specific commands. The parallel output from the shift register is latched to protect from the transient data patterns that occur in its shift register stages as a new command is entered.
Device ID Register	This 32-bit device IR allows the manufacturer, part number and variant of a component to be determined. For more information on the Device ID register and JTAG ID register, refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152).
Boundary Scan Register (BSR)	Consists of a number of cells combined to form a single shift-register-based path that is connected between TDI and TDO when an appropriate instruction is selected.

24.4.3 Boundary Scan Register (BSR)

The BSR is a large shift register that consists of all the I/O Boundary Scan Cells (BSCs) daisy-chained together, as illustrated in Figure 24-6. Each I/O pin has one BSC. Each BSC contains three BSC registers: an input cell register, an output cell register and a control cell register. When the SAMPLE/PRELOAD or EXTEST instructions are active, the BSR is placed between the TDI and TDO pins, with the TDI pin as the input and the TDO pin as the output.

The size of the BSR depends on the number of I/O pins on the device. For example, the dsPIC33FJ256GP710 has 82 I/O pins. Three BSC registers for each of the 82 I/Os yields a BSR length of 246 bits. Information on the I/O port pin count for a specific device is found in the specific Boundary Scan Description Language (BSDL) files.

> **Note:** The BSC is not used for power supply pins (V_DD, V_CAP, V_SS, AV_DD and AV_SS). The pins that have the JTAG interconnect function and JTAG control are not part of the scan-chain and are not JTAG testable.

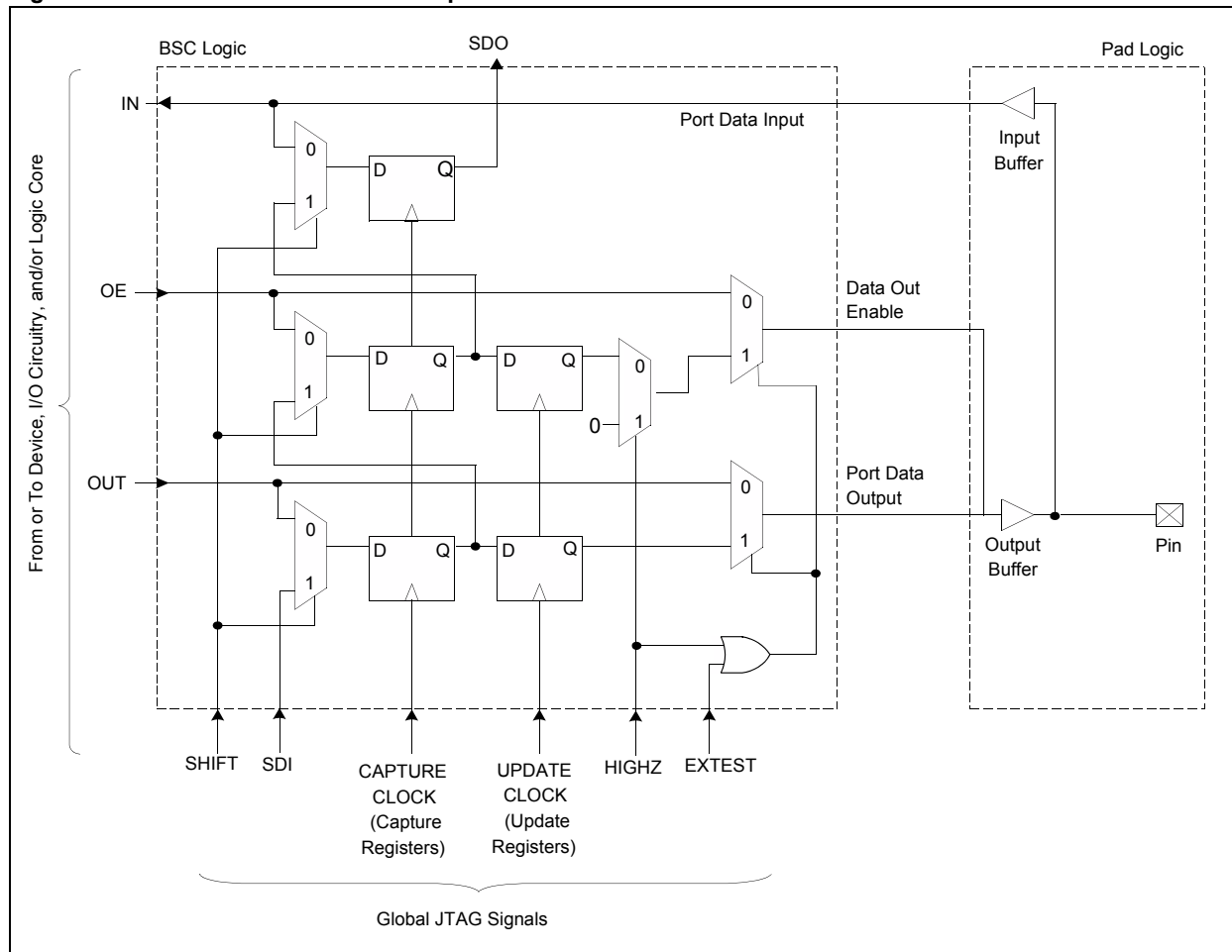**Figure 24-6: Daisy-chained BSC Registers on a dsPIC33F/PIC24H Device**

24.4.3.1   BOUNDARY SCAN CELL (BSC)

The BSC captures and overrides I/O input or output data values when JTAG is active. The BSC consists of three single-bit capture register cells and two single-bit holding register cells. The capture cells are daisy-chained to capture the port's input, output and control (output enable) data. The capture cells also pass JTAG data along to the BSR. Command signals from the TAP controller determine if the JTAG data is captured, and how and when it is clocked out of the BSC.

The first register either captures the internal data sent to the output driver, or provides serially scanned-in data for the output driver. The second register captures the internal output-enable control from the output driver, and also provides serially-scanned output-enable values. The third register captures the input data from the I/O input buffer. Figure 24-7 illustrates a typical BSC and its relationship to the I/O port.

Figure 24-7:   BSC and its Relationship to the I/O Port

24.4.4   JTAG Instructions

dsPIC33F/PIC24H devices support the mandatory instruction set that is specified by IEEE 1149.1, as well as several optional public instructions defined in the IEEE 1149.1 specification. These devices also implement Microchip-specific instructions. Table 24-4 describes the mandatory, optional and Microchip-specific JTAG instructions.

Table 24-4:   JTAG Instructions

JTAG Instruction	Hex Value	Description
Mandatory JTAG Instructions		
BYPASS	0x0F	Bypasses a device in a test chain. In Bypass mode, a single shift register stage provides a minimum length serial path between the TDI and TDO pins.
SAMPLE/PRELOAD	0x01	Takes snapshots of the component's input and output signals without interfering with the normal operation of the assembled board. The snapshot is taken on the rising edge of TCK in the Capture-DR controller state. The data can be viewed by shifting through the component's TDO output.
		This instruction also allows the scanning of the BSR without interfering with normal operation of the on-chip system logic. For example, before the EXTEST instruction is selected, data can be loaded onto the latched parallel outputs using PRELOAD. As soon as the EXTEST instruction is transferred to the parallel output of the Instruction register, the preloaded data is driven through the system output pins. This ensures that known data, consistent at the board level, is driven immediately when the EXTEST instruction is entered. Without PRELOAD, indeterminate data would be driven until the first scan sequence is completed.
EXTEST	0x03	Allows testing of the off-chip circuitry and board level interconnections. Data typically is loaded onto the latched parallel outputs of the Boundary Scan shift register stages, by using the PRELOAD instruction, before the EXTEST instruction is selected. BSR cells at output pins are used to apply test stimuli. BSR cells at input pins are used to capture test results.
Optional JTAG Instructions		
IDCODE	0x02	Selects a 32-bit identification register to be connected for serial access between TDI and TDO in the Shift-DR controller state. This instruction causes the 32-bit device identification word to be shifted out on the TDO pin.
HIGHZ	0x04	Places the component in a state in which all of its system logic outputs are placed in an inactive drive state (for example, high impedance). In this state, an in-circuit test system drives the signals onto the connections normally driven by a component output without damaging the component. In HIGHZ mode, the Bypass register is connected between the TDI and TDO pins in the Shift-DR state.
Microchip-Specific JTAG Instructions		
MCHP_SCAN	0x07	Selects the internal Microchip-specific scan register to be connected for serial access between the TDI and TDO in the Shift-DR controller state.
MCHP_CMD	0x08	Selects 8-bit Microchip Command shift register to be connected for serial access between the TDI and TDO pins in the Shift-DR controller state. This shift register supports up to 256 commands. The following two commands are available for the user; the rest are reserved: • JTAG_MCLR (0x01): Performs a device Master Clear Reset while the JTAG interface is active; functionally equivalent to hardware MCLR. The TAP interface itself is not reset. • JTAG_MUX (0x02): Switches the JTAG interface to ICSP operation. After this command, TDI and TDO assume the PGDx functions (split input and output, respectively) and TCK functions as PGC.

24.4.5   Boundary Scan Testing (BST)

Boundary Scan Testing (BST) is the method of controlling and observing the boundary pins of the JTAG compliant device with user software. BST can be used to test connectivity between devices by daisy-chaining the JTAG compliant devices to form a single scan chain. Several scan chains can exist on a printed circuit board to form multiple scan chains. These multiple scan chains can then be driven simultaneously to test many components in parallel. Scan chains can contain both, JTAG compliant devices and non-JTAG compliant devices.

A key advantage of the BST is that it can be implemented without physical test probes. A 4-wire or 5-wire interface, and an appropriate test platform is required for implementing the BST. Since JTAG boundary scan has been available for many years, many software tools exist for testing scan chains without the need for extensive physical probing. The main drawback to BST is that it can only evaluate digital signals and circuit continuity. It cannot measure input or output voltage levels or currents.

24.4.5.1   RELATED JTAG FILES

To implement BST, all JTAG test tools require a BSDL file. The BSDL file is a subset of the VHSIC Hardware Description Language (VHDL), and is described as part of the IEEE 1149.1 Standard. The device-specific BSDL file describes how the standard is implemented on a device and how it operates. The BSDL file for a specific device includes the following:

• Pinout and package configuration for the particular device
• Physical location of the TAP pins
• Device ID register and the device ID
• Length of the IR
• Supported BST instructions and their binary codes
• Length and structure of the BSR
• BSC definition

Device-specific BSDL files are available from the Microchip web site (www.microchip.com). The name for each BSDL file is the device name and silicon revision. For example, `dsPIC33FJ256GP710.BSD` is the BSDL file for the dsPIC33FJ256GP710 device.

24.4.6   JTAG Device Programming

The JTAG interface can also be used to program the dsPIC33F/PIC24H devices in their user applications. Using the JTAG interface allows users to include a specific test and programming port into their user-assigned applications, with a single 4-pin interface, without imposing the circuit constraints that the ICSP interface may require.

JTAG device programming actually uses the standard ICSP method over the four pins of the TAP interface. When triggered by the appropriate JTAG command sequence, the TDI, TDO and TCK pins assume the functions of the PGDx and PGCx pins. Apart from the pin remapping, ICSP programming over the JTAG interface behaves exactly as it does over the standard ICSP interface.

Because of the added time overhead for switching the TAP interface, JTAG device programming is slightly longer than the standard ICSP programming over the PGCx and PGDx pins. Enhanced ICSP programming is not available with JTAG programming.

Following are the steps required for JTAG device programming:

1.   Shift the `MCHP_CMD` instruction (0x08) into the Instruction Shift register. This instruction selects the 8-bit Microchip Command register to be connected for serial access between the TDI and TDO pins.
2.   Shift the `JTAG_MUX` instruction (0x02) into the Microchip Command register. This instruction switches the JTAG interface to the ICSP operation. This command causes the TDI and TDO pins to assume the PGD functions and the TCK pin to assume the PGC function.

24.5   RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Programming and Diagnostics module are:

Title	Application Note #
No related applications notes at this time.	N/A

> **Note:**   Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33F/PIC24H family of devices.

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24.6   REVISION HISTORY

Revision A (April 2007)

This is the initial released version of the document

Revision B (February 2010)

This revision incorporates the following updates:

- Renamed the Family Reference Manual name from dsPIC33F to dsPIC33F/PIC24H
- All references to dsPIC33F in the document are updated to dsPIC33F/PIC24H
- Figures:
  - Removed Figure 24-6: Device ID Register
- Note:
  - Added a note with information to customers for utilizing family reference manual sections and data sheets as a joint reference (see note above **24.1 "Introduction"**)
- Sections:
  - Removed the following redundant point in **24.2 "In-Circuit Serial Programming™ (ICSP™)"**: Originally introduced for 8-bit PIC16 devices, this method is used for virtually all Microchip microcontrollers
- Tables:
  - Removed the following reference to Figure 24-6: Device ID Register, in Table 24-3:

    The bit format of the dsPIC33F/PIC24H device is shown in Figure 24-3. It consists of an 11-bit manufacturer ID assigned by the IEEE (29h for Microchip Technology), device part number and device revision number

    For example, the JTAG ID for a dsPIC33FJ256GP710 device is:

    Manufacturer ID = 0x29

    Part number = 0XFF

    Silicon revision = A2

    JTAG ID = 0x03FC2053

  - Added the following reference in Table 24-3 (refer to Function column of Device ID Register in the table): Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for more details on Device ID register and JTAG ID register
- Changes to the text and formatting were incorporated throughout the document

Revision C (May 2012)

This revision incorporates the following updates:

- Figures:
  - Renamed V_{DDCORE} to V_{CAP} in Figure 24-1
- Sections:
  - Removed V_{DDCORE} and added V_{CAP} in the note in **24.4.3 "Boundary Scan Register (BSR)"**
- Minor updates to text and formatting were incorporated throughout the document

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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