Silicon Errata and Data Sheet Clarification

PAC1931/2/3/4 devices adhere to the functional specifications outlined in the device data sheet, with the exception of the anomalies described in this document.

The following silicon issues apply to silicon revisions with Product and Revision IDs that match those provided in Table 1-1. These silicon issues are summarized in Table 1-2.

Future revisions of the PAC1931/2/3/4 devices will address the outlined issues.

TABLE 1-1: SILICON REVISION

Part Number	Product ID	Manufacturer ID	Revision ID
PAC1931	58h	5Dh	03h
PAC1932	59h	5Dh	03h
PAC1933	5Ah	5Dh	03h
PAC1934	5Bh	5Dh	03h

Note 1: The Product, Manufacturer and Revision IDs are located in the FDh, FEh and FFh registers, respectively, as detailed in the PAC1931/2/3/4 Data Sheet.

TABLE 1-2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revision
Lower Sample Rates	Lower-Power Modes	1	When switching to a different sample rate than the default of 1,024 sps, a refresh causes the internal clock to wake up and not turn off. This results in higher than expected current in these lower sample rate modes.	03h

Silicon Errata Issues

1. Module: Lower Sample Rates

When the sampling rate of the PAC1931/2/3/4 changes from the default value of 1,024 sps, the device enters a Low-Power state until the next conversion is scheduled. The device then wakes up, performs the conversion, and re-enters the Low-Power state. This approach supports a lower I_{DD} value when lower sample rates are acceptable.

If a refresh is sent when the PAC1931/2/3/4 samples at lower rates, the internal clock activates to move the latest converted data to the I^2C register. The clock usually turns off so the PAC1931/2/3/4 can enter Low-Power mode. However, due to a silicon issue, the internal clock does not turn off. This increases I_{DD} by ~ 285 µA.

Workaround:

The software workaround for this silicon issue is to perform three specific Write commands after sending a refresh when the PAC1931/2/3/4 samples at lower rates:

Write() → Refresh (Send Byte) → Write()

The Write command must be the same as the mode Write. For example:

8 sps Mode:

1. Write to the CTRL register (`01h`) a payload of `C0h`.
2. Refresh (Send byte).
3. Write to the CTRL register (`01h`) a payload of `C0h`.

Performing this Write sequence meets the silicon requirements to deactivate the internal clock and return the current to the expected value when operating in Low-Power mode.

Note: The workaround must be performed any time a refresh is sent when the PAC1931/2/3/4 samples at lower rates.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision A (April 2025)

Initial release of this document. Issued for silicon revision 03h.

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