AN1798

Crystal Selection for Low-Power Secondary Oscillator

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INTRODUCTION

With the increasing development of low-power designs, including battery operated devices, more efforts have been made in designing low-power oscillators. In applications where an RTCC is maintained at all conditions, including Sleep, Deep Sleep and V_{BAT} modes, the current consumption of the secondary oscillator circuit becomes more critical in overall system-level application design. With improvements in secondary oscillator design, the secondary oscillator on Microchip microcontrollers has achieved an oscillator current of 400 nA (typical). This makes it even more critical to select the right crystal to match the low-power secondary oscillator.

This document provides guidelines for crystal selection for the 32 kHz low-power secondary oscillator. This document should not be the sole criteria for crystal selection. It is recommended to get the oscillator characterized by the crystal vendor. The devices below have implemented the specific low-power oscillator discussed in this document:

- PIC24FJ128GA310 Family
- PIC24FJ128GC010 Family
- PIC24FJ128GA/GB204 Family

For devices not listed above, the secondary oscillator design may be different and data provided in this document may not be relevant. For new devices which implement the same secondary oscillator design, this document will be referred to in the device data sheet.

OSCILLATOR PERFORMANCE

The performance of the oscillator is dependent on multiple factors; some of the parameters are covered in this document. Oscillator behavior can be influenced by:

- Layout and PCB Cleaning
- ESR of the Crystal
- Load Capacitance
- Effect of Voltage
- Effect of Temperature

The above parameters can interact with each other, thus making it critical to know the influence of these parameters on oscillator behavior.

The following sections describe how different design elements can affect the 32 kHz oscillator overall performance. When selecting a suitable crystal for use with a Microchip microcontroller, the most important parameters are the loading capacitance and the ESR. The Load Capacitance (C_L) should be 12.5 pF and the ESR range should be 50 kOhm (Typ.)/70 kOhm (Max.). The crystal drive circuitry in the microcontroller is optimized for these specifications. Selecting a lower load capacitance and/or lower ESR may cause crystal start-up or stability issues.

Layout and PCB Cleaning

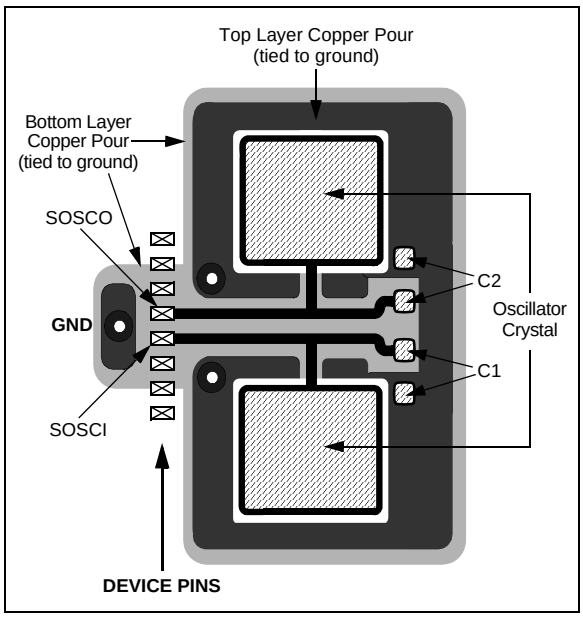
Crystal layout is very critical in design. Due to the low-power operation of the oscillator, it is even more important to provide proper grounding around the crystal. The data sheet for the specific devices describes the details of layout consideration.

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins, with no more than 0.25 inches (6 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 1. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

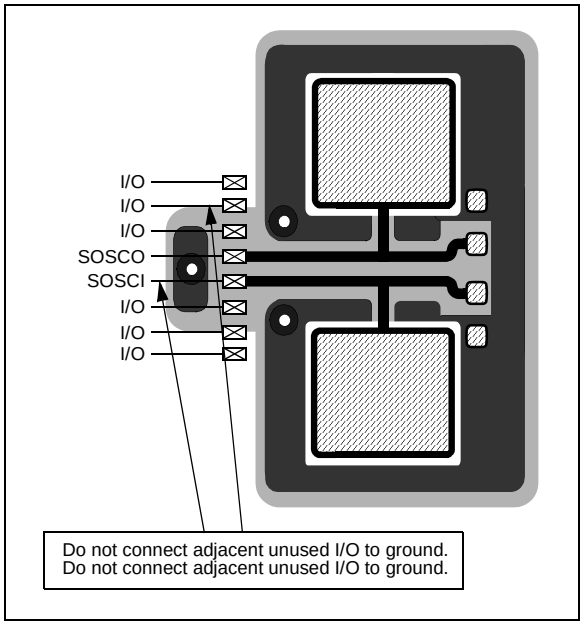
FIGURE 1: FINE-PITCH (DUAL-SIDED) LAYOUTS



While choosing the pinout, avoid the pins adjacent to the SOSC pins for high-frequency switching signals. If there is a choice to leave the adjacent pins not utilized in the application, leave the adjacent pins unused. Do not connect the unused adjacent port pins to ground or V_{DD}.

Once the crystal is soldered to the PC board, it is critical that all flux residue is removed by thoroughly washing the PCB with clean water and drying with hot air. This is especially true when hand-soldering prototype boards. If the board area surrounding the crystal is not cleaned, excess stray capacitance and leakage paths may cause the crystal to be off-frequency or experience other abnormal behavior.

FIGURE 2: UNUSED ADJACENT I/O



ESR of the Crystal

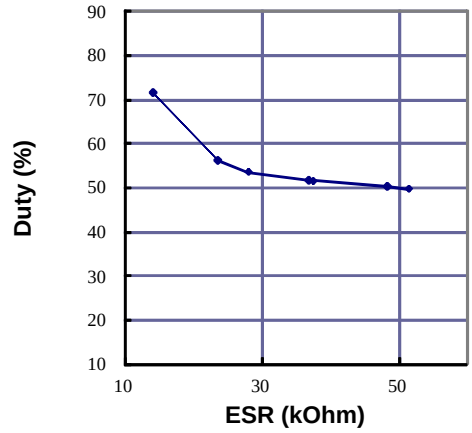
The Equivalent Series Resistor (ESR) is a parameter provided in the crystal data sheet and is the resistance in the crystal during oscillation. The oscillator on the devices mentioned in the **"Introduction"** section has a low-power design with a self-biasing Analog-to-Digital comparator.

When using a crystal with a low-ESR, less than 50 kOhm, the oscillator does not need much energy to drive, which in turn, makes the self-biasing comparator unstable. This results in the comparator producing a 32 kHz digital clock with the duty cycle not being 50%. Variation in the duty cycle is a direct representation of oscillator performance and accuracy.

The desired ESR rating of 50K typical (70K max) will provide an optimum performance across temperature and voltage. Figure 3 shows the plot of the duty cycle of the SOSC digital clock vs. ESR. Temperature, voltage and load capacitance are not varied. The only parameter that is varied is the ESR (from 14K to 51K).

Note:	The duty cycle mentioned in this document refers to the 32 kHz digital clock provided by the secondary oscillator. This can be measured on a REFO pin by configuring the REFO pin for 32 kHz or this can be measured on the RTCC pin by configuring the RTCC module.

FIGURE 3: SOSC DUTY vs. ESR



ESR (kOhm)	SOSC Duty (%)
14.0	71.7
23.5	56.3
27.9	53.6
36.8	51.8
37.4	51.6
48.2	50.3
51.4	49.8

C1,C2 = 22 pF, VDD = 3.3V, Temperature = +25ºC

If the ESR is much higher than the optimal value, it may result in starting problems, as well as slowing down the oscillator start-up, so care should be taken to monitor the duty cycle and select the ESR to achieve an optimum value. The recommended oscillator value for reliable operation is 50K typical and 65K/75K max. There is also a recommended specification for the duty cycle to make sure there are no missing counts. It is recommended that the duty cycle of the SOSC digital clock be within 35%-65% for reliable SOSC operation without any missing counts.

Load Capacitance

The load capacitance is another parameter provided in the crystal data sheet. It is represented as CL and is calculated as follows:

$$C_L = (C_1 \cdot C_2)/(C_1 + C_2) + C_{stray}$$

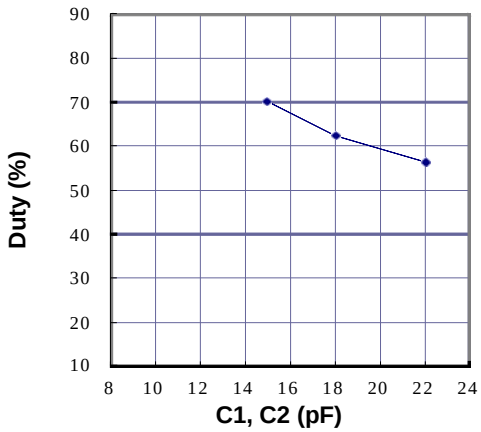
Figure 4 shows the variation of the SOSC duty cycle vs. the loading capacitor, with a constant ESR, VDD and temperature.

Since C1 = C2, then the capacitors are selected by:

$$C1, C2 = (C_L - C_{stray})/2$$

For example, a 32 kHz crystal with a 12.5 pF load capacitance, the recommended values of C1 and C2 are 22 pF ±5%, 50V NP0 (Negative-Positive 0 ppm/°C) ceramic.

FIGURE 4: DUTY vs. CL



C1, C2 (pF)	Duty (%)
22	56.3
18	62.3
15	70.1
12	Not Functional
10	Not Functional

VDD = 3.3V
Temperature = +25°C

The higher the loading capacitor, the better the duty cycle. Therefore, when calculating the CL based on Example 1, always try to use the highest value closest to the calculated loading capacitor.

Using a loading capacitor with too high a value will cause problems, so after selecting the optimum loading capacitor, the SOSC should be characterized across voltage and temperature. Selecting a much higher value than the recommended capacitor may result in the SOSC not starting-up.

EXAMPLE 1: LOADING CAPACITOR CALCULATION

If C_L = 12.5 pF (Load capacitance provided by the vendor):

$$C_L = (C_1 \cdot C_2)/(C_1 + C_2) + C_{stray}$$

Assuming C_{stray} = 2 pF and $C_1 = C_2$:

$C_1 = 2(CL - C_{stray})$

$C_1 = 2(12.5\ pF\text{-}2\ pF)$

$C_1 = 2(10.5\ pF) = 21\ pF$

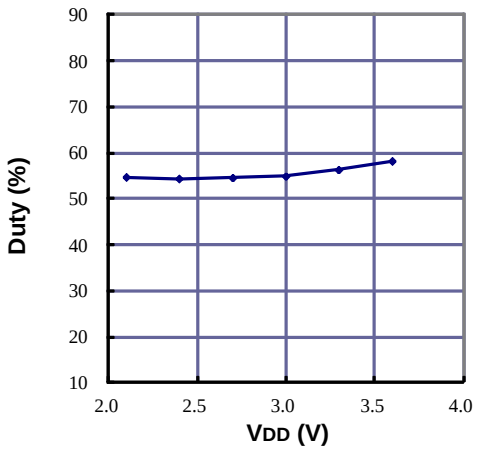
Note 1: In these examples, do not use a loading capacitor below 21 pF. It is recommended to use the next standard ceramic capacitor value of 22 pF.

Effect of Voltage

The VDD at which the device is operated also plays a role in SOSC behavior. The SOSC tends to have a more stable operation at a lower VDD.

There is an internal analog comparator that generates the 32 kHz digital clock. With a lower ESR value, the operation of this comparator will be unstable. This instability is more dominant when the VDD is higher. When the VDD is lower, this internal comparator tends to work in a stable mode.

FIGURE 5: DUTY vs. VDD



VDD (V)	Duty (%)
3.6	58.1
3.3	56.3
3.0	54.9
2.7	54.6
2.4	54.5
2.1	54.6

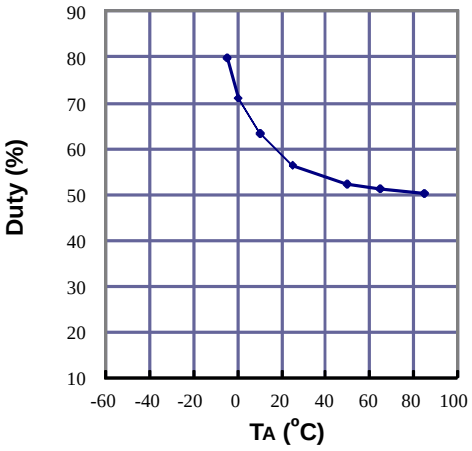
Temperature = +25ºC
ESR = 23.5 kOhm
C1, C2 = 22 pF

Effect of Temperature

The performance of the secondary oscillator is more stable at higher temperatures. With experiments conducted on a low-ESR crystal (ESR of 23.5 kOhm), the oscillator performance is better for higher temperatures (as shown in Figure 6). When the temperature is varied from -40ºC to +85ºC, the best performance is found at +85ºC. Behavior starts deteriorating as the temperature gets closer to -40ºC.

If the ESR of the crystal is increased to 70K ESR, as recommended, the impact of negative temperatures will not have a significant effect on oscillator behavior.

FIGURE 6: DUTY vs. TEMPERATURE



TA (ºC)	Duty (%)
-40	No Output
-10	No Output
-5	79.9(1)
0	71.1(1)
10	63.3
25	56.3
50	52.3
65	51.3
85	50.3

VDD = 3.3V
ESR = 23.5 kOhm
C1,C2 = 22 pF

Note 1: Violates the duty cycle specification of 35% to 65%.

CONCLUSION

The parameters of operating voltage, temperature, loading capacitors, ESR and layout play a role in SOSC behavior. To improve the Secondary Oscillator performance, the following criteria should be met:

- Use the recommended layout as discussed in the Layout and PCB Cleaning section.
- Use a high-ESR (70K max) crystal to provide an optimum performance across temperature and voltage.
- Use a higher loading capacitor (use a crystal of C_L = 12.5) for a better duty cycle.
- A lower V_{DD}, within the V_{DD} operating range, provides reliable performance.
- The higher the temperature, the better the performance of the oscillator.

To provide a guideline for crystal selection, an ESR of 50K typical (65K/70K max) is recommended for an optimum performance across temperature and voltage.

It is recommended to avoid any switching signals adjacent to the SOSC pins to avoid noise due to the low-power SOSC design.

Note: It is strongly recommended to get the oscillator characterized by the crystal vendor.

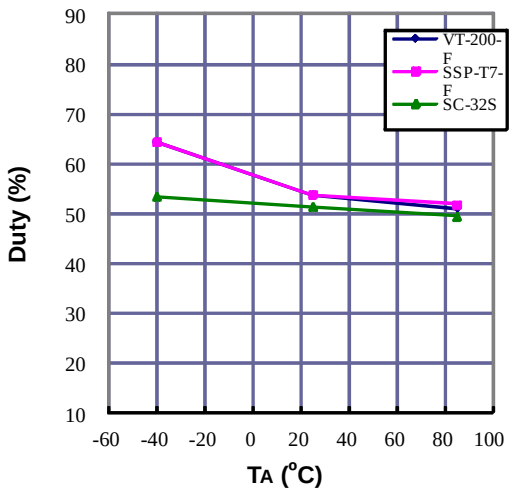
Tests with Seiko Crystals

Further tests were conducted with Seiko crystals to confirm the above mentioned parameters. Three Seiko crystals with different ESRs were used for conducting the tests.

Product	f_num (Hz)	f_tol (x10^{-6})	C_L (pF)	ESR_{MAX} (kOhm)
VT-200-F	32768	±20	12.5	50
SSP-T7-F	32768	±20	12.5	65
SC-32S	32768	±20	12.5	70

Figure 7, Figure 8 and Figure 9 show the test results for the three crystals.

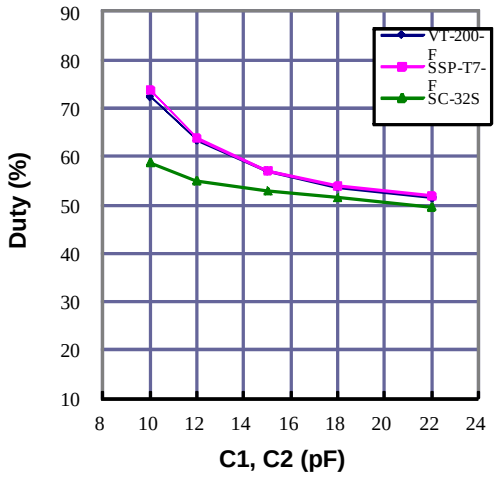
FIGURE 7: DUTY vs. TEMPERATURE



V_{DD} = 3.3V	Duty (%)		
T_A (°C)	VT-200-F	SSP-T7-F	SC-32S
-40	64.4	64.3	53.4
25	53.8	53.9	51.5
85	51.2	51.9	49.5

C1, C2 = 18 pF
V_{DD} = 3.3V

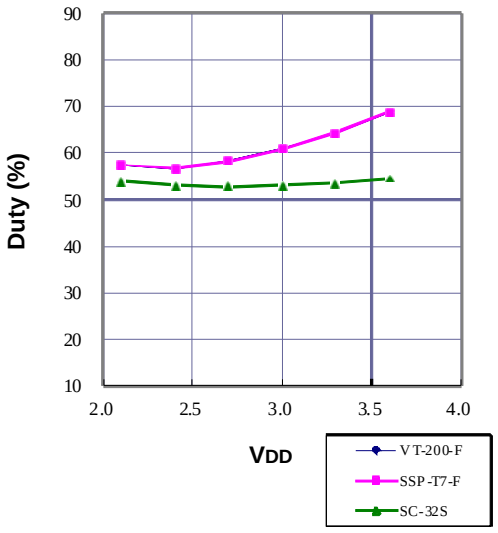
FIGURE 8: DUTY vs. CL



VDD = 3.3V	Duty (%)		
C1, C2 (pF)	VT-200-F	SSP-T7-F	SC-32S
22	51.6	51.8	49.6
18	53.8	53.9	51.5
15	57.1	57.1	52.8
12	63.4	63.8	55.0
10	72.4	73.7	58.8

Temperature = +25ºC
VDD = 3.3V

FIGURE 9: DUTY vs. VDD



-40ºC	Duty (%)		
VDD (V)	VT-200-F	SSP-T7-F	SC-32S
3.6	68.8	68.9	54.5
3.3	64.4	64.3	53.4
3.0	61.0	61.0	53.1
2.7	58.2	58.2	52.9
2.4	56.6	56.6	53.0
2.1	57.5	57.5	54.0

Temperature = -40ºC
VDD = 3.6V

NOTES:

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