

REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		10-15-09

Any assistance, services, comments, information, or suggestions provided by SMSC (including without limitation any comments to the effect that the Company's product designs do not require any changes) (collectively, "SMSC Feedback") are provided solely for the purpose of assisting the Company in the Company's attempt to optimize compatibility of the Company's product designs with certain SMSC products. SMSC does not promise that such compatibility optimization will actually be achieved. Circuit diagrams utilizing SMSC products are included as a means of illustrating typical applications; consequently, complete information sufficient for construction purposes is not necessarily given. Although the information has been checked and is believed to be accurate, no responsibility is assumed for inaccuracies. SMSC reserves the right to make changes to specifications and product descriptions at any time without notice.

DOCUMENT DESCRIPTION
Routing Checklist for the LAN8700, 36-pin QFN Package

 	SMSC 80 Arkay Drive Hauppauge, New York 11788	
	Document Number	Revision
	RC614937	A

Routing Checklist for LAN8700

Information Particular for the 36-pin QFN Package

LAN8700 QFN Phy Interface:

1. The traces connecting the transmit outputs (TXP, pin 29) & (TXN, pin 28) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
2. The traces connecting the receive inputs (RXP, pin 32) & (RXN, pin 31) from the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
3. For differential traces running from the LAN controller to the magnetics, SMSC recommends routing these traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.
4. Refer to Figure No. 1 for differential pair routing details.
5. The VDDA3.3 power supply should be routed as a mini-plane and can be routed on an internal power plane layer.
6. The union of the 10.0 Ω resistor supplying VDDA3.3 to the Transmit Channel center tap of the magnetics and the 0.022 μ F capacitor, should be routed as a mini-plane or with wide traces.
7. Refer to Figure No. 2 for VDDA3.3 power plane details.

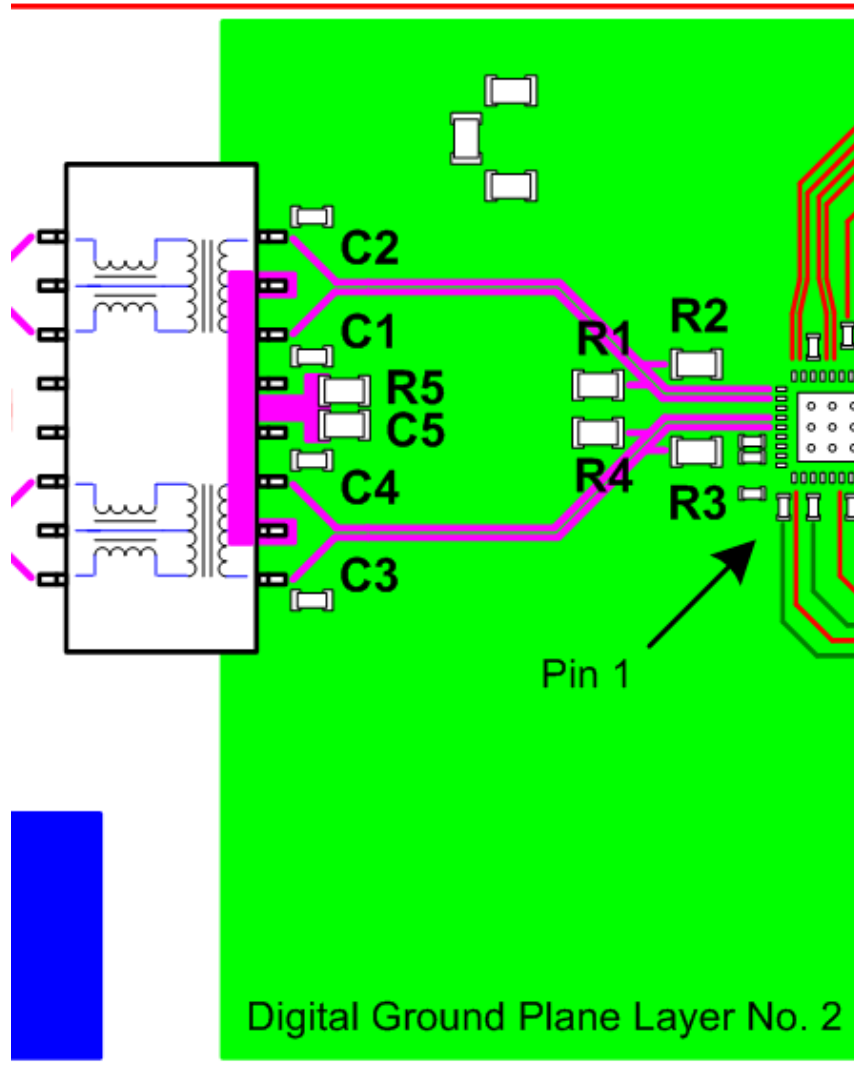


Figure No. 1

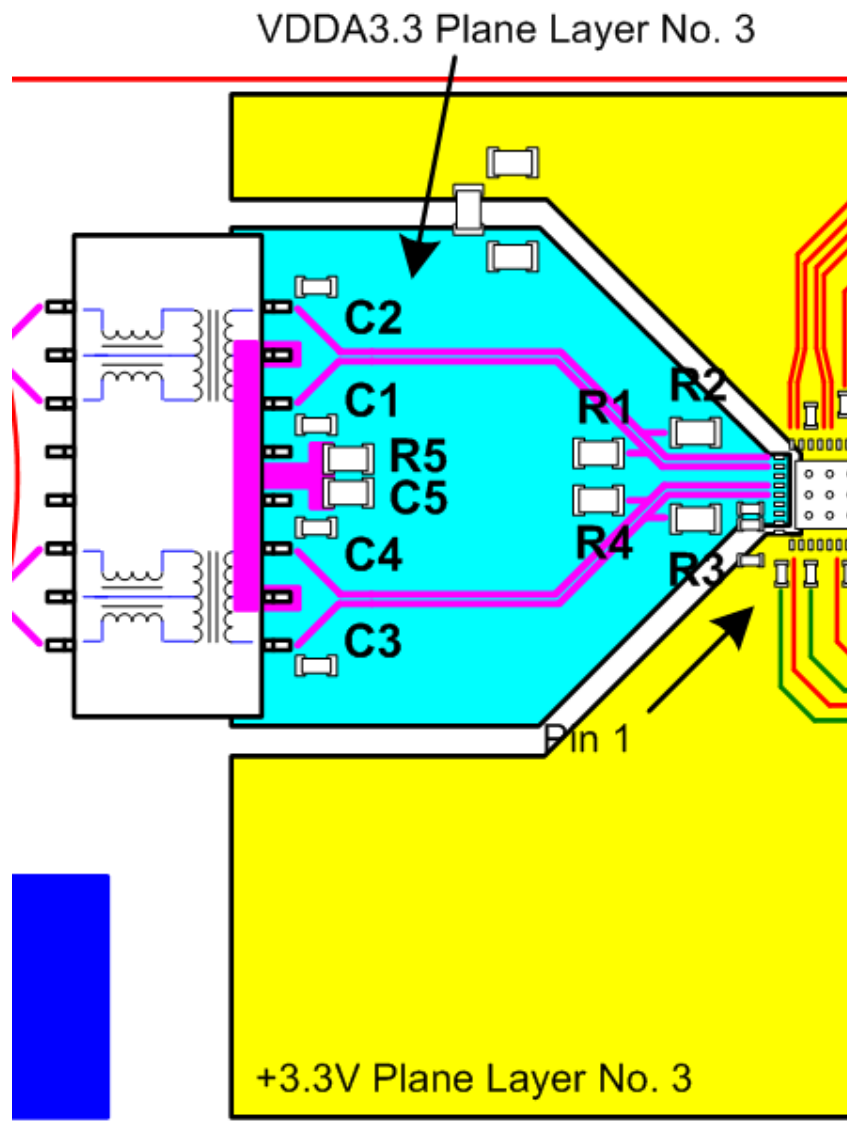


Figure No. 2

LAN8700 QFN Magnetics:

1. The traces connecting the transmit outputs from the magnetics to pins 1 & 2 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.
2. The traces connecting the receive inputs on the magnetics from pins 3 & 6 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.
3. For differential traces running from the magnetics to the RJ45 connector, SMSC recommends routing these traces on the component side of the PCB with all power planes (including chassis ground) cleared out from under these traces. This will minimize the use of vias and minimize any unwanted noise from coupling into the differential pairs. The plane clear out boundary is usually halfway through the magnetics.

RJ45 Connector:

1. Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the LAN chip). Any noise from other traces may couple into the Ethernet section and cause EMC problems.
2. Also recommended, is the construction of a separate chassis ground that can be easily connected to digital ground at one point. This plane provides the lowest impedance path to earth ground.
3. Refer to Figure No. 3 for Ethernet front end routing details.

No Planes or Traces Underneath Two
Differential Pairs in This Area

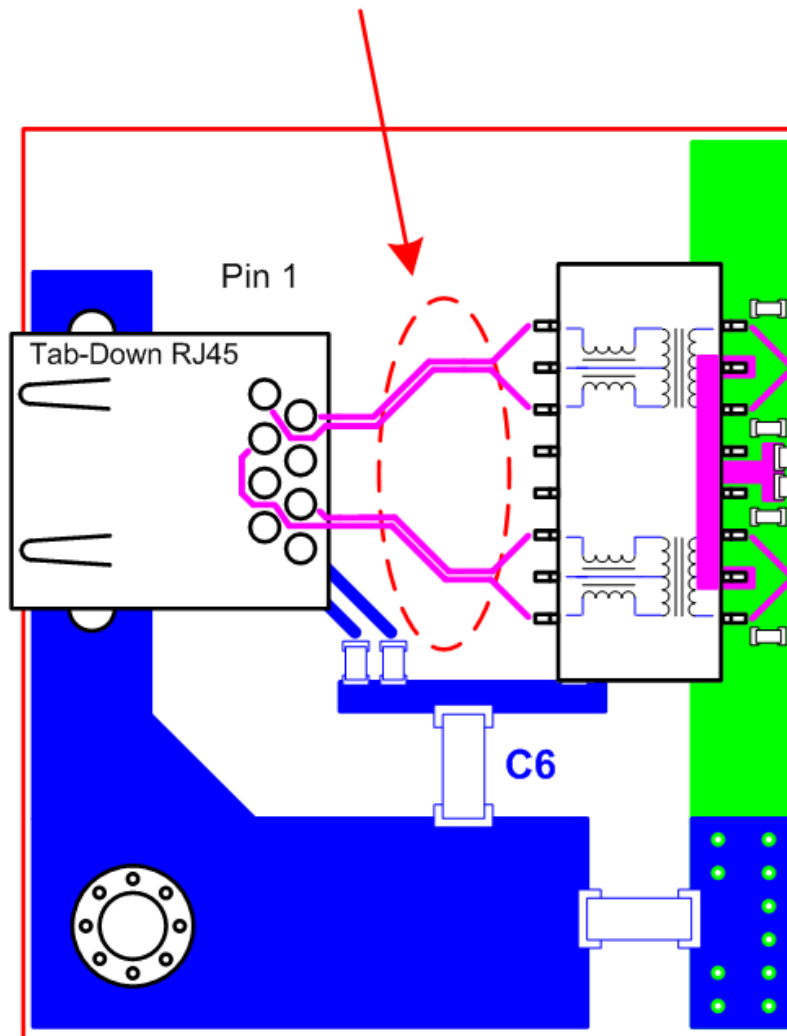


Figure No. 3

Power Supply Connections:

1. Route the (1) VDD33 pin of the LAN8700 QFN directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.
2. In addition, route the (1) VDD33 decoupling capacitor for the LAN8700 QFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for the cap.
3. Route the (3) VDDA3.3 pins of the LAN8700 QFN directly into a solid, +3.3V power plane (created with a ferrite bead). The pin-to-plane trace should be as short as possible and as wide as possible.
4. In addition, route the (3) VDDA3.3 decoupling capacitors for the LAN8700 QFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.
5. Route the (1) VDDIO pin of the LAN8700 QFN directly into a solid, variable voltage (+1.8V to +3.3V) power plane. The pin-to-plane trace should be as short as possible and as wide as possible.
6. In addition, route the (1) VDDIO decoupling capacitor for the LAN8700 power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (power plane & digital ground plane) for the cap.

Ground Connections:

1. The single digital ground pin (pin 37, EDP) on the LAN8700 QFN should be connected directly into a solid, contiguous, internal ground plane. The EDP pad on the component side of the PCB should be connected to the internal digital ground plane with 9 power vias in a 3x3 grid.
2. We recommend that all Ground pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

VDD_CORE:

1. The VDD_CORE pin, pin 8, must be routed with a heavy, wide trace with multiple vias to the single decoupling cap and the single bulk capacitor associated with it. A mini-plane is also acceptable.

Crystal Connections:

1. The routing for the crystal or clock circuitry should be kept as small as possible and as short as possible. Refer to Figure No. 4 below for details.
2. A small ground flood routed under the crystal package on the component layer of PCB may improve the emissions signature. Stitch the flood with multiple vias into the digital ground plane directly below it.

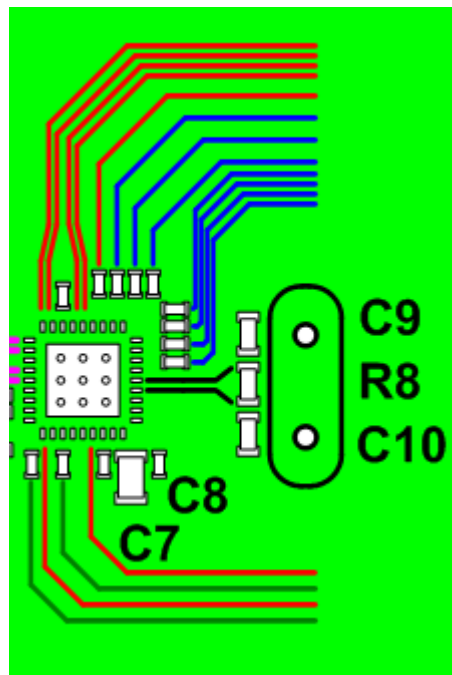


Figure No. 4

Clock Oscillator Connections:

1. When using the LAN8700 in RMII mode, place the 50 MHz clock oscillator approximately half-way between the LAN8700 and the RMII MAC in the application. This should ensure relatively matched clock runs to each.
2. Place any series terminations for splitting the 50 MHz clock as close as possible to the clock oscillator in the design.
3. As controlled by the different component placements, the two resultant clock traces should be matched to within 0.10" and have an overall trace length of less than 6.0".

EXRES1 Resistor:

1. The EXRES1 resistor (pin 34) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the EXRES1 resistor.

MII Interface:

1. The MII interface on the LAN8700 should be constructed using 68-ohm traces.
2. Similar groups of the MII interface should be routed together on the PCB. Transmit channel signals should be routed together and separate from Receive channel signals.
3. RX_CLK and TX_CLK signals should be given sufficient spacing from all other MII signals.
4. MII signals considered critical should be routed on the top layer next to a contiguous, digital ground plane. Slower MII signals can be routed on the bottom layer of the PCB.
5. As with any high-speed digital design, inter-space and intra-space guidelines between MII signals should help to improve crosstalk and signal integrity issues.
6. Refer to Figures No. 5 and No. 6 for details on MII signal routing.

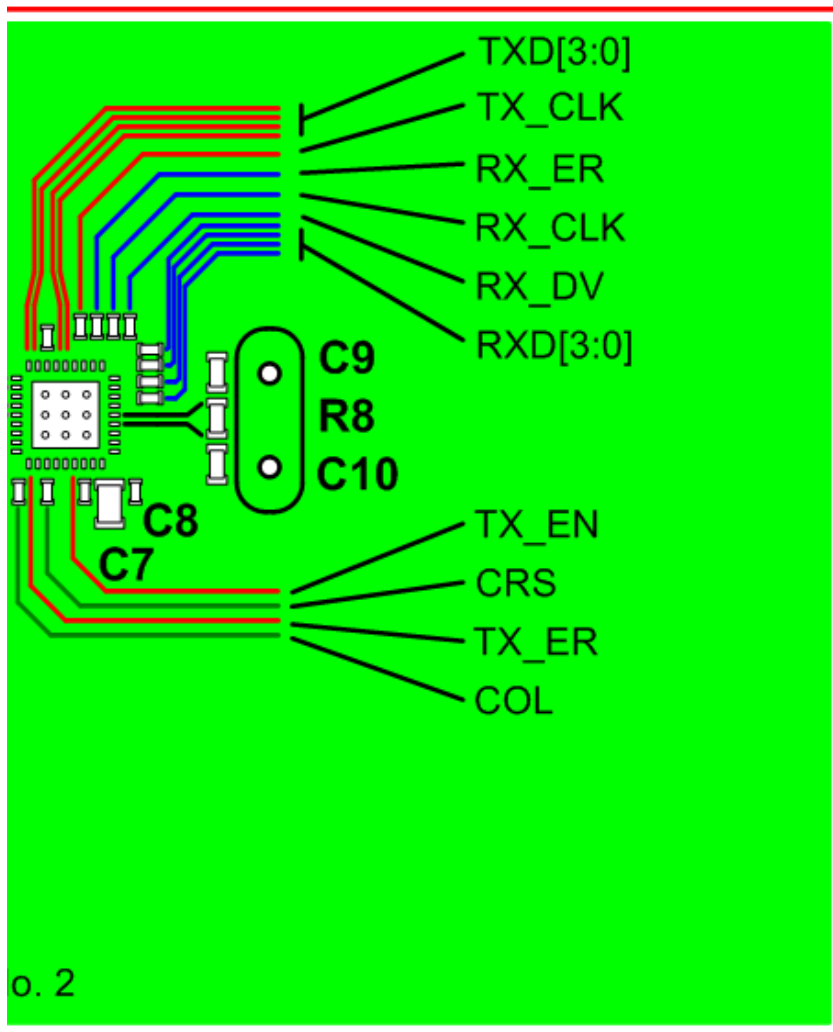


Figure No. 5

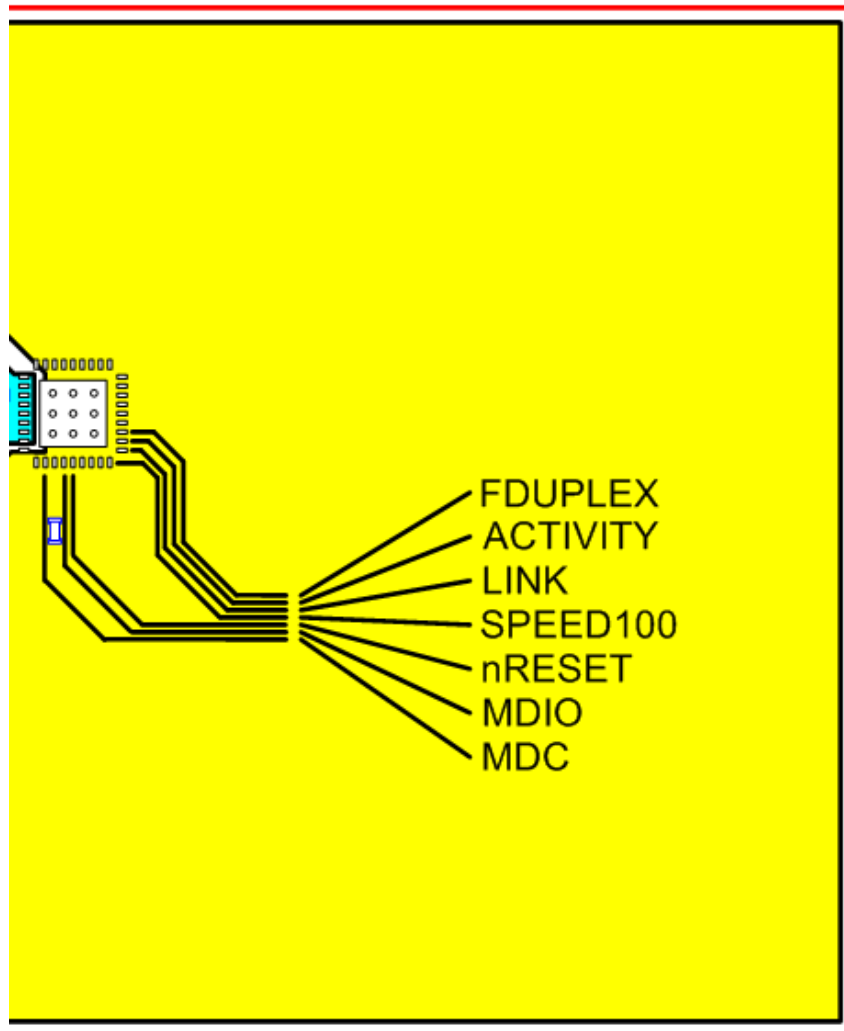


Figure No. 6

RMII Interface:

1. The RMII interface on the LAN8700 should be constructed using 68-ohm traces.
2. Similar design guidelines as per the MII signals should be followed for the RMII signals.

MII/RMII Series Terminations:

1. If the designer has elected to use impedance matching terminations in his design, these series resistors should be placed as close as possible to the source of the driving signal.
2. The MII/RMII Series Terminations should be considered critical components. To ensure the best signal integrity and good EMI performance, these critical components should be placed on the component side of the PCB. This will ensure that these components will be referenced to a contiguous ground plane reference on Layer 2 of the design. This will also minimize the use of vias in routing these signals.

Required External Pull-ups:

1. There are no critical routing instructions for the Required External Pull-up connections.

Mode Pins:

1. Since the MODE Pins are shared with the RXD[2..0] signals of the LAN8700, any resistor used for termination for the power-on-reset MODE selection, should be placed on the component side of the PCB. This will minimize vias and ensure the reference plane remains constant.
2. Any stub added to the MII lines due to MODE pin terminations should be kept to a minimum.

Phy Address Pins:

1. Phy Address pin PHYAD4 should be considered critical. This pin is shared with the CRS function of the MII interface. Any resistor used for termination for the power-on-reset Phy Address selection, should be placed on the component side of the PCB. This will minimize vias and ensure the reference plane remains constant for the CRS signal.
2. Any stub added to the MII lines due to PHYAD4 terminations should be kept to a minimum.

LED Pins:

1. There are no critical routing instructions for the LED Pin connections.

Interrupt Functionality:

1. There are no critical routing instructions for the Interrupt connection.

Miscellaneous:

1. SMSC recommends utilizing at least a four-layer design for boards for the LAN8700 QFN device. The design engineer should be aware, however, as tighter EMC standards are applied to his product and as faster signal rates are utilized by his design, the product design may benefit by utilizing up to eight layers for the PCB construction.
2. As with any high-speed design, the use of series resistors and AC terminations is very application dependant. Buffer impedances should be anticipated and series resistors added to ensure that the board impedance matches the driver. Any critical clock lines should be evaluated for the need for AC terminations. Prototype validation will confirm the optimum value for any series and/or AC terminations.
3. Bulk capacitors for each power plane should be routed immediately into power planes with traces as short as possible and as wide as possible.
4. Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.
5. Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, etc.). The electrical engineer needs to work with the PCB designer to determine all these variables.

No Planes or Traces Underneath Two
Differential Pairs in This Area

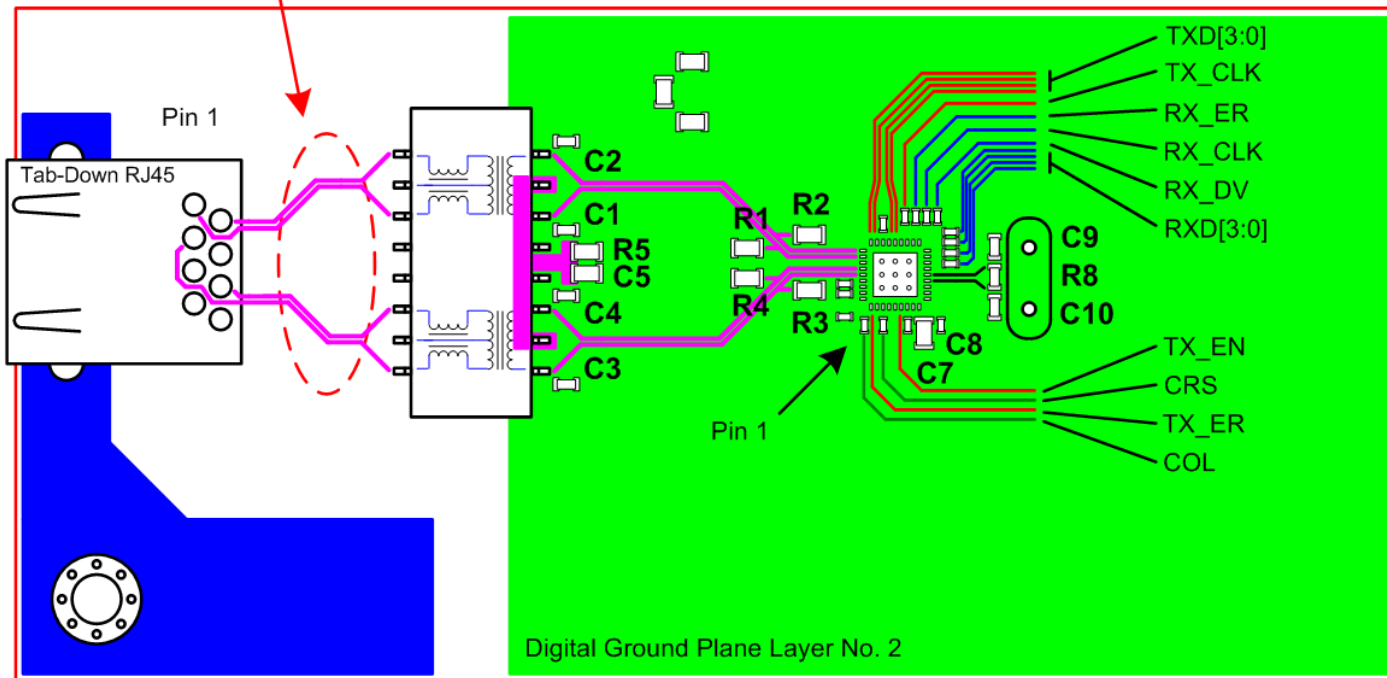


Figure No. 7

No Planes or Traces Underneath Two
Differential Pairs in This Area

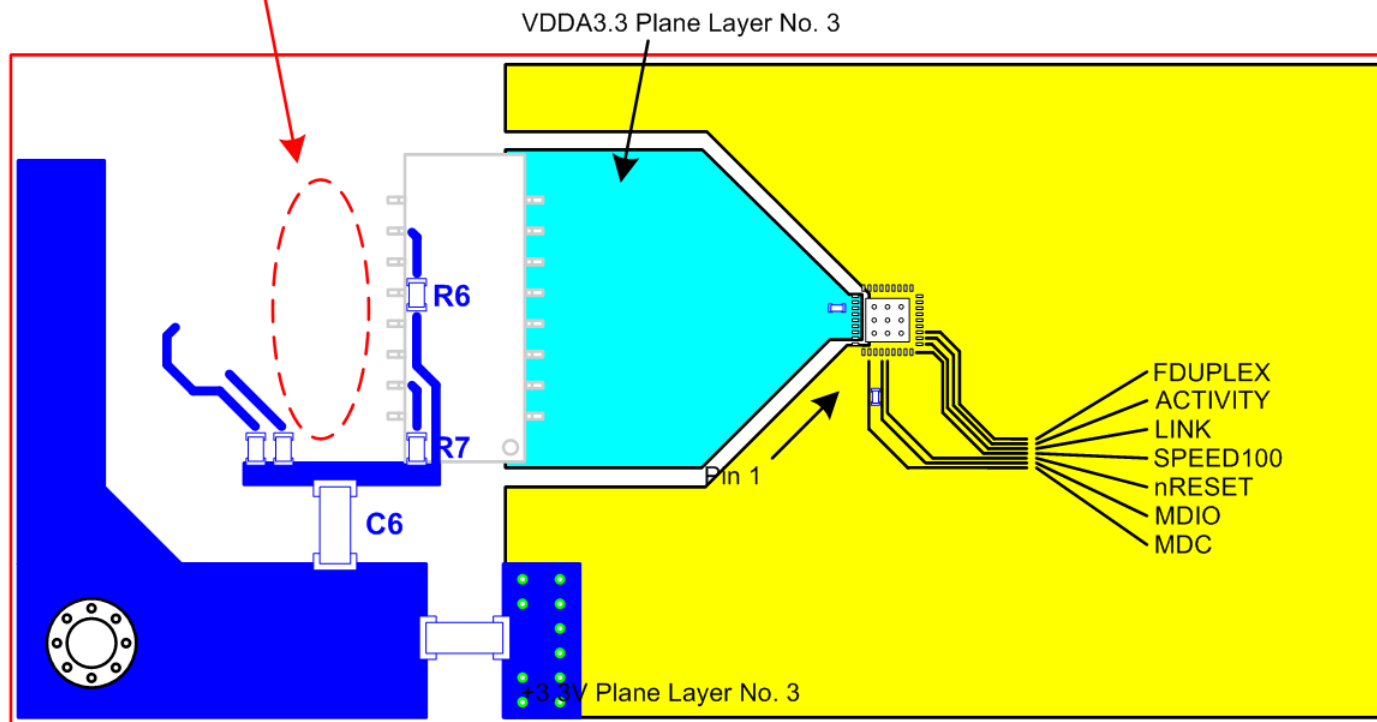


Figure No. 8