LAN7431

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip LAN7431. These checklist items should be followed when utilizing the LAN7431 in a new design. A summary of these items is provided in Section 7.0, "Hardware Checklist Summary," on page 11. Detailed information on these subjects can be found in the corresponding section:

2.0 GENERAL CONSIDERATIONS

2.1 Pin Check

Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs or bidirectional for error checking.

2.2 Ground

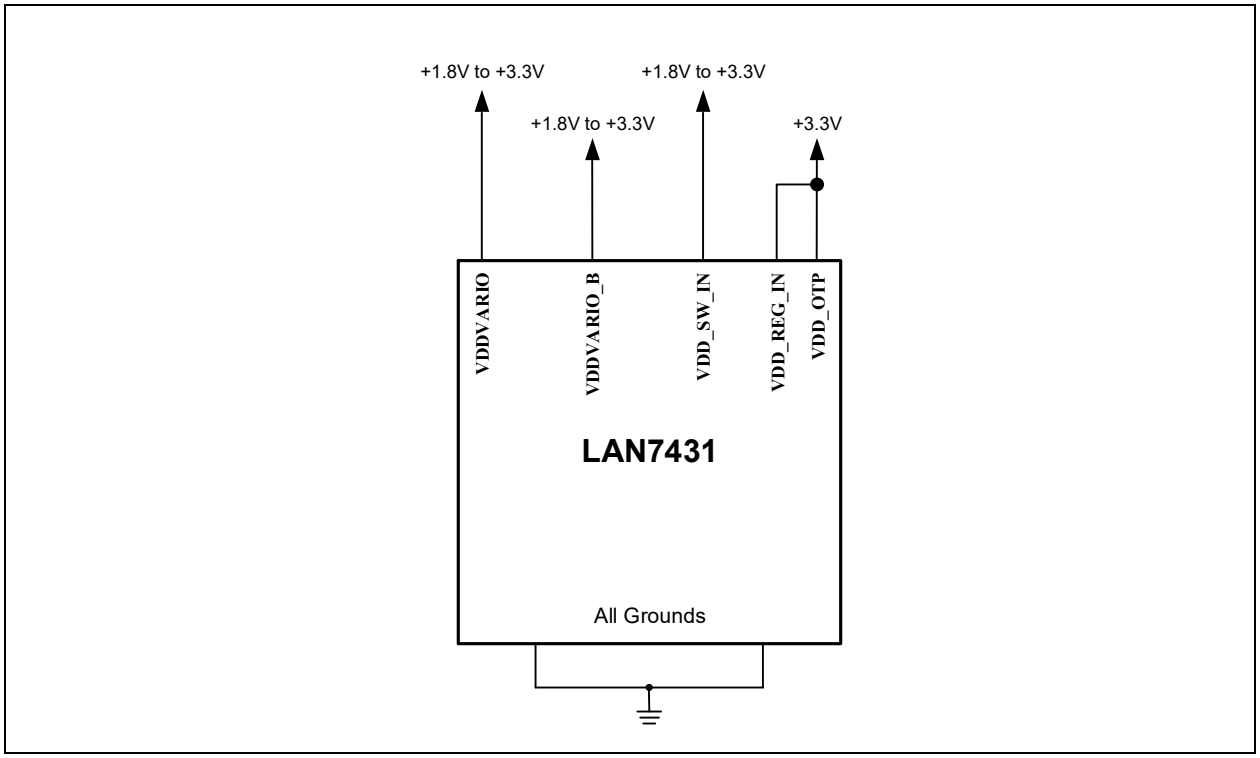
- All grounds, digital ground pins (**GND**), core ground pins (**GND_CORE**), and analog ground pins (**VSS_A**) on the LAN7431, are all connected internally to the exposed die paddle ground (**VSS**). The exposed die paddle (EDP) ground pad on the underside of the LAN7431 must be connected directly to a solid, contiguous digital ground plane.
- Connect pins **GD_1**, **GD_2**, and **GD_3** (pins 26, 29, and 33) directly to the same digital ground plane as the EDP pad.
- On the PCB, one digital ground is recommended. Running separate ground planes for any of Microchip LAN products is not recommended.

3.0 POWER

3.1 +3.3V Power Supply Connections

- The supply (**VDD_OTP**) pin on the LAN7431 is pin 65. This pin requires a connection to +3.3V. This pin is the +3.3V power supply for the one-time programmable (OTP) charge pump.
- The **VDD_OTP** pin should also have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.
- The supply (**VDD_REG_IN**) pin for the +2.5V LDO regulator in the LAN7431 is pin 39. This pin requires a connection to +3.3V.
- The **VDD_REG_IN** pin should also have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.
- The supply (**VDD_SW_IN**) pin for the +1.2V switching regulator in the LAN7431 is pin 52. This pin requires a connection to +1.8V to +3.3V.
- The **VDD_SW_IN** pin should also have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.

FIGURE 3-1: +3.3V POWER SUPPLY CONNECTIONS



3.2 VDDVARIO Power Supply Connections

- The **VDDVARIO** supply pin on the LAN7431 are pins 43, 48, and 61. These pins require a connection to +1.8V to +3.3V.
- Each **VDDVARIO** pin should also have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.

3.3 VDDVARIO_B Power Supply Connections

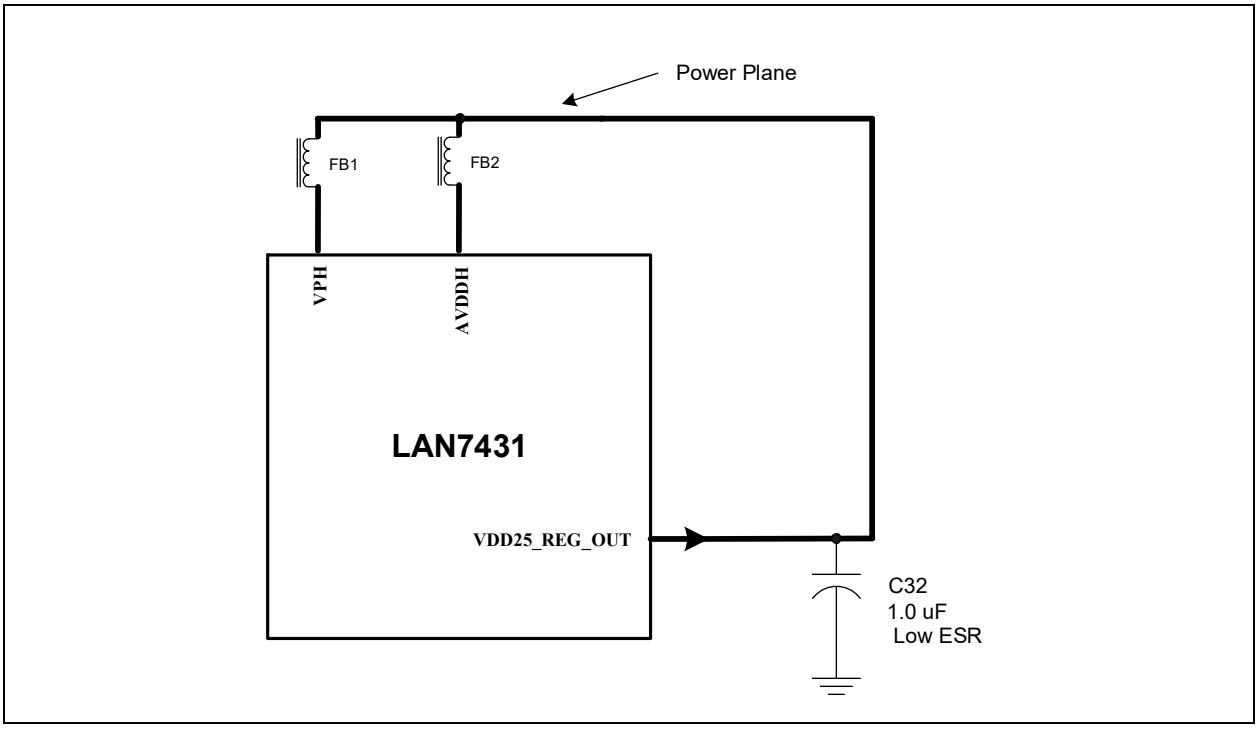
- The **VDDVARIO_B** supply pin on LAN7431 are pins 3, 7, 12, and 19. These pins require a connection to +1.8V to +3.3V.
- Each **VDDVARIO_B** pin should also have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.

3.4 +2.5V Power Supply Connections

- **VDD25_REG_OUT** (pin 38) is the output pin of the internal +2.5V LDO regulator for the LAN7431.
- The **VDD25_REG_OUT** pin should have one 0.01 µF (or smaller) capacitor to bypass the LAN7431. The capacitor size should be SMD_0603 or smaller.
- The **VDD25_REG_OUT** pin also requires a 1.0 µF, low equivalent series resistance (ESR) capacitor. The low ESR requirement ensures the proper stability of the +2.5V internal regulator of the LAN7431. High-quality, low-ESR, ceramic-type capacitor for this particular application is recommended. ESR not higher than 2.0Ω for frequency ranges from 10 KHz to 1 GHz is also recommended.
- The **AVDDH** (pin 1) pin supplies power to the bandgap reference, and the crystal oscillator amplifier of the LAN7431. This pin should be powered from pin 38 (**VDD25_REG_OUT**) through a suitable ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. Optionally, this pin can also be supplied from an external +3.3V power supply.

- The **AVDDH** pin should have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.
- The **VPH** (pin 34) supplies power to the PCIe PHY of the LAN7431. This pin should be powered from pin 38 (**VDD25_REG_OUT**) through a suitable ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.
- The **VPH** pin should have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.

FIGURE 3-2: LAN7431 +2.5V POWER CONNECTIONS

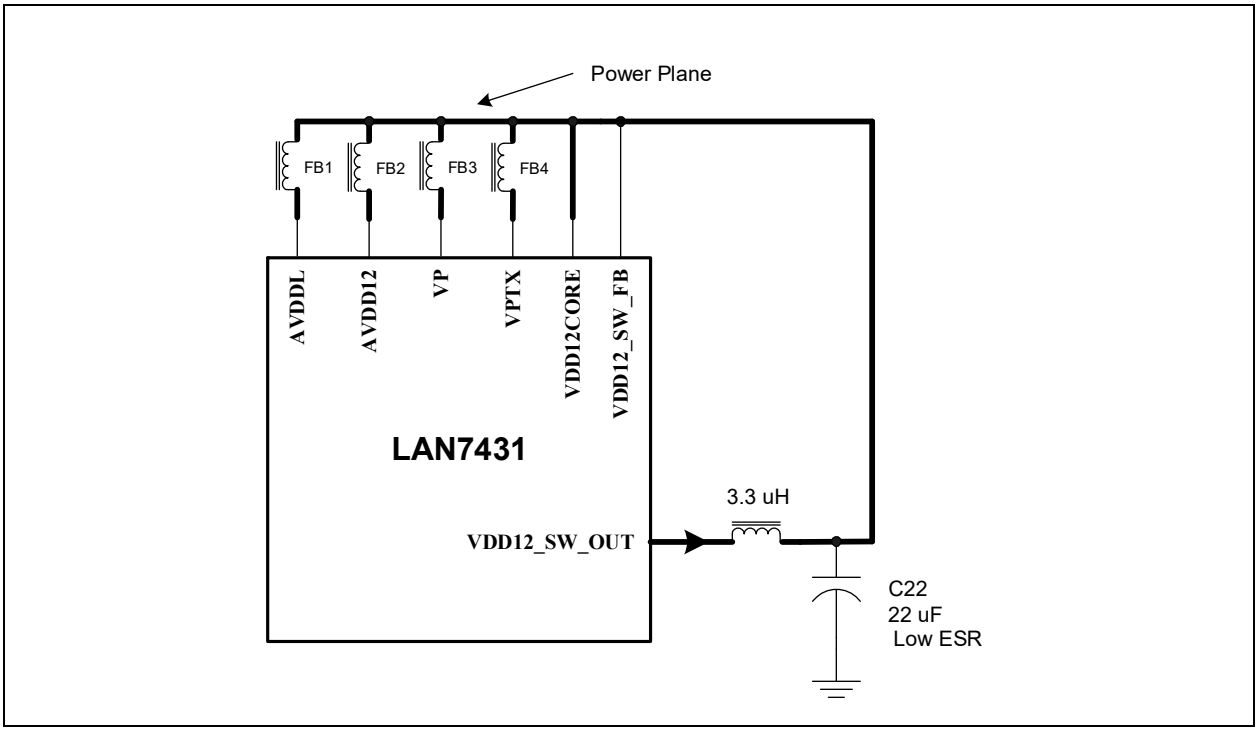


3.5 +1.2V Power Supply Connections

- The **VDD12_SW_OUT** (pin 51) pin is the output pin of the internal +1.2V switching regulator for the LAN7431. This pin must be connected directly to a series 3.3 uH inductor.
- The **VDD12_SW_OUT** pin/3.3 uH inductor node in the design should have one 0.1 µF (or smaller) capacitor to bypass the LAN7431. The capacitor size should be SMD_0603 or smaller.
- The **VDD12_SW_OUT** pin/3.3 uH inductor node also requires a 22 µF, low-ESR capacitor. The low ESR requirement ensures the proper stability of the +1.2V internal regulator of the LAN7431. High-quality, low-ESR, ceramic-type capacitor for this particular application is recommended. ESR not higher than 2.0Ω for frequency ranges from 10 KHz to 1 GHz is also recommended.
- The **VDD12_SW_FB** (pin 53) pin supplies feedback for the internal +1.2V switching regulator. In this application, this pin should be connected directly to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7431. For applications where the +1.2V internal switching regulator is disabled, connect **VDD12_SW_FB** directly to **VDD_SW_IN** (pin 52).
- The **VDD12_SW_FB** pin should have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.
- The **VDD12CORE** (pins 24, 46, and 62) core input power supply pins may be powered from the internal +1.2V switching regulator. In this application, these three pins should be connected directly to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7431. See Figure 3-3 for more details. These three pins can also be supplied from an external +1.2V power supply. In this application, the internal +1.2V switching regulator can be disabled.

- The **VDD12CORE** pins should each have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.
- The **AVDDL** (pin 2) pin supplies power to the analog core of the LAN7431 from the internal +1.2V switching regulator through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. In this application, the ferrite bead should be connected to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7431. See Figure 3-3 for more details. This pin can also be supplied from an external +1.2V power supply. In this application, the internal +1.2V switching regulator can be disabled.
- The **AVDDL** pin should have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.
- The **AVDD12** (pin 69) pin supplies power to the PLL/DLL of the LAN7431 from the internal +1.2V switching regulator through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. In this application, the ferrite bead should be connected to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7431. See Figure 3-3 for more details. This pin can also be supplied from an external +1.2V power supply. In this application, the internal +1.2V switching regulator can be disabled.
- The **AVDD12** pin should have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.
- The **VP** (pin 25) pin supplies power to the PCIe PHY of the LAN7431 from the internal +1.2V switching regulator through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. In this application, the ferrite bead should be connected to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7431. See Figure 3-3 for more details. This pin can also be supplied from an external +1.2V power supply. In this application, the internal +1.2V switching regulator can be disabled.
- The **VP** pin should have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.
- The **VPTX** (pin 31) pin supplies power to the PCIe PHY transmitter of the LAN7431 from the internal +1.2V switching regulator through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. In this application, the ferrite bead should be connected to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7431. See Figure 3-3 for more details. This pin can also be supplied from an external +1.2V power supply. In this application, the internal +1.2V switching regulator can be disabled.
- The **VPTX** pin should have one 0.01 µF (or smaller) capacitor to decouple the LAN7431. The capacitor size should be SMD_0603 or smaller.

FIGURE 3-3: LAN7431 +1.2V POWER CONNECTIONS



4.0 CLOCK CIRCUIT

- A 25.000 MHz crystal must be used with the LAN7431. For exact specifications and tolerances, refer to the latest revision *LAN7431 Data Sheet*.
- **XI** (pin 71) on the LAN7431 is the clock circuit input. This pin requires a 15 to 33 pF capacitor to the digital ground. One side of the crystal connects to this pin.
- **XO** (pin 70) on the LAN7431 is the clock circuit output. This pin requires a matching 15 to 33 pF capacitor to ground and the other side of the crystal.
- Since every system design is unique, the capacitor values are system-dependent. The PCB design, the crystal selected, the layout, and the type of capacitors selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability, and the voltage level of the circuit to guarantee that the circuit meets all design criteria as presented in the data sheet.
- For proper operation, the additional 1.0 MΩ external resistor across the crystal is no longer required. The necessary resistance has been designed internally on the LAN7431.

5.0 DIGITAL INTERFACES

5.1 RGMII Interface

- Table 5-1 indicates the proper connections for the 14 RGMII signals.

TABLE 5-1: RGMII SIGNALS

From	Connects to	
LAN7431	**RGMII Phy Device**	**Notes**
RXD0 (pin 15)	RXD<0>	
RXD1 (pin 16)	RXD<1>	
RXD2 (pin 17)	RXD<2>	
RXD3 (pin 18)	RXD<3>	
RXD4	*RXD<4>*	*Not used in RGMII mode*
RXD5	*RXD<5>*	*Not used in RGMII mode*
RXD6	*RXD<6>*	*Not used in RGMII mode*
RXD7	*RXD<7>*	*Not used in RGMII mode*
RX_CTL (pin 14)	RXCTRL	
RX_DV	*RX_DV*	*Not used in RGMII mode*
RX_ER	*RX_ER*	*Not used in RGMII mode*
RXC (pin 13)	RX_CLK	
TX_ER	*TX_ER*	*Not used in RGMII mode*
TXD0 (pin 8)	TXD<0>	
TXD1 (pin 6)	TXD<1>	
TXD2 (pin 5)	TXD<2>	
TXD3 (pin 4)	TXD<3>	
TXD4	*TXD<4>*	*Not used in RGMII mode*
TXD5	*TXD<5>*	*Not used in RGMII mode*
TXD6	*TXD<6>*	*Not used in RGMII mode*
TXD7	*TXD<7>*	*Not used in RGMII mode*
TX_CTL (pin 10)	TXCTRL	
TX_EN	*TX_EN*	*Not used in RGMII mode*
TXC (pin 11)	TX_CLK	
GTXCLK	*GTX_CLK*	*Not used in RGMII mode*
CRS	*CRS*	*Not used in RGMII mode*
COL	*COL*	*Not used in RGMII mode*
MDIO (pin 63)	MDIO	
MDC (pin 64)	MDC	

- Provisions should be made for series terminations for all outputs on the RGMII interface. Series resistors enable the designer to closely match the output driver impedance of the LAN7431 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors might be 10.0Ω.
- The **REFCLK_25** (pin 21) output pin of the LAN7431 can be used as a reference clock to the external Gigabit Ethernet PHY. This must be enabled (set) in the HARDWARE CONFIGURATION REGISTER (HW_CFG).
- An external 125 MHz clock can be supplied to the **CLK125** (pin 20) input pin of the LAN7431 to generate the internal RGMII TX clock. If this pin is not used, it should be tied low with a 10 KΩ pull-down. In this case, if the 125 MHz is not supplied, the LAN7431 can generate its own 125 MHz internally. This functionality must be enabled (set) in the HARDWARE CONFIGURATION REGISTER (HW_CFG).
- The **DUPLEX** (pin 40) input pin of the LAN7431 connects to the Duplex Mode output pin from the external PHY.

When asserted, the partner PHY is in Full Duplex mode. If the partner PHY does not have a duplex output signal, then it is recommended that this signal be tied to VDD to force full duplex operation.

- The **PHY_INT_N** (pin 41) input pin of the LAN7431 can be used to indicate an interrupt from the external Gigabit PHY.
- The **PHY_RESET_N** (pin 42) output pin of the LAN7431 can be used to reset the external Gigabit PHY.

5.2 MII Interface

- When utilizing either an external MII PHY or an MII connector, Table 5-2 indicates the proper connections for the 18 signals.

TABLE 5-2: MII SIGNALS

From	Connects to	
LAN7431	**MII Physical Device**	**MII Connector**
RXD0 (pin 15)	RXD<0>	RXD<0> (contact 7)
RXD1 (pin 16)	RXD<1>	RXD<1> (contact 6)
RXD2 (pin 17)	RXD<2>	RXD<2> (contact 5)
RXD3 (pin 18)	RXD<3>	RXD<3> (contact 4)
RX_DV (pin 14)	RX_DV	RX_DV (contact 8)
RX_ER (pin 20)	RX_ER	RX_ER (contact 10)
RX_CLK (pin 13)	RX_CLK	RX_CLK (contact 9)
TX_ER (pin 9)	TX_ER	TX_ER (contact 11)
TXD0 (pin 8)	TXD<0>	TXD<0> (contact 14)
TXD1 (pin 6)	TXD<1>	TXD<1> (contact 15)
TXD2 (pin 5)	TXD<2>	TXD<2> (contact 16)
TXD3 (pin 4)	TXD<3>	TXD<3> (contact 17)
TX_EN (pin 10)	TX_EN	TX_EN (contact 13)
TX_CLK (pin 11)	TX_CLK	TX_CLK (contact 12)
CRS (pin 23)	CRS	CRS (contact 19)
COL (pin 22)	COL	COL (contact 18)
MDIO (pin 63)	MDIO	MDIO (contact 2)
MDC (pin 64)	MDC	MDC (contact 3)

5.3 EEPROM Interface

- **EECS** (pin 60) on the LAN7431 connects to the external EEPROM's chip select (CS) pin.
- **EECLK** (pin 58) on the LAN7431 connects to the external EEPROM's serial clock pin.
- **EEDIO** (pin 59) on the LAN7431 connects to the external EEPROM's Data Out pin through an external series resistor, and connects directly to the external EEPROM's Data In pin.
- Be sure to select a 3-wire style 2K/4K EEPROM that is organized for 256/512 x 8-bit operation.
- Be sure to select an EEPROM with an operational voltage that matches the VDDVARIO voltage level of your design.

5.4 PCIe Interface

- The **PCIE_TX_P** (pin 30) pin is the PCIe (v 3.1) Serial Data Output positive data pin. This is the serial differential output link running at 2.5 GT/s. A series capacitor in the range of 0.1 to 0.2 µF (DC blocking capacitor) is required here.
- The **PCIE_TX_M** (pin 32) pin is the PCIe (v 3.1) Serial Data Output negative data pin. This is the serial differential output link running at 2.5 GT/s. A series capacitor in the range of 0.1 to 0.2 µF (DC blocking capacitor) is required here.
- For the DC blocking capacitors, SMD_0402 capacitors are recommended (no larger).

- The **PCIE_RX_P** (pin 27) pin is the PCIe (v 3.1) Serial Data Input positive data pin. This is the serial differential output link running at 2.5 GT/s.
- The **PCIE_RX_M** (pin 28) pin is the PCIe (v 3.1) Serial Data Input negative data pin. This is the serial differential output link running at 2.5 GT/s.
- For PCIe interconnections, the receiver pins have Auto-Polarity correction, by specification. This allows the pairs to be swapped to facilitate board layout concerns. This allows **PCIE_TX_P** to be swapped with **PCIE_TX_M** or **PCIE_RX_P** to be swapped with **PCIE_RX_M**.
- For board applications where the PCIe link is between two devices intra-board, the PCIE_TX and PCIE_RX channels must be crossed over. Two DC blocking capacitors (0.1 µF) should be placed as close as possible to PCIE_TX pins on the LAN7431 device. Two more DC blocking caps should be placed on the transmit pins of the other PCIE device.
- The **PCIE_CLK_P** (pin 36) pin is the differential reference clock in positive signal. This input receives a 100 MHz differential clock input signal.
- The **PCIE_CLK_M** (pin 37) pin is the differential reference clock in negative signal. This input receives a 100 MHz differential clock input signal.
- The **PERST#** (pin 68), which is the active-low input to the LAN7431, indicates that both PCIe power and clock are available.

6.0 MISCELLANEOUS

6.1 ISET Resistor

ISET (pin 72) on the LAN7431 should connect to digital ground through a 6.04 KΩ resistor with a tolerance of 1.0%. This pin is used to set up critical bias currents for the embedded 10/100 Ethernet Physical device.

6.2 RESREF Resistor

RESREF (pin 35) on the LAN7431 should connect to digital ground through a 200Ω resistor with a tolerance of 1.0%, 100 ppm per C.

6.3 Required External Pull-Ups/Pull-Downs

- When using either the RGMII or the MII of the LAN7431 with a PHY device on board, a pull-up resistor on the MDIO signal (pin 63) is required. A pull-up resistor of 1.5 KΩ to VDDVARIO is required for this application.
- The following pins would require a pull-up resistor if the pin is programmed as an Open Drain Output; reference to VDDVARIO power rail:
  - **GPIO0** (pin 60)
  - **GPIO1** (pin 59)
  - **GPIO2** (pin 58)
  - **GPIO3** (pin 57)
  - **GPIO4** (pin 56)
  - **GPIO5** (pin 55)
  - **GPIO6** (pin 54)
  - **GPIO7** (pin 50)
  - **GPIO8** (pin 49)
  - **GPIO9** (pin 47)
- The following pins would require a pull-up resistor if the pin is programmed as an Open Drain Output; reference to VDDVARIO_B power rail:
  - **GPIO10** (pin 22)
  - **GPIO11** (pin 21)
- The following pins require a pull-up resistor as these pins are Open Drain Outputs; reference to VDDVARIO power rail:
  - **WAKE#** (pin 67)
  - **CLKREQ#** (pin 66)

6.4 Other Considerations

- The **RESET_N** (pin 44) pin, when driven low, causes a hardware reset. Assertion of **RESET_N** is not required at power-on. However, if used, **RESET_N** must be driven low for a minimum period as defined in the data sheet. The **RESET_N** pin is pulled-high internally but must be connected externally to VDDVARIO if unused.
  For a more robust LAN7431 design, a hardware reset (nRST assertion) is recommended following power-up. This signal resets all logic and registers within the LAN7431. Microchip does not recommend the use of an RC circuit for this pin reset. A reset generator/voltage monitor is one option to provide a proper reset. Preferably, for increased design flexibility, a controllable reset (GPIO, dedicated reset output) should be considered. In this case, Microchip recommends a push-pull type output (not an open-drain type) for the monotonic reset to ensure a sharp rise time transition from low to high.
- **MII_EN** (pin 9), when pulled high, the part operates in MII mode. When pulled low or floated, the part operates in RGMII mode. The internal pull-down is disabled once the strap is latched. If an external pull-up is used, it should be connected to **VDDVARIO_B**.
- **TEST** (pin 45) must be tied directly to the digital ground to ensure proper operation.
- To take advantage of the JTAG interface, the **TEST** pin must be driven high. Then, for normal operation, the **TEST** pin must be driven low.
- The **VAUX_DET** (pin 57) Auxiliary Voltage Detection input pin is used to indicate when Power Management Event (PME) from $D3_{cold}$ is supported. When tied to VSS, PME from $D3_{cold}$ is not supported. The weak pull-down cre-

ates a logic low when plugged into a system board that does not support the delivery of the auxiliary voltage (the auxiliary voltage connection is floating).
When the device is powered exclusively from the auxiliary voltage, this pin is tied to the auxiliary voltage (3.3V) to indicate PME from $D3_{cold}$ is supported.
When the device is powered from a multiplexed main voltage/auxiliary voltage, this pin is tied to the auxiliary voltage (3.3V) to indicate PME from $D3_{cold}$ is supported and to monitor the presence of the auxiliary voltage.

Note: If alternate usage of this pin (**GPIO3**) is enabled, the pull-down is disabled, and the input value of the pin is overridden to a low value.

- Since this pin is shared with **GPIO3**, a series resistor is recommended to prevent an accidental conflict with the auxiliary voltage. This resistor must be low enough in value to override the on-chip pull-down.

  Note: For a detailed description of the PME pins and operation with the LAN7431, refer to the *LAN7431 Data Sheet*.

- The LAN7431 has an IEEE 1149.1-compliant JTAG Boundary Scan interface. This test interface can be utilized to accomplish board-level testing to ensure system functionality and board manufacturability. For details, see the *LAN7431 Data Sheet*.
- Be sure to incorporate enough bulk capacitors (4.7-22 µF) for each power plane.

7.0 HARDWARE CHECKLIST SUMMARY

TABLE 7-1: HARDWARE CHECKLIST SUMMARY

Sections	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Pin Check"	Verify pins match the data sheet.		
	Section 2.2, "Ground"	Verify grounds are tied together.		
Section 3.0, "Power"	Section 3.1, "+3.3V Power Supply Connections", Section 3.2, "VDDVARIO Power Supply Connections", Section 3.3, "VDDVARIO_B Power Supply Connections", Section 3.4, "+2.5V Power Supply Connections", and Section 3.5, "+1.2V Power Supply Connections"	• Ensure **VDDVARIO**, **VDD_SW_IN**, **VDD_REG_IN**, and **VDD_OTP** pins are connected to 3.3V with 0.01 µF decoupling capacitor. • Ensure **VPH** and **AVDDH** pins are connected to **VDD25_REG_OUT** pin by a ferrite bead and a low ESR, 1.0 µF decoupling capacitor. • Ensure **AVDDL**, **AVDD12**, **VP**, and **VPTX** pins are connected to **VDD12_SW_OUT** by a ferrite bead. • Ensure **VDD12CORE**, and **VDD12_SW_FB** pins are connected to **VDD12_SW_OUT** pin. • Ensure **VDD12_SW_OUT** pin has a low ESR 22 µF capacitor connected to GND.		
Section 4.0, "Clock Circuit"	Section 4.0, "Clock Circuit"	• Verify usage of 25M Hz +/- ppm crystal. • Verify a 25 MHz ppm external oscillator.		
Section 5.0, "Digital Interfaces"	Section 5.1, "RGMII Interface"	• Verify that RGMII pin connections are correct. • Provide provision for the series termination resistors.		
	Section 5.2, "MII Interface"	Verify that MII pin connections are correct.		
	Section 5.3, "EEPROM Interface"	• Ensure usage of 3-wire style 2K/4K EEPROM that is organized for 256/512 X 8-bit operation. • Verify the **EECS**, **EECLK**, and **EEDIO** pin connections. Note that **EEDIO** (pin 37) connects to EEPROM's Data out and Data In, both pins.		
	Section 5.4, "PCIe Interface"	Verify **PCIE_TX_P**, **PCIE_TX_N**, **PCIE_RX_P**, and **PCIE_RX_N** pin connections are correct. Note that **PCIE_TX_P** and **PCIE_TX_N** pin requires 0.1 to 0.2 µF DC blocking capacitors.		
Section 6.0, "Miscellaneous"	Section 6.1, "ISET Resistor"	Confirm a precise 6.04K (with 1% tolerance) resistor on the ISET pin.		
	Section 6.2, "RESREF Resistor"	Confirm a 200Ω resistor on RESREF pin.		
	Section 6.3, "Required External Pull-Ups/Pull-Downs"	Verify a pull-up or pull-down resistor on **GPIO0-GPIO3**, **LED0-LED3**, **WAKE#**, and **CLKREQ#** pins.		
	Section 6.4, "Other Considerations"	• Verify that the **TEST** pin is connected to GND. • Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. • Incorporate sufficient power plane bulk capacitors (4.7-22 µF).		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002910A (01-08-19)	All	Initial release.

NOTES:

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
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- Field Application Engineer (FAE)
- Technical Support

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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ISBN: 978-1-5224-4029-1

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