APPLICATION NOTE

AT11309: Advanced RF Layout with Altium

ATSAMR21, ATmega256RFR2, AT86212B

Introduction

Printed Circuit Board (PCB) layout for Radio Frequency (RF) uses uncommon techniques that contradict basic design rules. RF designers use physical structures on PCBs as circuit elements; complex impedances, transmission lines, PCB-antennas, intentional shorts, tuning stubs, and ground-planes are all tools used by RF designers. These structures work at high frequency but they can violate Design Rules (DRCs) followed by basic Computer Aided Design (CAD) tools. Altium® is no exception. This paper illustrates how to configure Altium to manage these uncommon layout techniques.

Features

- PCB Stack-up Management
- Configuring Component Classes
- Configuring Design rules
- Net Ties
- Transmission Lines
- Polygon Pouring
- Polygon Keepouts
- Via Stitching
- 3D modeling with Paper Mock-ups

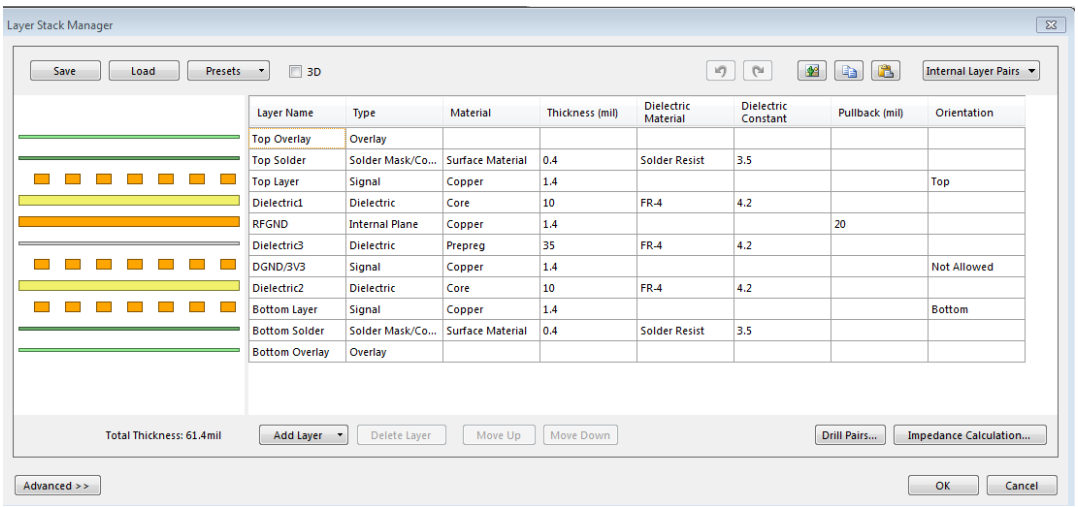
1 Background

When laying out Atmel® RF devices like ATSAMR21 or ATmega256RFR2, there are several uncommon techniques that are required to succeed. Management of multiple ground-planes, using stack-up to control impedance, and Via Stitching to improve Electro-Magnetic Compliance (EMC). This paper is a companion document to the AT08973 SAMR21 Basic Connections and Wireless Design [1] application note and illustrates the use of Altium in the Ramen design. It is expected that the reader has AT08973 available for reference.

2 Stack-up Management

Atmel recommends using a minimum 4-layer stack-up for RF PCBs. 4-layer PCBs consistently exhibit improved transmitter efficiency and EMC over 2-layer construction. The Layer Stack Manager in Altium is used to select the dielectric thickness and stack-up order. In Figure 2-1, the PCB has four layers; Top-Layer, RFGND, DGND/3V3, and Bottom-Layer.

Figure 2-1. Altium Layer Stack Manager



2.2 Altium Layer Stack Manager

In this document, we use the terms Layer-1, Layer-2, Layer-3, and Layer-4. Layer-1 is the “Top-Layer”. This is where all the RF signals are routed. Layer-2 is the RF Ground-plane; this is an Internal Plane that covers the entire PCB (with a few exceptions). Layer-3 is a split-plane for digital power and ground. Layer-4 is for general purpose baseband signals.

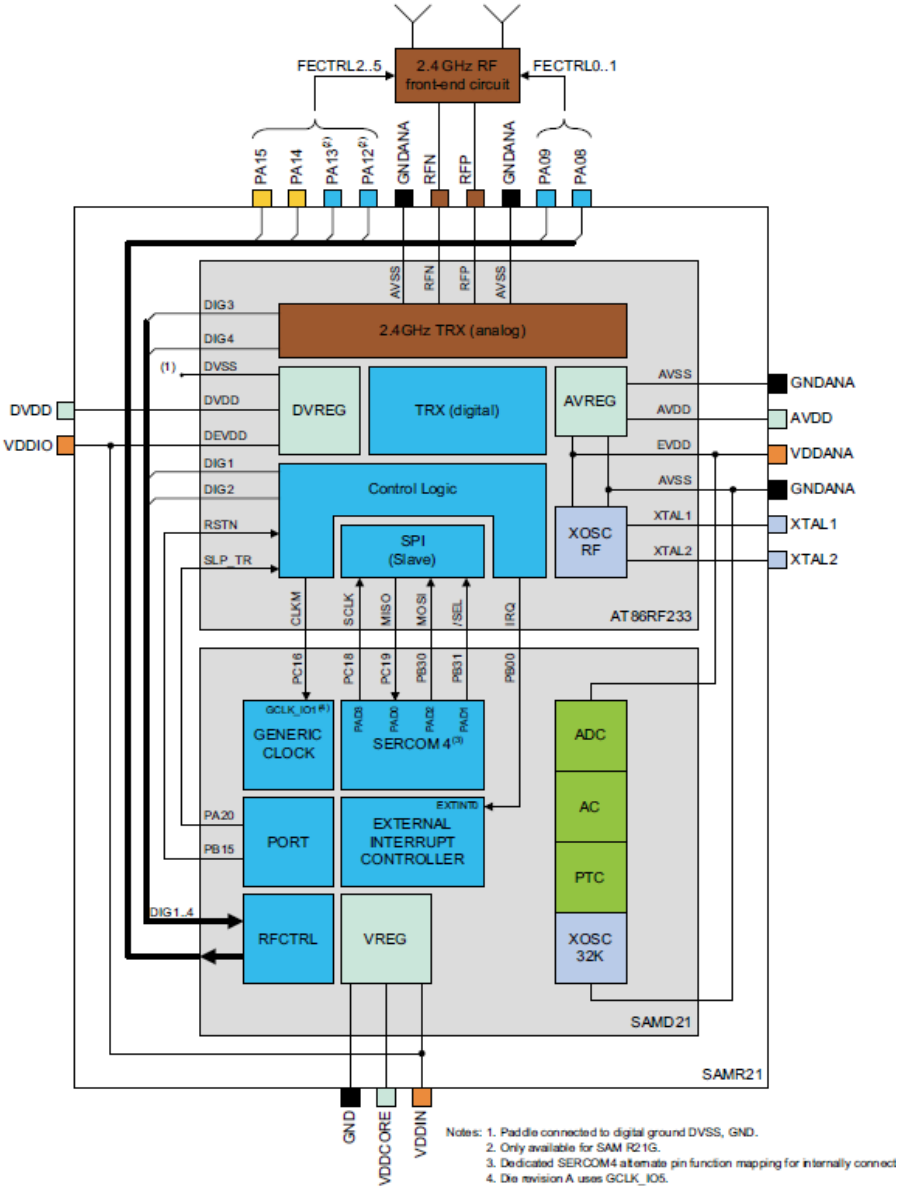
The dielectric thickness between Layer-1 and Layer-2 are adjusted to control the transmission line impedance. Microstrip is used in this design. A 20 mil trances for 50Ω transmission lines results in a 10 mil dielectric. 20 mil traces abut cleanly to 0402 components. The application note AT02865 RF Layout with Microstrip [2] goes into details about dimensions and material selection. The basic idea is to work with the Fabrication House to achieve 50Ω controlled impedance using easily obtainable material. Altium and many other tools can be used to calculate controlled impedance, however, the Fabrication House will have calibrated models and the best working knowledge of available materials.

A core/prepreg/core (CPC) stack-up is used in this design. This is uncommon. Low-cost Fabrication Houses prefer prepreg/core/prepreg (PCP). Using a rigid core dielectric provides a truly planer slab that is more consistent with theoretical modeling. Prepreg is compliant and deformation of dielectric slabs is not negligible. CPC is preferred, however, low-cost products with can use PCP if the Fabrication House can maintain controlled impedance tolerances to 50Ω ±10%.

3 Managing Ground Domains

To start the discussion about Net Ties, the ground domains must be considered. Review of the ATSAMR21 Datasheet [3] shows several ground domains: GNDANA, AVSS, and DVSS. Complete discussion of the grounding system is given in the Ramen reference design [1].

Figure 3-1. ATSAMR21 Power and Ground Connections



To summarize the grounding system used in the Ramen design: GNDANA is connected to RFGND (the plane on Layer-2), AVSS is connected to AGND (signal traces on Layer-1), and DGND (split plane on Layer-3). Altium can cope with one plane and will route the other ground domains as signals as long as they have unique names. The problem is electrically connecting these planes together, at the IC, to form a star topology without confusing the layout tool, or the engineer. The recommended technique for connecting these domains together is adding a metal patch on Layer-1 between the IC pins and the “Paddle”. This makes the paddle the common node of the star network. Regrettably, simply shorting the domains with a “Fill” Polygon will cause DRC errors and/or merging of the signal names.

3.1 NET_TIES

Altium provides a special virtual component for shorting signals called a “Net Tie”. Net Ties are allowed to short two networks without throwing DRC errors. To implement Net Ties we need to take the following steps:

- Define the footprint of the Net Tie
- Define a schematic symbol for the Net Tie
- Connect the ground domains to the Net Tie in the schematic
- Create a NET_TIE class
- Create rules for the NET_TIE class
- Place the NET_TIE on the layout

3.2 Defining the Net Tie Footprint

The Net Tie footprint is created in the PCB library like any other custom footprint. In this example the Net Tie has two pins and is a 12 mil metal strap between the pins. The dimensions are chosen to work with the pins on the ATSAMR21 QFN package. The reader should review the Altium application note “Net Ties and How to Use Them” [4] for more details.

Figure 3-2. Net Tie in Footprint Editor

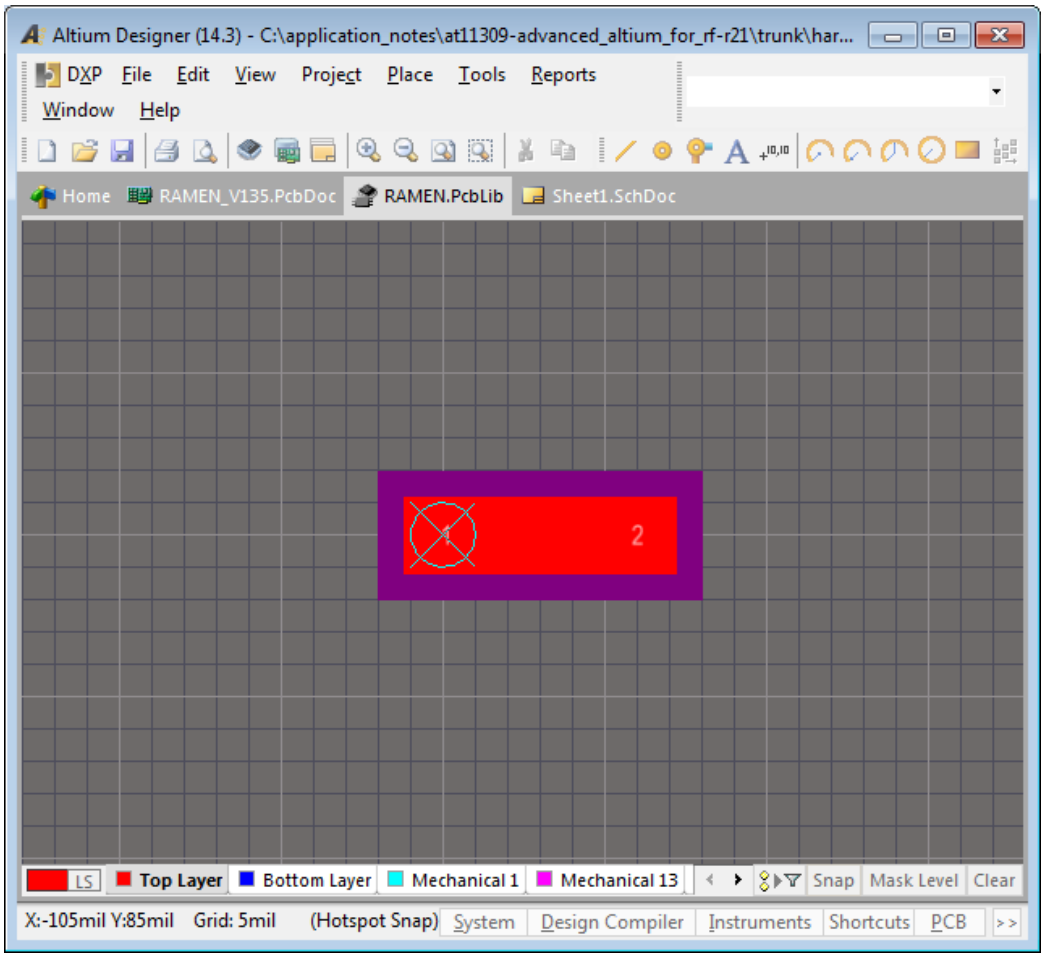
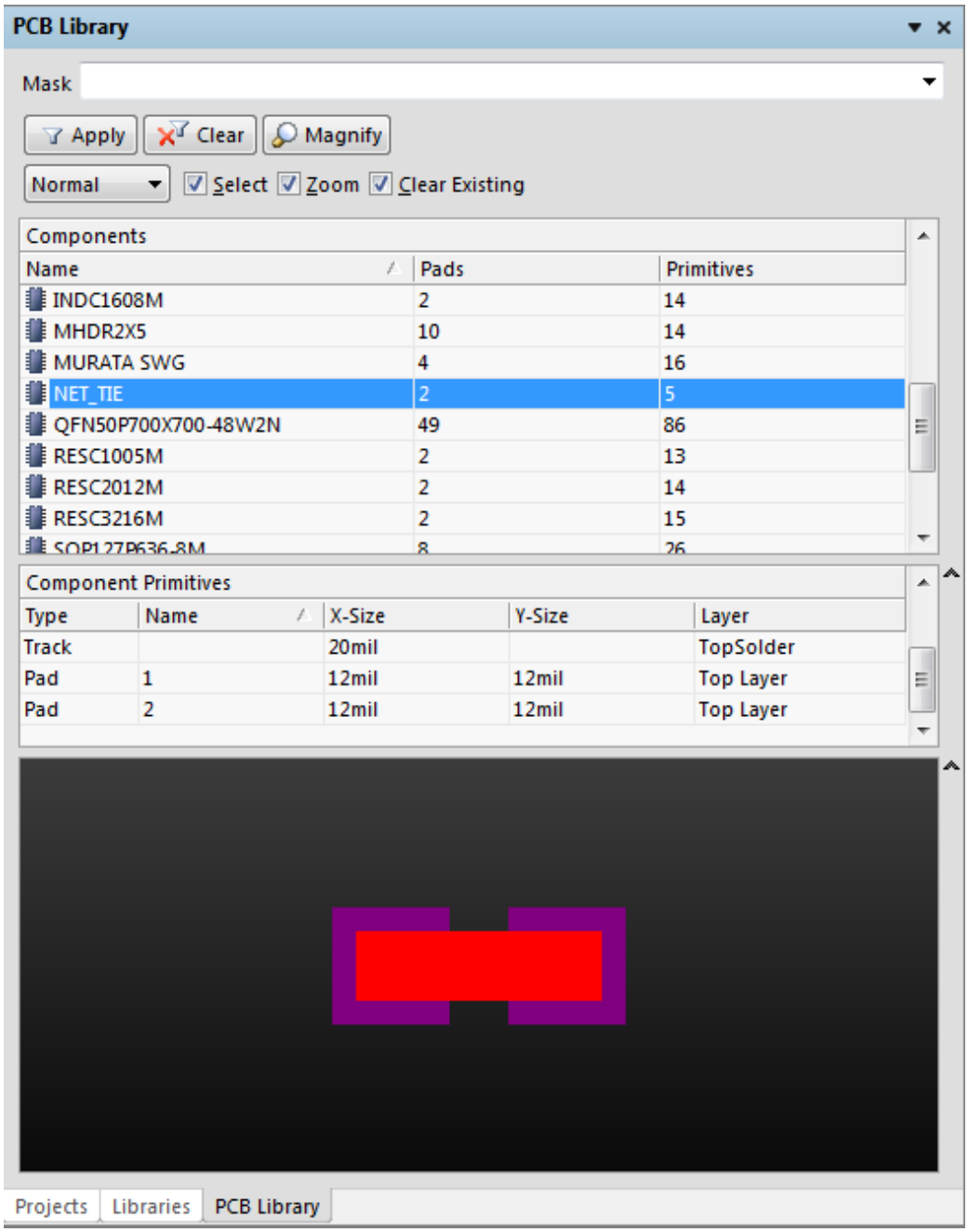


Figure 3-3. Net Tie in PCB Library



3.3 Defining a Schematic Symbol for the Net Tie

After making a footprint the Layout Engineer needs to define a schematic symbol for the Net Tie in the SCH Library editor. A simple two pin block is used in this design, shown in Figure 3-4.

Figure 3-4. Net Tie Schematic Symbol

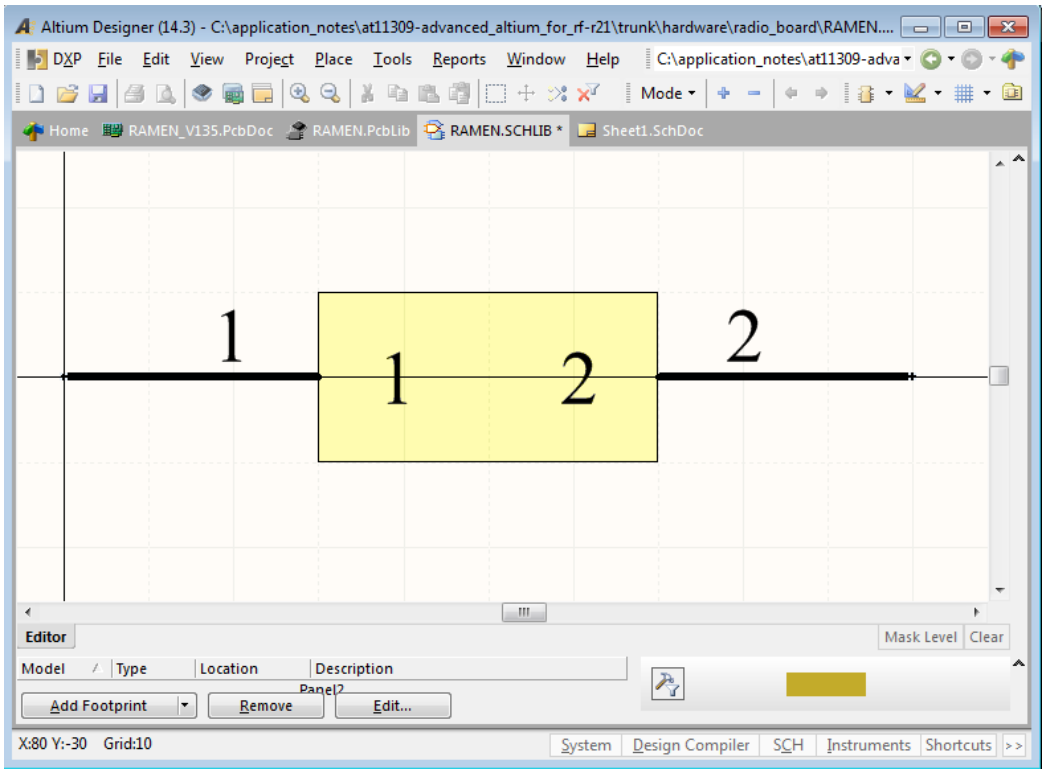
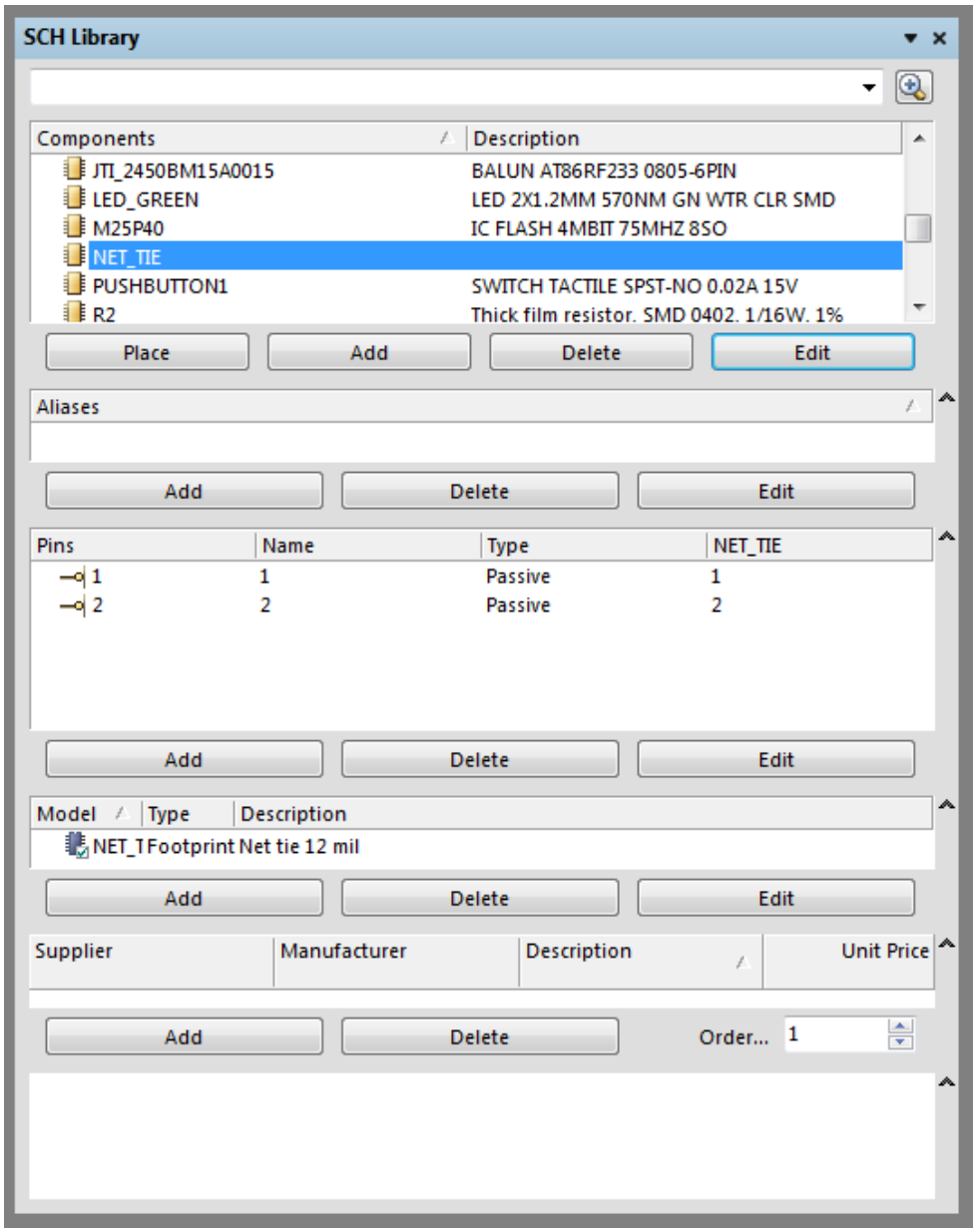
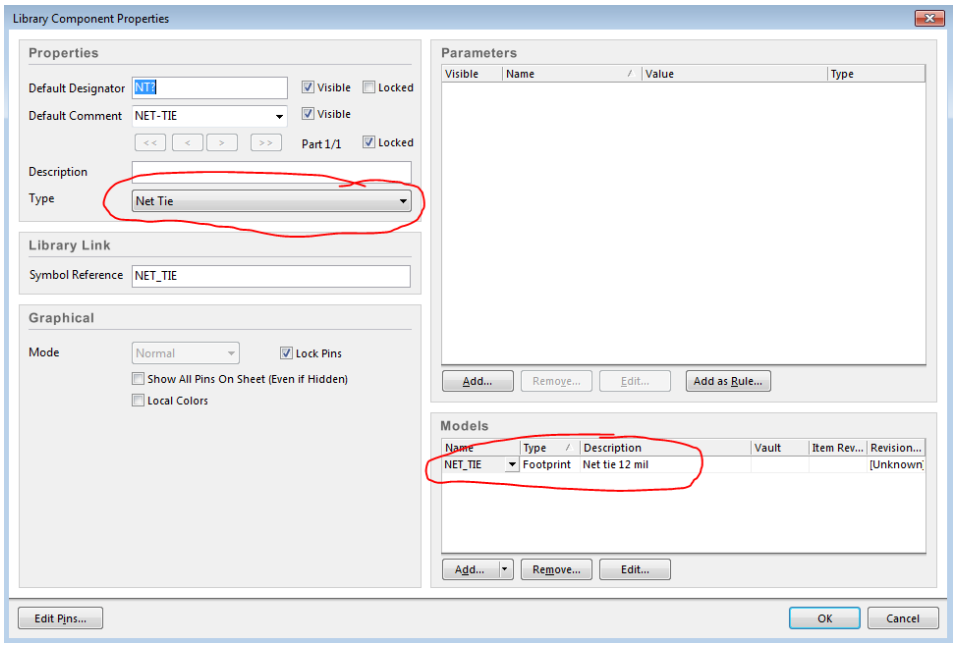


Figure 3-5. Net Tie Symbol in SCH Library



Now, to make it all work, define the Component Properties Type as “Net Tie” and link it to the footprint made previously. To get to the Library Component Properties panel, select the NET_TIE component in the SCH Library and push the “Edit” button. Also note the use of the “NT?” prefix for the reference designator. This will be useful later when establishing rules.

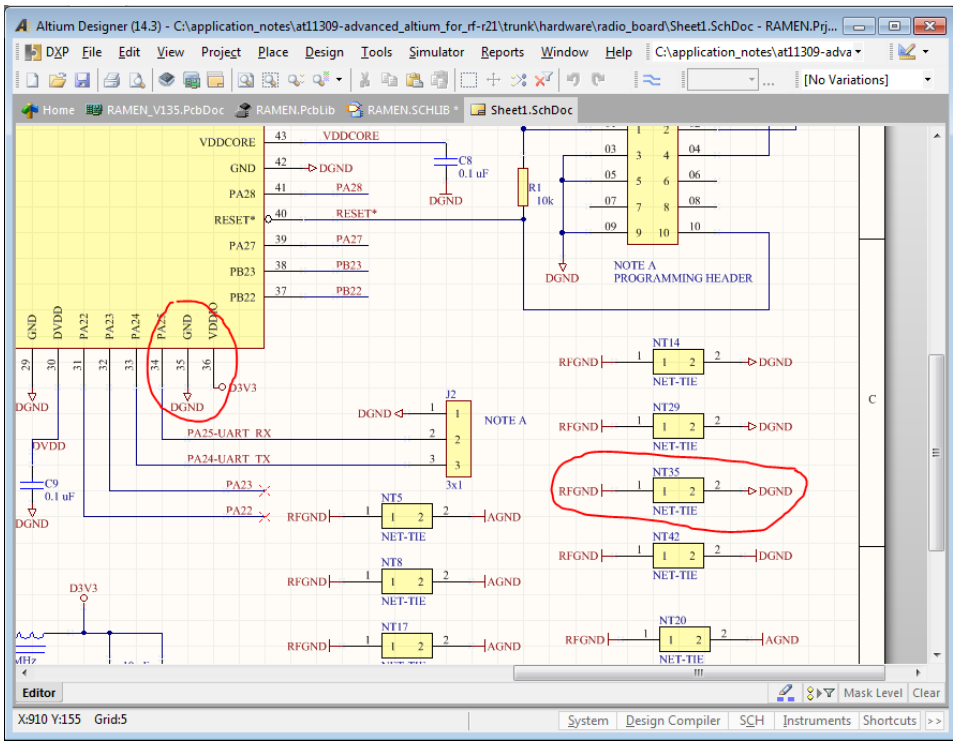
Figure 3-6. Component Properties for Net Ties



3.4 Connecting Grounds in the Schematic

Using the Net Tie component in the schematic is simple although the additional symbol will be a bit confusing to the uninitiated. In the Ramen design the reference designators match the pin numbers of the SAMR21. In this way, place them on the correct pins in layout. Figure 3-7 shows NT35, which will be used to connect RFGND and DGND at Pin 35.

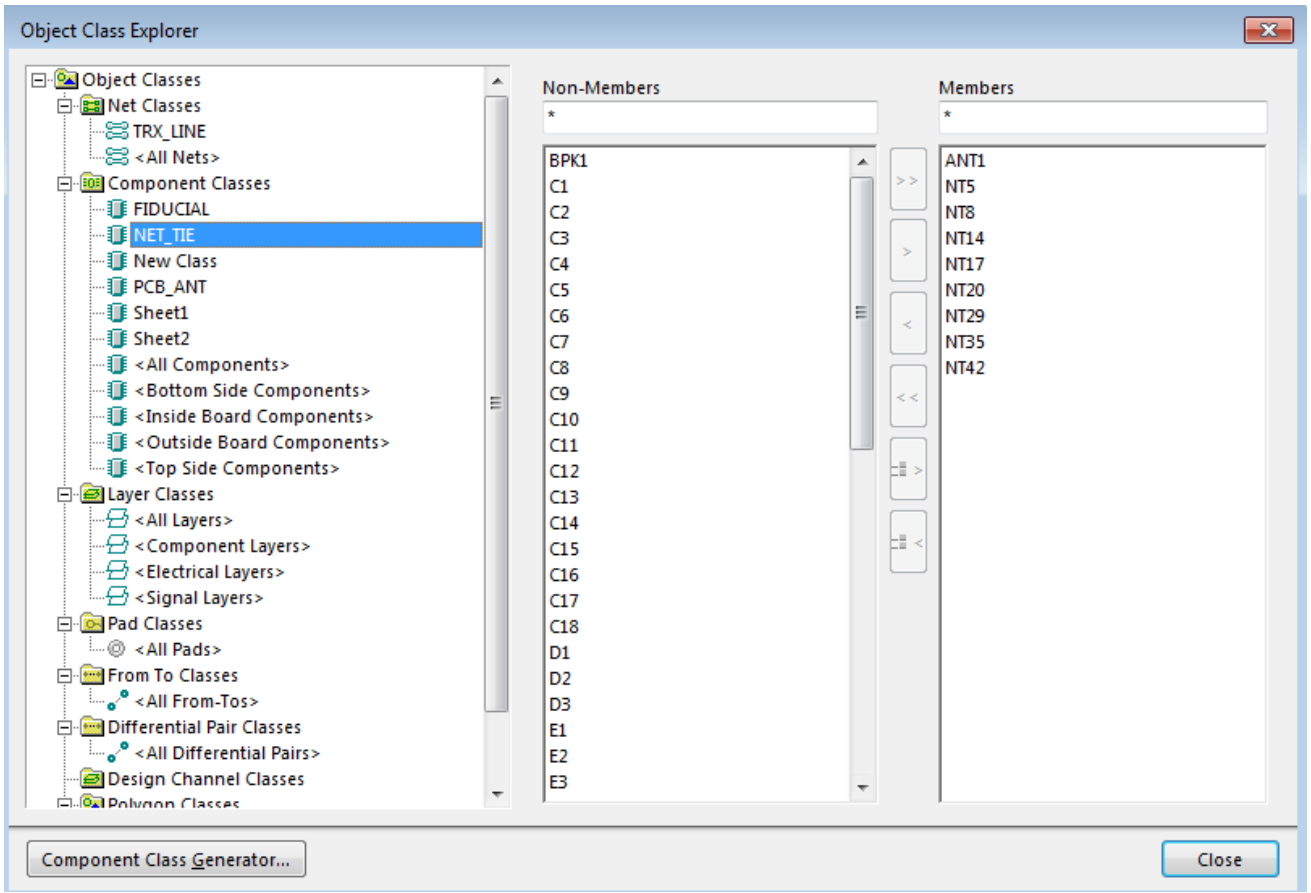
Figure 3-7. NET_TIEs Connected in the Schematic



3.5 Creating a NET_TIE Class

Create a NET_TIE class in the PCB Editor. In the PCB Editor select Design → Classes… to open the Object Class Explorer. Right-click on “Component Classes” and add a new class. In the example the class is called “NET_TIE”. Upper case labels are used to distinguish the special entries from the default configuration. After adding the new class, use the tool to add members to the class. In this case all the Net Ties have the “NT” prefix.

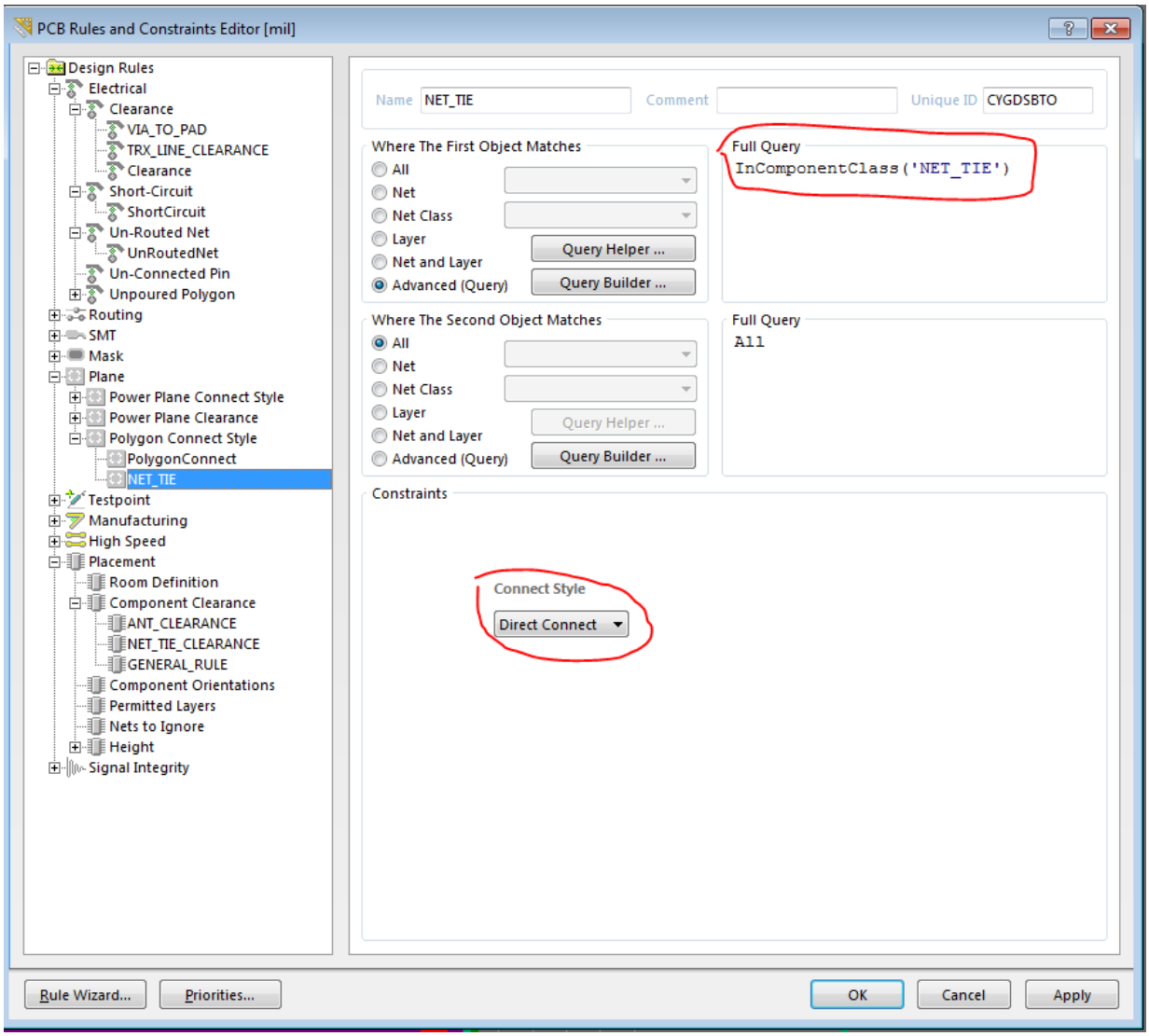
Figure 3-8. NET_TIE Class and its Members



3.6 Creating Rules for NET_TIEs

Create the rules for the NET_TIE class to avoid generating DRC errors. From the PCB editor menu select Design → Rules… to open the PCB Rules and Constraint Editor. In the editor, create two rules for NET_TIES. First add a rule to the Plane → Polygon Connect Style group. Set the Connect Style to Direct Connect. This allows to place the NET_TIE directly on the metal plane. See [4] for details.

Figure 3-9. Changing the NET_TIE Rules



Next, make changes to the vertical component clearance because Altium does not know NET_TIES have zero height. There are two steps:

A. Exclude NET_TIES from the default rules.

B. Make a special rule for NET_TIES that ignores clearances about U1.

Figure 3-10 shows a modification of the of the Placement → Component Clearance rule. The new "GENERAL_RULE" is the same as the default except the NET_TIE and PCB_ANT classes are excluded.

Figure 3-10. GENERAL_RULE for Component Placement

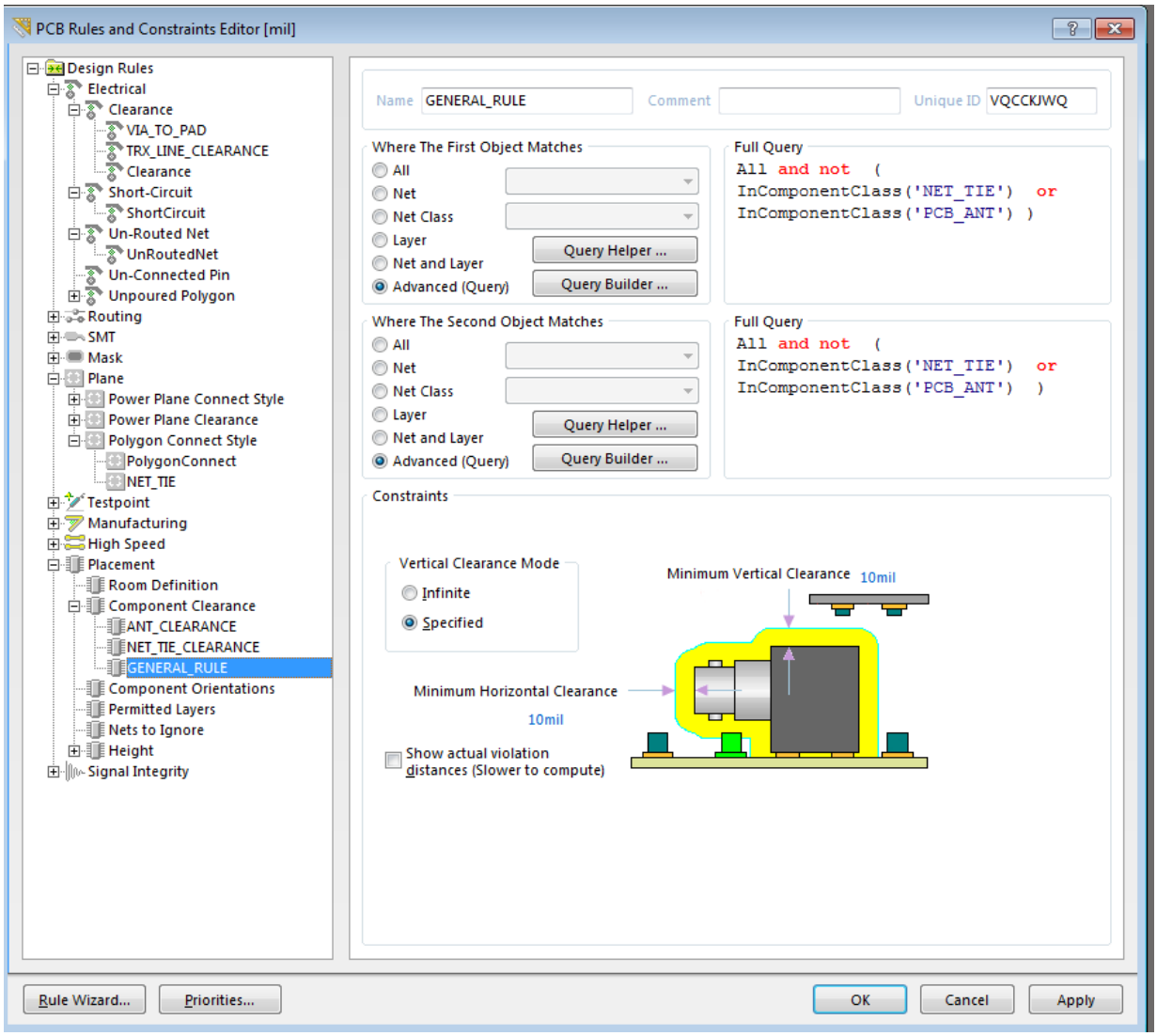
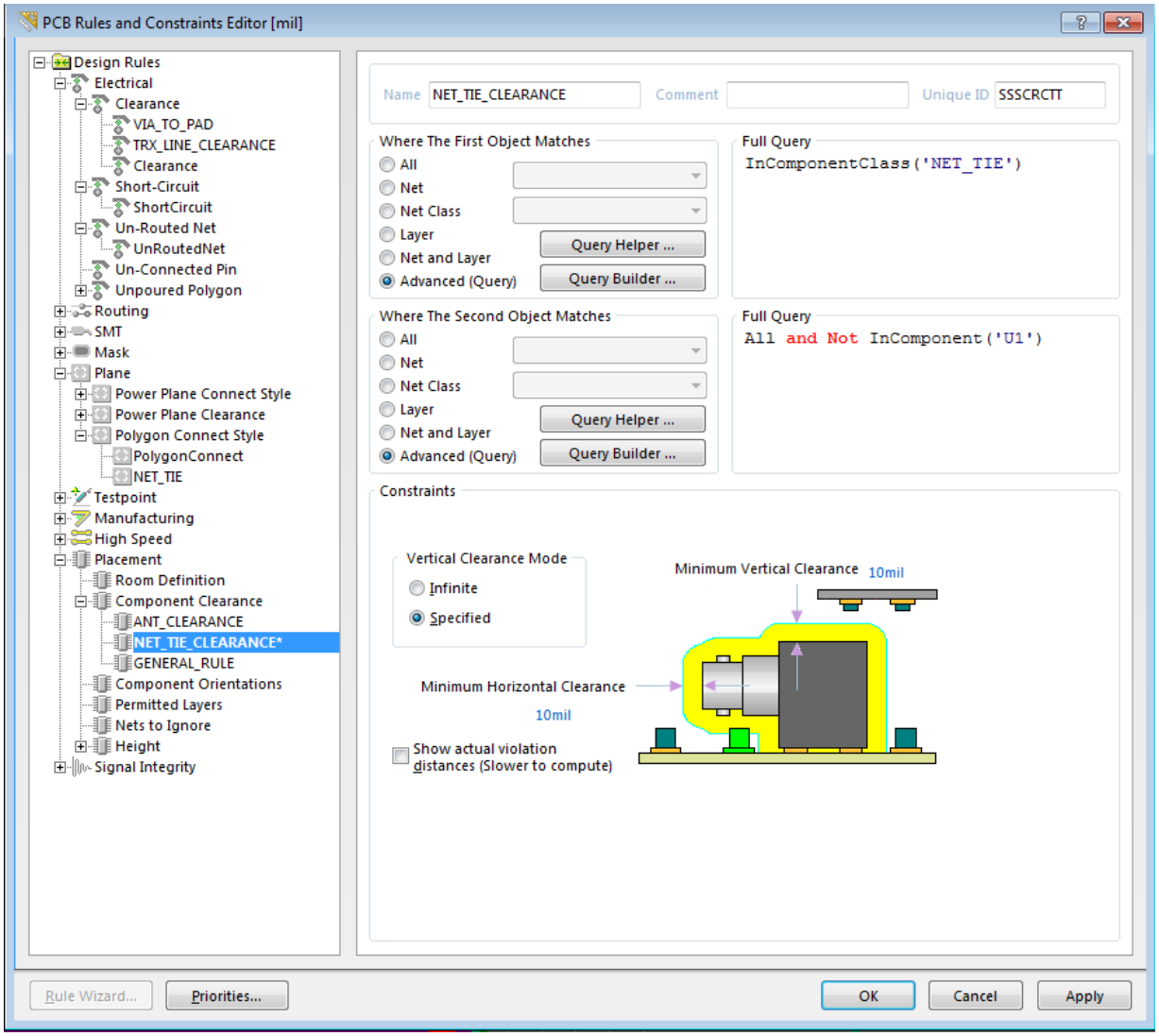


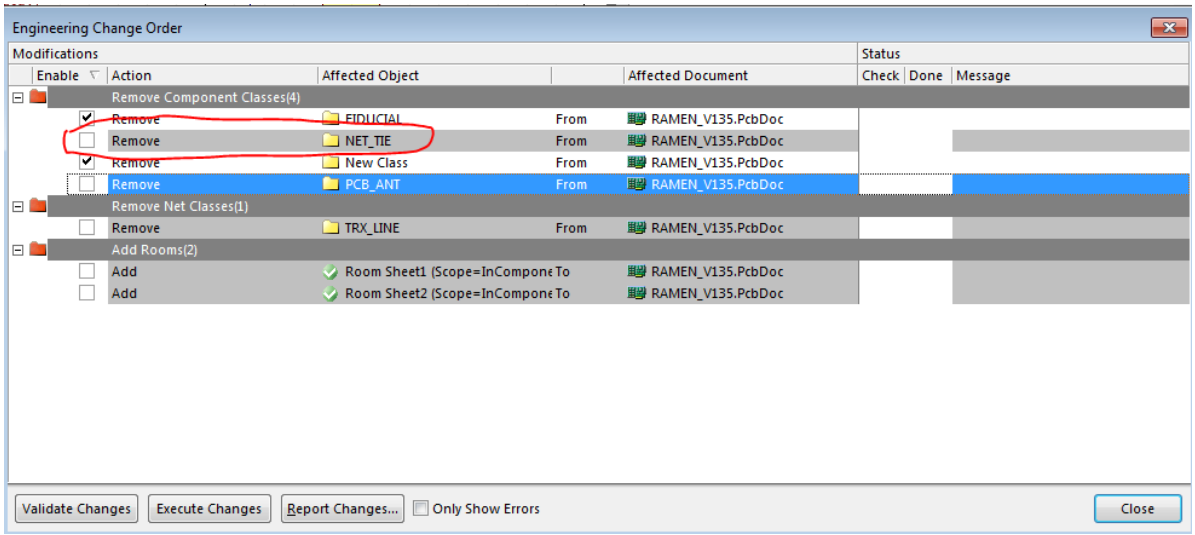
Figure 3-11 shows the special rule for the NET_TIE class. The dimensions are the same as the GENERAL_RULE except it ignores U1. Now place NET_TIES under U1 without throwing errors. For everything else, U1 is still protected from encroachment by the GENERAL_RULE.

Figure 3-11. NET_TIE Rule Ignoring U1



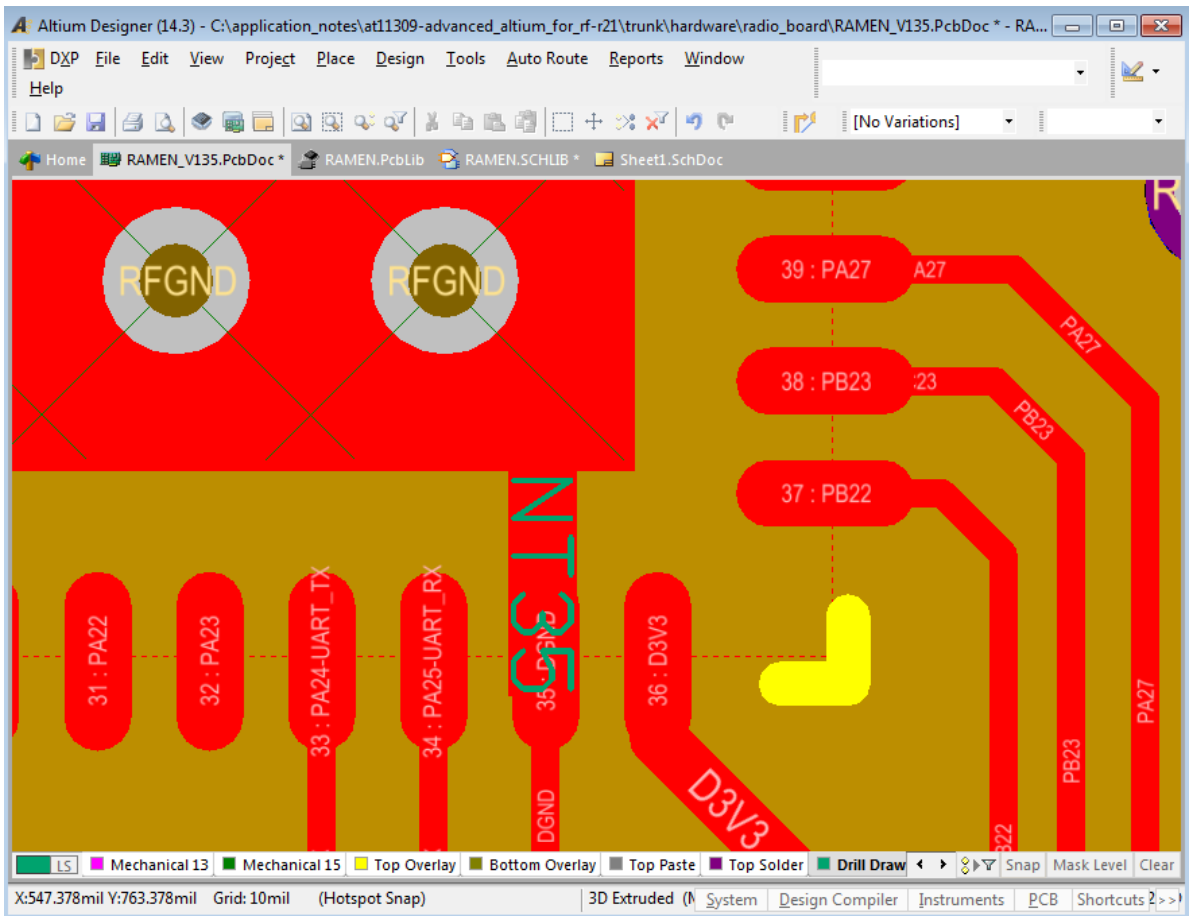
Place the NET_TIE on the layout. When pushing changes from the Schematic Editor down to the PCB Editor the Altium ECO tool attempts to remove the special classes. Bad ECO tool. These boxes need to be unchecked every time the ECO tool is run, or the classes will be omitted.

Figure 3-12. Unchecking the Remove Classes Box in the ECO Tool



Place the NET_TIE in the layout. To keep things organized, use reference designator numbers that match the pin numbers of U1. In Figure 3-13 NT35 connects DGND to RFGND by shorting U1.35 and the Paddle U1.49. This process is repeated for all eight of the Net Tie points.

Figure 3-13. NT35 Connecting DGND to RFGND



4 Transmission Lines

Controlled Impedance transmission lines are used in good RF layouts. There are two popular types; microstrip and Coplanar Wave Guide (CPW). This design use microstrip. The impedance control relies on the RFGND plane and dielectric thickness to establish the proper structure to conduct the Transverse Electromagnetic (TEM) Wave. To reduce parasitic coupling, random metal polygons on the top layer need to be pushed away from the transmission line by 40 mil, or 4x the dielectric thickness. To do this, make a TRX_LINE class and set up a special clearance rule. This will keep the Polygon Pour on Layer-1 40 mil away from the transmission line. In this way, Layer-2 becomes the dominant ground-plane for the fields surrounding the transmission line. The parasitic effects of the remaining metal structures on Layer-1 are reduced to less than 1% of the 50Ω impedance.

Figure 4-1. TRX_LINE Class and Members

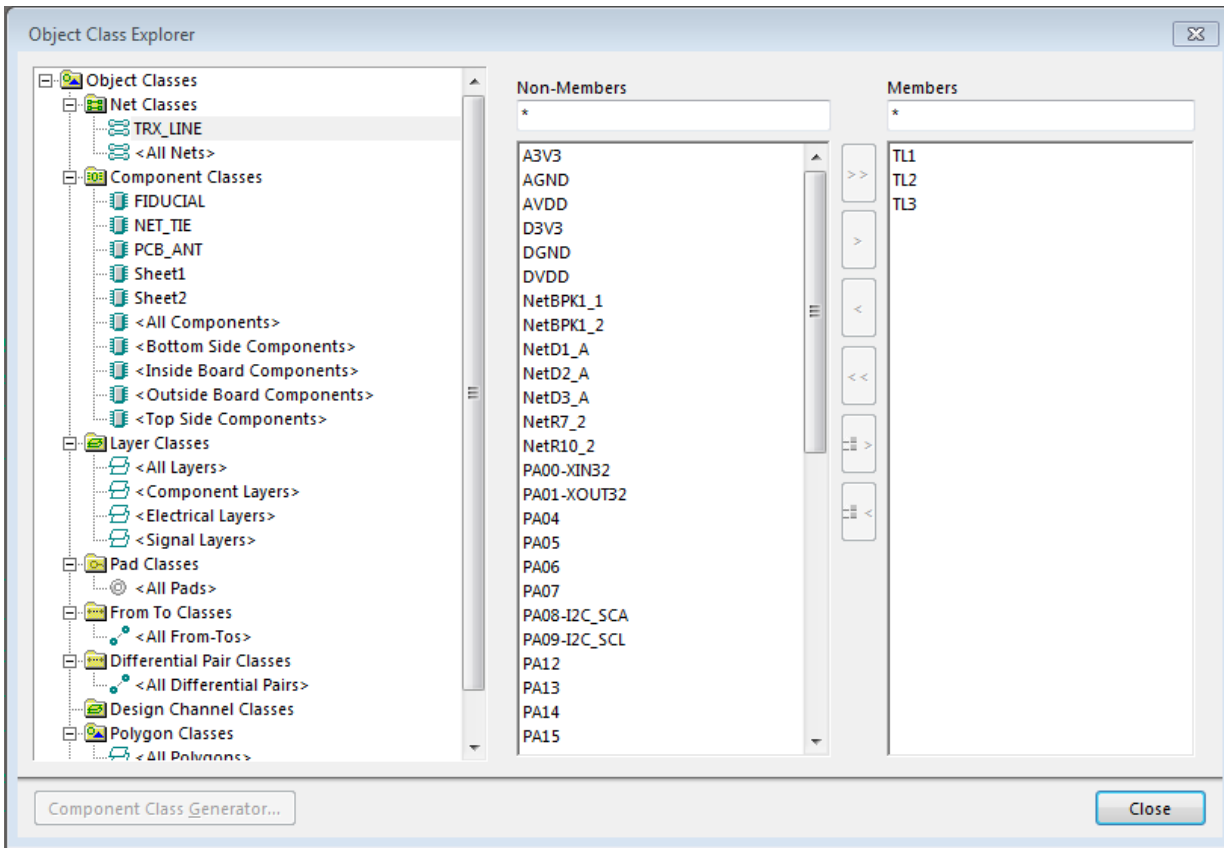


Figure 4-2. TRX_LINE Rule 40 Mil Minimum Clearance

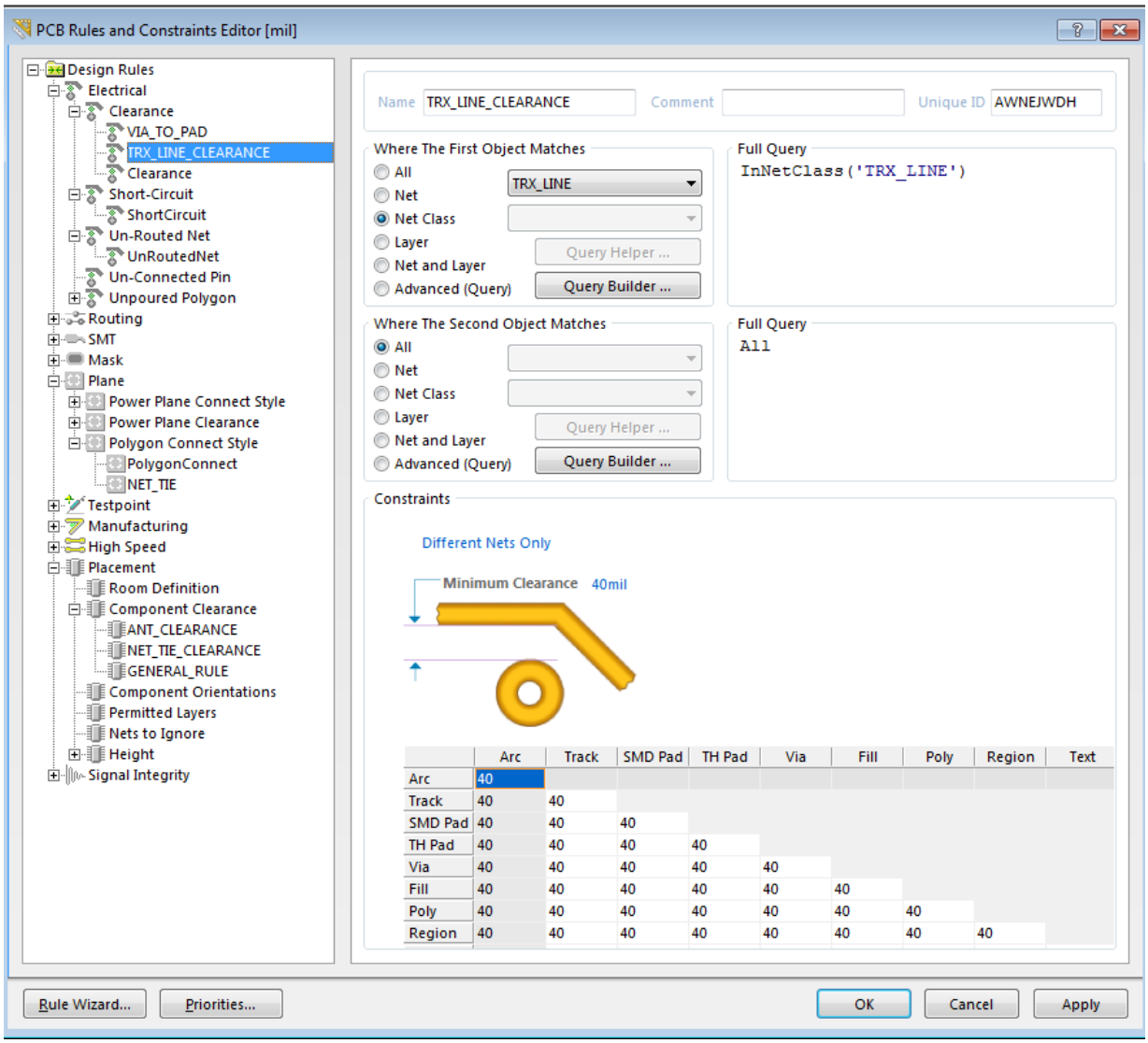
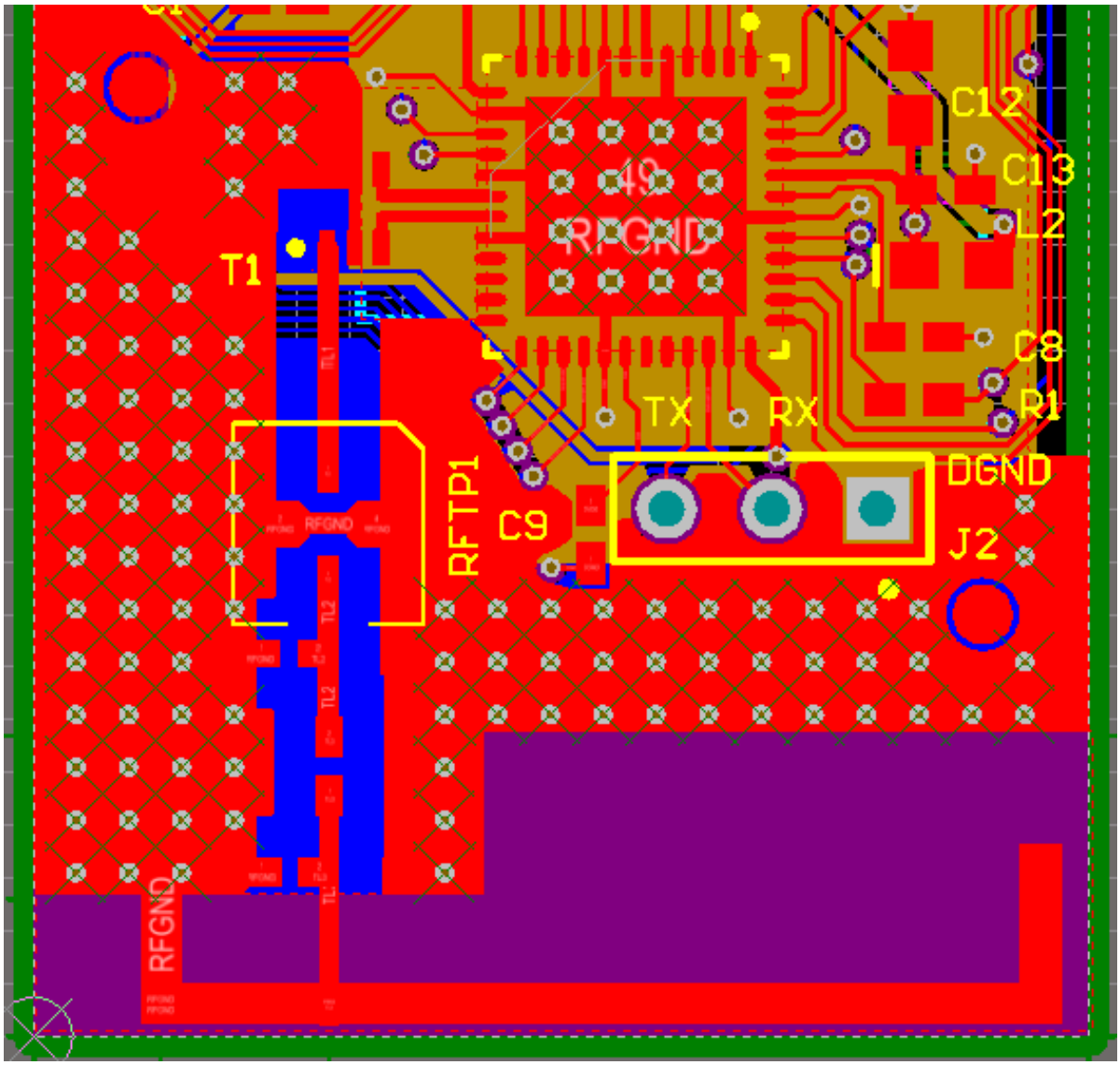


Figure 4-3. RF Transmission Lines with 40 Mil Clearance Shown in Blue



Note: The RFGND plane on Layer-2 is transparent.

5 Copper Pour and Stitching Vias

Copper Pour is a classical Electro Magnetic Interference (EMI) suppression technique. The pour covers un-used areas of the outer layers with metal. For non-radiating designs, this provides shielding and absorption of stray electric fields. The usefulness of copper pour in RF design is debatable; in microstrip designs Layer-2 is the dominant RF Ground-plane and metal structures on Layer-1 will distort the E-Field formation surrounding the transmission line. Additionally, metal polygons in the outer layers can act as sympathetic resonators and increase EMI. In practice. In practical design we must place discrete RF components on top of Layer-1 and these components need a low-impedance path to the RF ground. Making this connection is where copper pour is useful to the RF designers.

Via Stitching is another EMI suppression technique commonly used in RF layout. A matrix of vias is used to provide abundant connections between metal planes. Altium provides an automated Via Stitching tool that is used in conjunction with the Polygon Pour tool to reduce EMI. The CAD Engineer can control the via diameter and the spacing of the matrix. Also the vias are grouped together for across-the-board editing.

Polygon Pour and Via Stitching are automated tools and need some configuration to keep them from running amok. To illustrate, the configuration options are shown in Figure 5-1 through Figure 5-6. First we need to define the design objectives for Poly Pour and Via Stitching:

- Connect RFGND to components on the surface
- Eliminate floating metal islands that act as shields
- Reduce metal ‘Necks’ that act as antennas
- Contain internal planes and reduce edge effects by stitching around the perimeter of the PCB
- Keep Pour away from overcrowded areas
- Guide Via placement with internal DGND plane

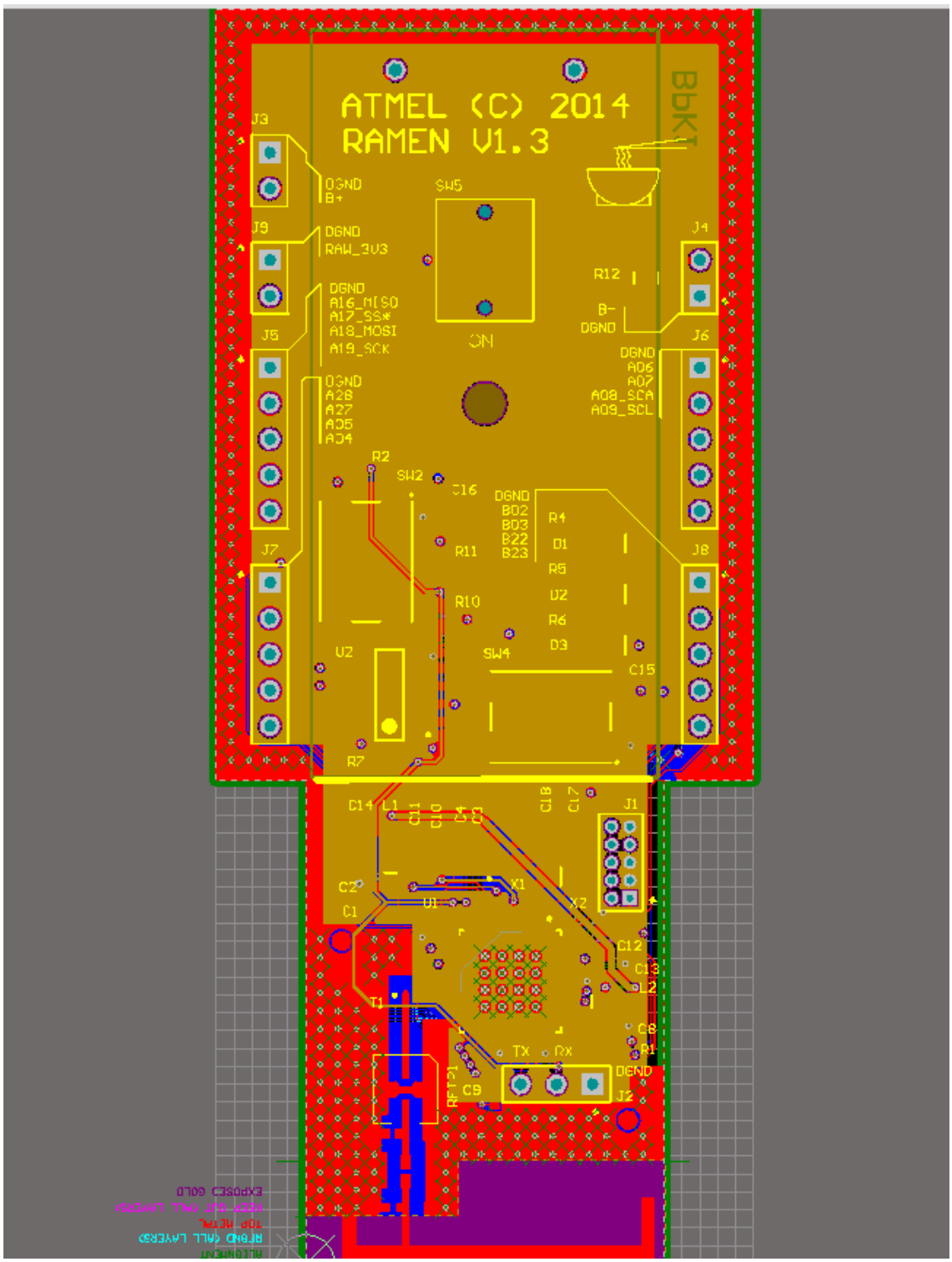
Follow the four step process:

1. Define Internal DGND Plane and pour it on Layer-3. This will connect signals and guide via placement because Vias Stitching is omitted over DGND polygons.
2. Pour top and bottom layers with Remove Dead Copper de-selected.
3. Add stitching vias that will connect RFGND planes on Layer1, Layer-2, and Layer-4.
4. Re-pour top and bottom with Remove Dead Copper selected. This removes any islands that were not connected by Via Stitching.

5.1 Defining the DGND Plane

The first phase is to define the DGND internal plane on Layer-3. Figure 5-1 shows the DGND internal plane on Layer-3. Note the stitching vias are automatically placed outside this plane. Also note when viewing these images, the RFGND plane on Layer-2 covers the entire PCB (except the antenna areas), however, because Altium uses a “negative” image for this plane, Layer-2 cannot be seen.

Figure 5-1. DGND Internal Plane Shown in Brown



5.2 Poly Pour 1st Pass

To configure the Poly Pour tool, use the settings shown in Figure 5-2 in the Poly Pour control panel. Use larger than default values in the Remove Islands and Remove Necks options.

Note: The Remove Dead Copper box is de-selected in the first pass.

Figure 5-2. Poly Pour Configuration, First Pass

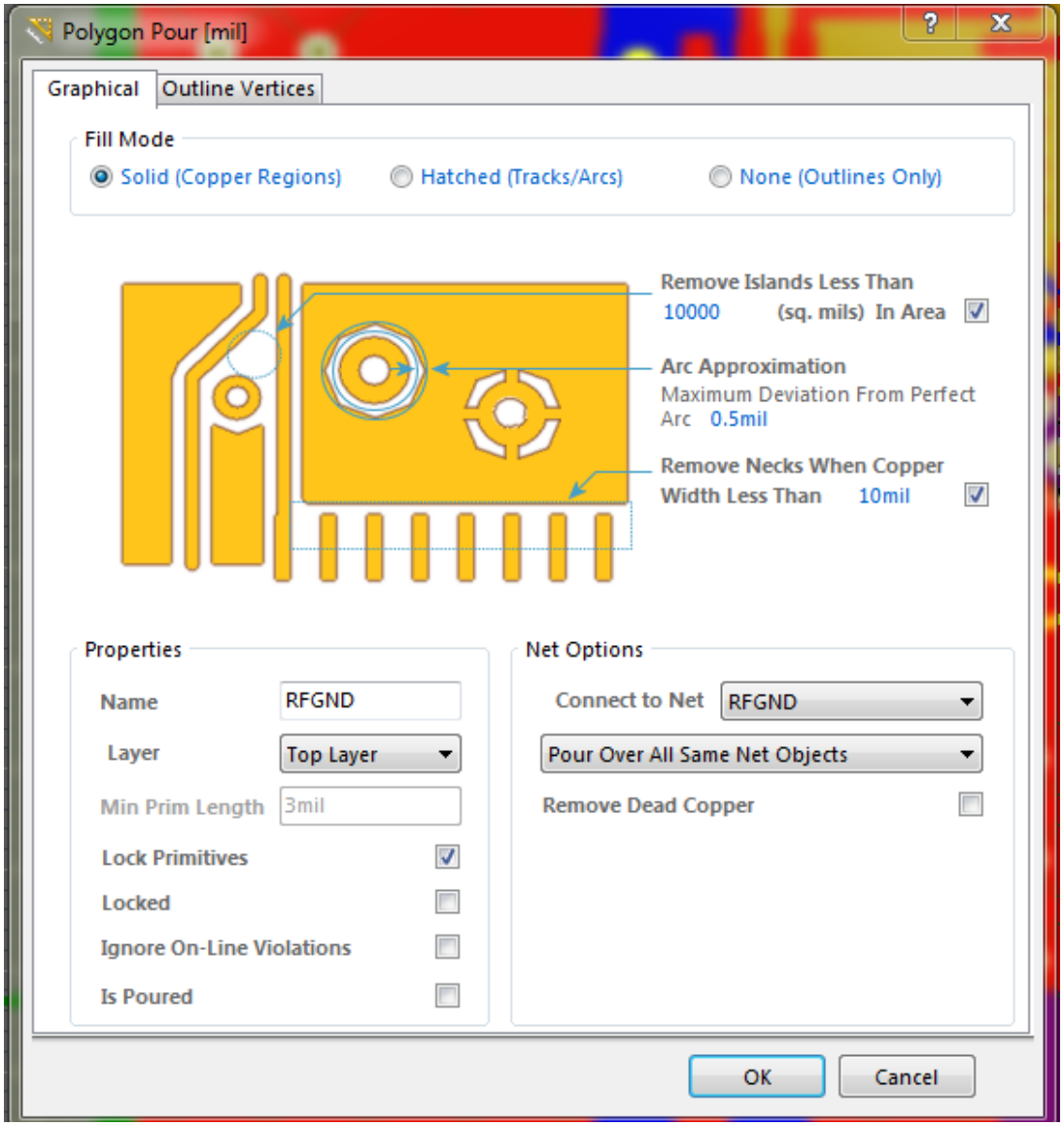
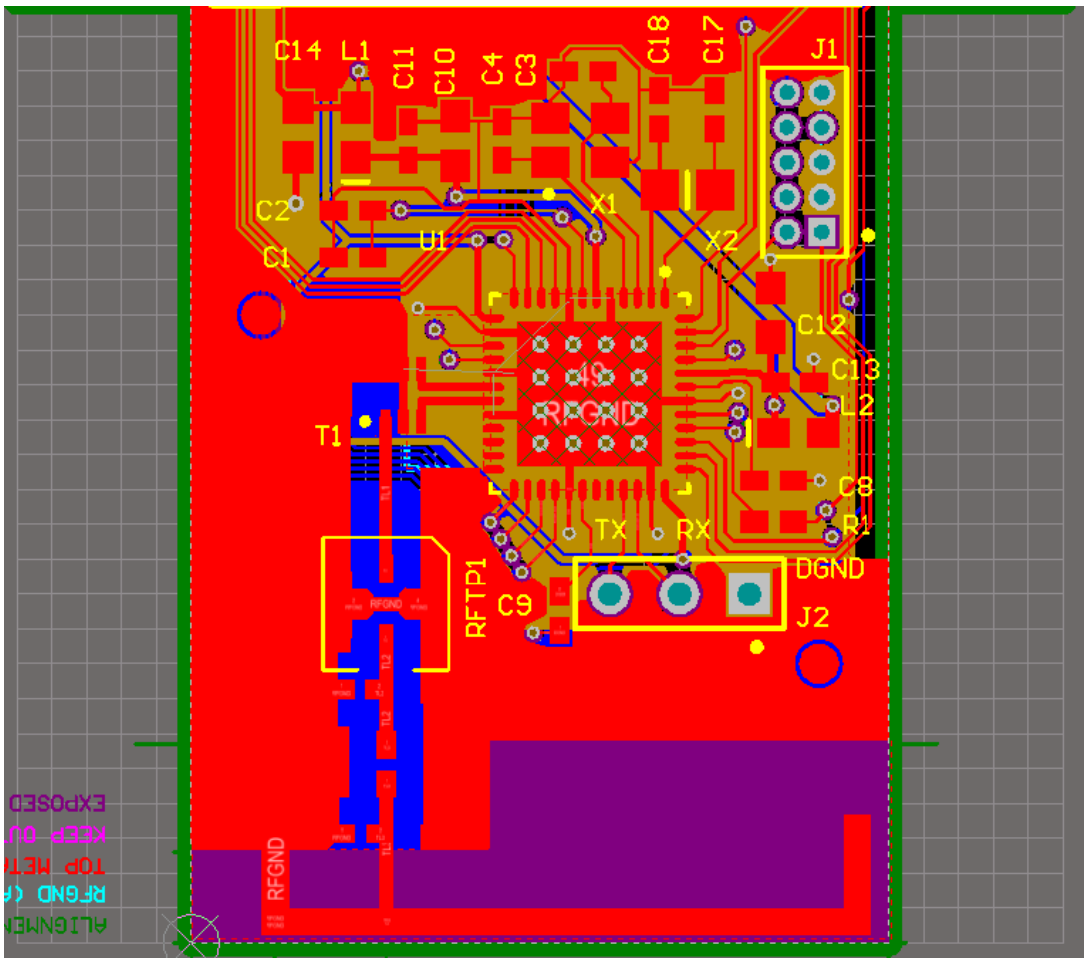


Figure 5-3 shows the top and bottom planes poured with the Remove Dead Copper option disabled. The layout is ready for the vias that will join RFGND signals on the Layer-1, Layer-2, and Layer-4.

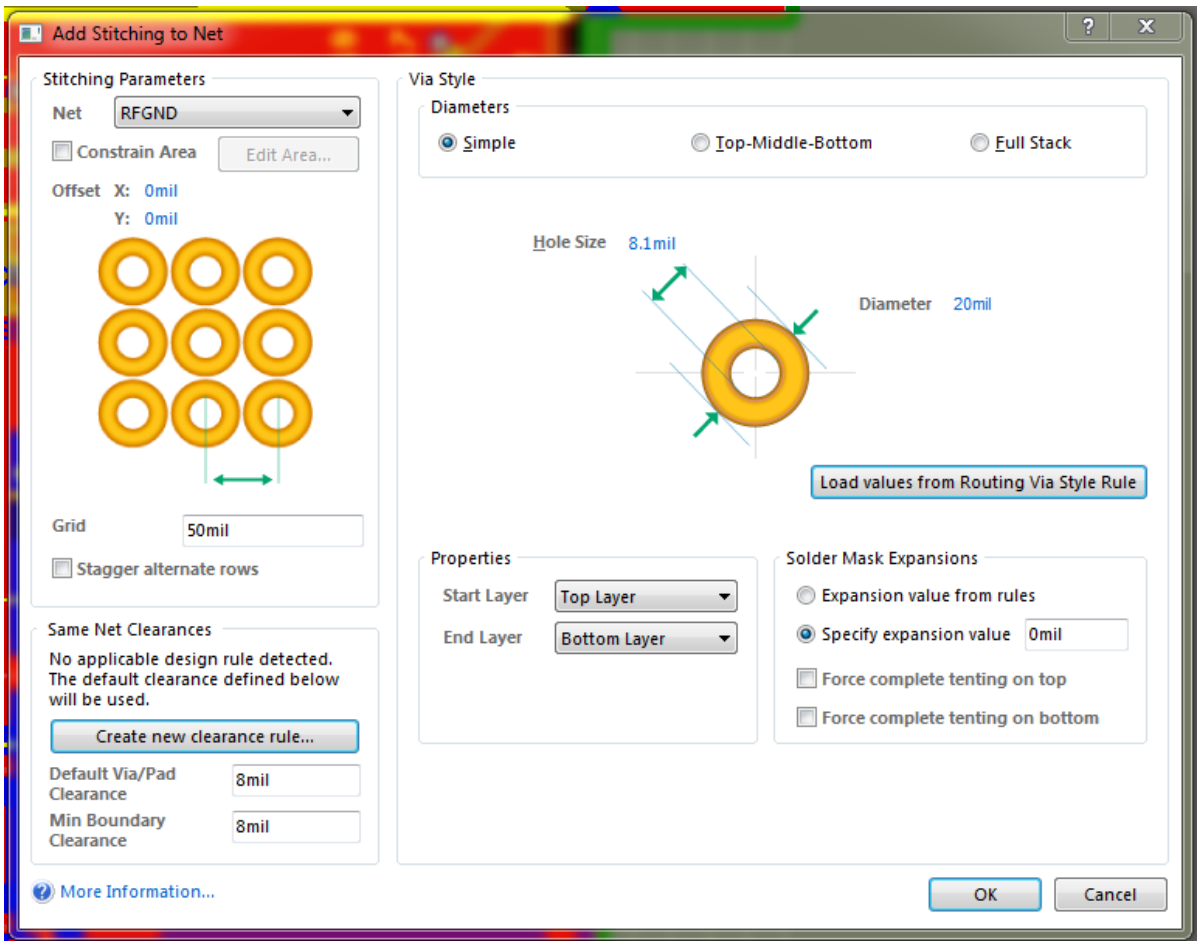
Note: The Floating Island of Copper under the “J1”, this will be removed after the vias are in place.

Figure 5-3. Top and Bottom Planes Poured Ready for Vias



5.3 Adding Stitching Vias

Figure 5-4. Via Stitching Setup

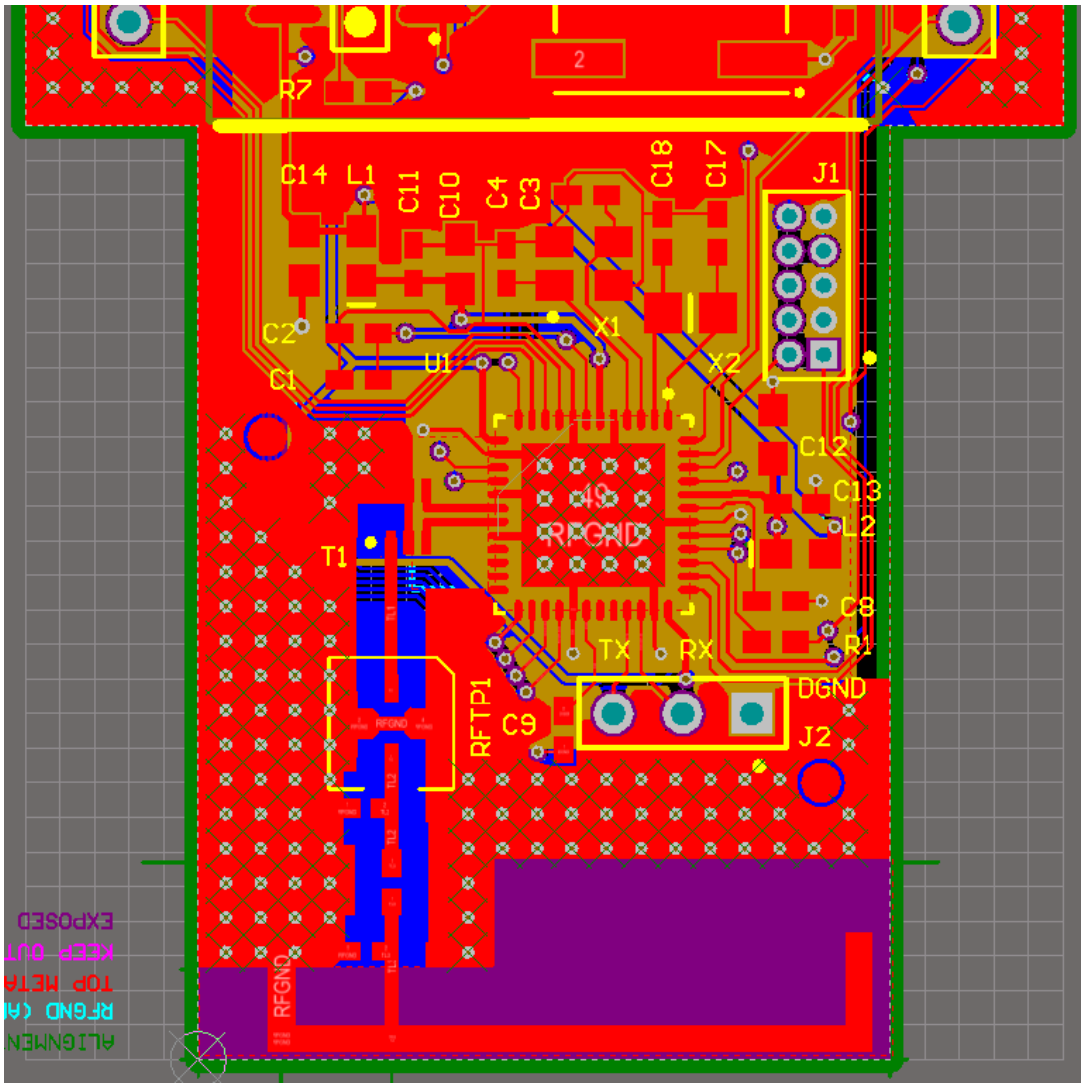


The Stitching Via set panel is shown in Figure 5-4. 50 mil spacing was chosen to get good coverage and eliminating structures that might resonate in the C band.

Note: The diameter of 8.1 mil, was chosen to differentiate the Stitching Vias (8.1 mil) from arbitrary Signal Vias (8.0 mil) for easy identification with the “Find Similar Object” feature in Altium.

The milling machine will round these to the same drill size. After the stitching via tool has run we get the layout in Figure 5-5. Notice the vias were omitted over the DGND plane. This isolated the Floating Island under the J1 designator.

Figure 5-5. Stitching Vias Added



5.4 Poly Pour 2nd Pass

Re-pour the polygons with the Remove Dead Copper option enabled. This eliminates any floating Islands that were not connected by the stitching vias.

Figure 5-6. Final Re-Pour With Remove Dead Copper Enabled

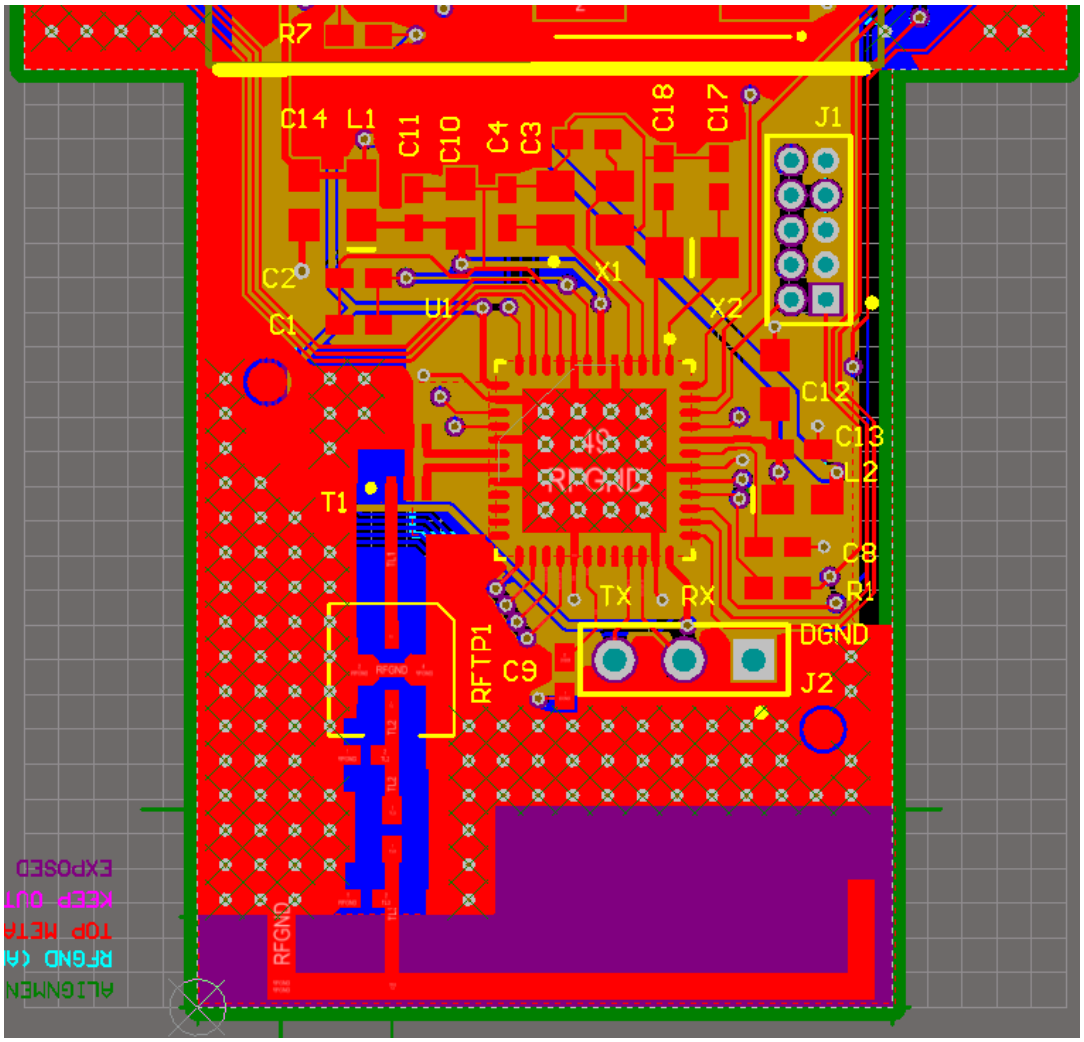
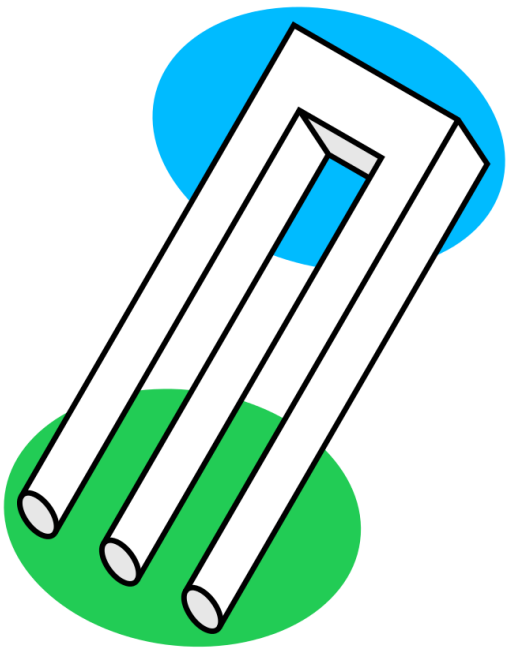


Figure 5-6 shows the final result. The Floating Island under the J1 designator is gone. The small metal necks and islands around the U1 are cleaned up and the remaining Copper Pour on Layer-1 is well connected to the RFGND plane on Layer-2. This provides a generous RF current return path to the balun, RFTP1, and antenna trimming components. Remember, Layer-2 cannot be seen in this image because it is a photographic 'negative'. It covers most of the PCB except the purple keep-put areas near the antenna. A final review of the Gerbers is always recommended to verify the artwork.

6 3D Modeling With Paper Mock-ups

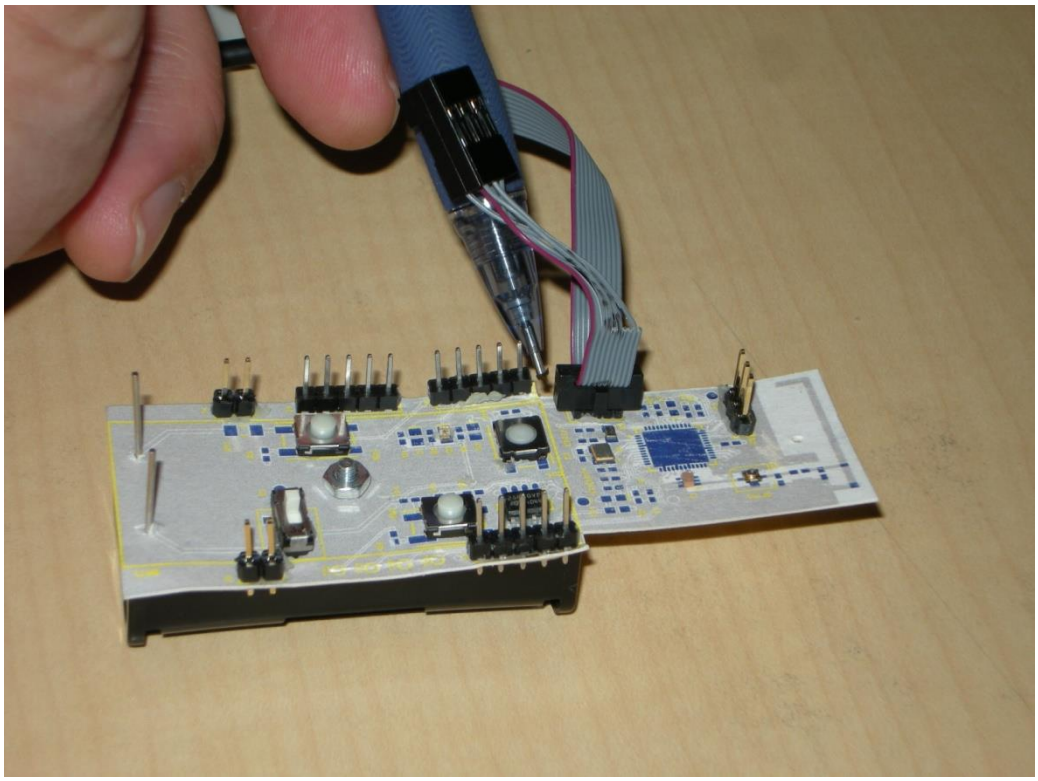
Modern CAD tools have incredible 3D modeling capability. These tools can be used to evaluate mechanical fit of components and enclosures with mind-blowing graphic details, however, virtual 3D models need to be collected and carefully audited for reliable analysis. In practice STEP models may not be available for all the electronic components, particularly new devices. Similarly, mechanical design files for enclosures may be incomplete or non-existent and ultimately, human perception of virtual-reality is abstract and often deficient as illustrated by Figure 6-1.

Figure 6-1. The Blivet, a Great Looking 3D Model With DFM Issues



To improve the PCBA design process, paper mock-up models are an indispensable alternative. Mock-ups are frequently used in advanced Architectural and Mechanical design and can provide physical and tactile observations that elude us in virtual reality. They can be assembled quickly with real-world parts and sub-assemblies from the proto-build. Use case scenarios, like connecting programming cables and button action can be tested. The mock-up shown in Figure 6-2, is an early revision of the Ramen using a 1:1 paper plot, real-world components, and hot glue.

Figure 6-2. Early Paper Mock-Up of Ramen



The mock-up above took only a few hours to construct and provided valuable observations. The pencil is pointing a potential clearance problem with the programming cable. Also note the QFN land pattern came from a mislabeled footprint library and is too big for the real 7x7 mm package. Users got a chance to critique the form-fit-and-function and ultimately reoriented the on/off switch because the neighboring headers poked their fingers. PCBA mock-ups are quick to make and give designers an unmatched practical perspective. A few hours with scissors and glue will save designers some unnecessary grief and insure the project's success.

7 Bibliography

[1] AT08973: SAMR21 Basic Connections and Wireless Design

[2] Atmel AT02865: RF Layout with Microstrip

[3] ATSAMR21 Datasheet

[4] Altium Net Ties and How to Use Them

8 Revision History

Doc Rev.	Date	Comments
42478A	07/2015	Initial document release.

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