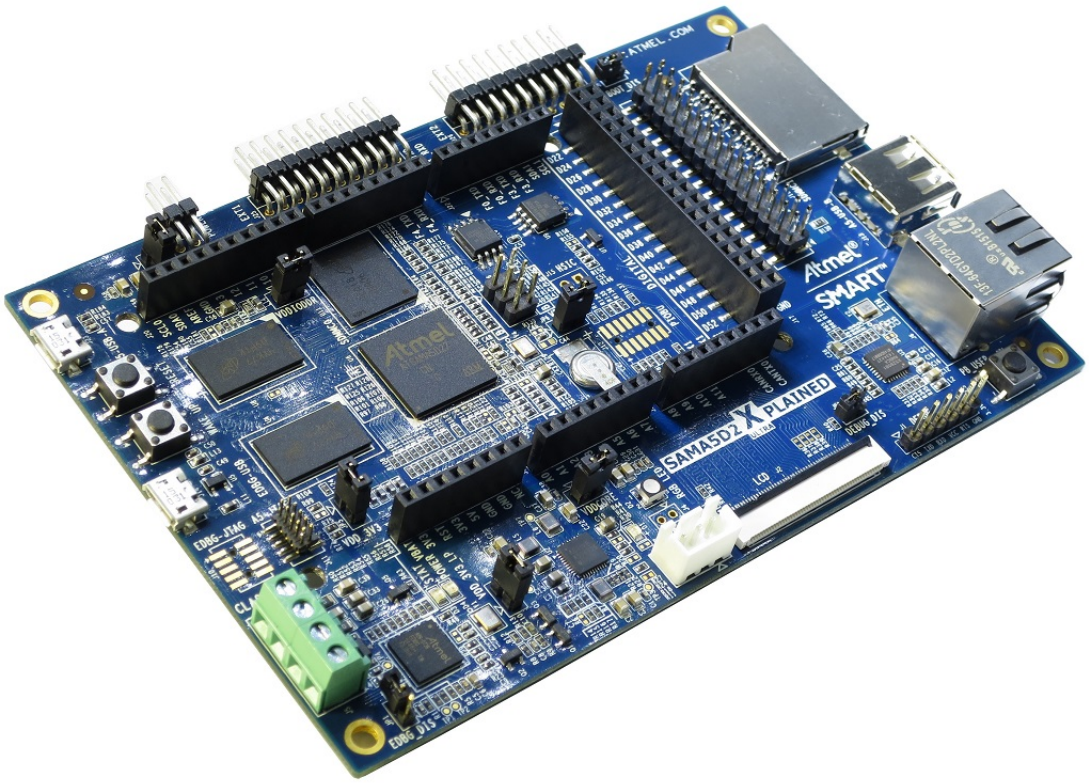
SAMA5D2C XULT

SAMA5D2C XULT User's Guide

Introduction



This user's guide introduces the Microchip SAMA5D2C Xplained Ultra evaluation kit (SAMA5D2C-XULT kit) and describes the development and debugging capabilities for applications running on the SAMA5D2 Arm® Cortex®-A5-based microprocessor unit (MPU). The SAMA5D2C-XULT kit supports the following part numbers:

- ATSAMA5D21C
- ATSAMA5D22C
- ATSAMA5D23C
- ATSAMA5D24C
- ATSAMA5D26C
- ATSAMA5D27C
- ATSAMA5D28C

Table of Contents

1. Kit Contents

The SAMA5D2C Xplained Ultra evaluation kit includes:

- One SAMA5D2C-XULT board
- One Micro-AB type USB cable

2. Evaluation Kit Specifications

Table 2-1. Evaluation Kit Specifications

Characteristic		Specifications
Board		SAMA5D2C-XULT
Part Number		ATSAMA5D2C-XULT
Board Supply Voltage		USB and/or Battery powered
Temperature	Operating	0°C to +70°C
	Storage	-40°C to +85°C
Relative Humidity		0 to 90% (non-condensing)
Main Board Dimensions (L x W x H)		135 × 88 × 20 mm
Board Identification		SAMA5D2 XPLAINED ULTRA

2.1 Electrostatic Warning

⚠WARNING ESD-Sensitive Electronic Equipment!
The evaluation kit is shipped in a protective anti-static package. The board system must not be subject to high electrostatic potentials.

We recommend using a grounding strap or similar ESD protective device when handling the board in hostile ESD environments (offices with synthetic carpet, for example). Avoid touching the component pins or any other metallic element on the board.

2.2 Power Supply Warning

⚠WARNING Hardware Power Supply Limitation
Powering the board with voltages higher than 5 VCC (e.g., the 12 VCC power adapters from other kits such as Arduino kits) may damage the board.

⚠WARNING Hardware Power Budget
Using the USB as the main power source (max. 500 mA) is acceptable only with the use of the on-board peripherals and low-power LCD extension.

When external peripheral or add-on boards need to be powered, we recommend the use of an external power adapter connected to the USB Micro-AB connectors (can provide up to 1.2A on the 3.3V node).

3. Board Power-Up

Three sources are available to power-up the SAMA5D2C-XULT board:

- USB-powered through the USB Micro-AB connector (J23 - default configuration)
- Powered through the USB Micro-AB connector on the Embedded Debugger (EDBG) interface (J14)
- Powered through a rechargeable battery Li-polymer 3.7V connected to J3 or J4

⚠WARNING Unlike Arduino Uno boards, the SAMA5D2C-XULT board runs at 3.3V. The maximum voltage that the I/O pins can tolerate is 3.3V. Providing higher voltages (e.g., 5V) to an I/O pin could damage the board.

The sequence for the initial power-up of the board is the following:

1. Unpack the board, taking care to avoid electrostatic discharge.
2. Connect the USB Micro-AB cable to the connector J23 (or J14).
3. Connect the other end of the cable to a free USB port of your PC.

Table 3-1. Electrical Characteristics

Parameter	Value
Input voltage	5 VCC
Maximum input voltage (limits)	6 VCC
Maximum DC 3.3V current available	1.2A
I/O voltage	3.3V only

4. Sample Code and Technical Support

After boot up, you can run sample code or your own application on the evaluation kit. Sample code and technical support is available on www.microchip.com. In particular, the software package (example source code and drivers) can be found on the “SAMA5D2 Software Package” page of our website.

Linux® software and demos can be found on www.at91.com/linux4sam/bin/view/Linux4SAM/.

⚠WARNING Make sure that the latest software version is downloaded before starting your evaluation. For more information, go to www.at91.com/linux4sam/bin/view/Linux4SAM/.

5. Hardware Overview

5.1 Introduction

The SAMA5D2C-XULT kit is a full-featured evaluation platform for the SAMA5D2 series ARM-based microprocessor units (MPU). It allows users to extensively evaluate, prototype and create application-specific designs.

5.2 Equipment List

The SAMA5D2C-XULT board is based on the integration of an ARM Cortex-A5-based microprocessor with external memory, one Ethernet physical layer transceiver, one SD/MMC interface, one host USB port and one device USB port, one 24-bit RGB LCD and debug interfaces.

Seven headers, compatible with Arduino R3 (Uno, Due) and two Xplained headers are available for various shield connections.

5.3 Board Features

Table 5-1. Board Specifications

Characteristics	Specifications
Dimensions (L x W x H)	135 x 88 x 20 mm
Processor	SAMA5D27C (289-ball BGA package), 14x14 mm body, 0.8 mm ball pitch
Oscillators	MPU, EDBG: 12 MHz crystal RTC: 32.768 kHz PHY: 25 MHz
Main memory	2 x DDR3L SDRAM 2 Gbit - 16 Mbit x 16 x 8 banks (total 4 Gbit = 512 Mbyte) 1 x eMMC NAND Flash 4 Gbit
Accessory memories	One Serial EEPROM SPI One QSPI Serial Flash One EEPROM with MAC Address and Serial Number
SD/MMC	One 4-bit SD card connector
USB	One USB Host with power switch One Micro-AB USB device
Display	One LCD interface connector, LCD TFT Controller with overlay, alpha-blending, rotation, scaling and color space conversion
Image sensor	One ISC interface and connector
Ethernet	One Ethernet PHY (RMII 10/100 MHz)
Debug port	One JTAG interface connector One EDBG interface with CDC One serial debug console interface (3.3V level)
Expansion connector	Arduino R3 compatible set of connectors XPRO set of connectors

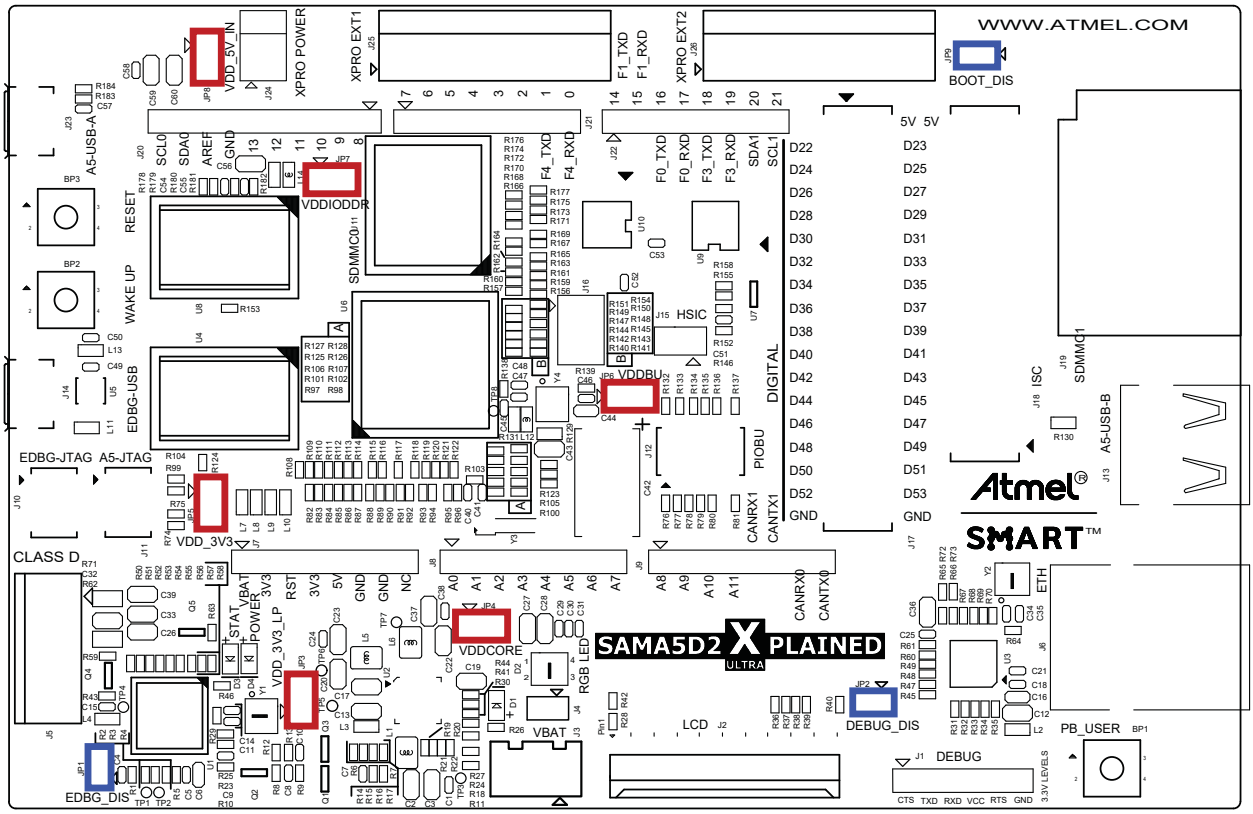
.....continued	
Characteristics	**Specifications**
Board supply voltage	5V from USB On-board power regulation by PMIC External battery-powered capability
Battery	On-board PowerCap
User interface	Reset, wake-up and user configurable push buttons One tri-color user LED (red, green, blue)

6. Board Components

6.1 Board Overview

The fully-featured SAMA5D2C-XULT board integrates multiple peripherals and interface connectors as shown in the figure below.

Figure 6-1. SAMA5D2C-XULT Board Overview



6.1.1 Default Jumper Settings

The board overview shows the default jumper settings. Blue jumpers are configuration items. Red jumpers are current measurement points. The table below describes the functionality of the jumpers.

Table 6-1. SAMA5D2C-XULT Jumper Settings

Jumper	Default	Function
JP1	OPEN	Disable EDBG
JP2	OPEN	Disable Debug
JP3	CLOSE	VDD_3V3_LP current measurement
JP4	CLOSE	VDDCORE current measurement
JP5	CLOSE	VDDISC + VDDIOP0/1/2 current measurement
JP6	CLOSE	VDDBU current measurement
JP7	CLOSE	VDDIODDR_MPU current measurement
JP8	CLOSE	VDD_5V_IN current measurement

.....continued		
Jumper	**Default**	**Function**
JP9	OPEN	Disable CS of SPI, QSPI and eMMC memories

6.2 Connectors On Board

The table below describes the interface connectors on the SAMA5D2C-XULT board.

Table 6-2. SAMA5D2C-XULT Board Interface Connectors

Connector	Interfaces to
J23	USB-A Device. Supports USB device using a type Micro-AB connector
J13	USB Host B. Supports USB host using a type A connector
J1	Serial DBGU (3.3V level)
J11	JTAG, 10-pin IDC connector
J14	EDBG USB connector
J15	USB-C™ (not populated)
J6	Ethernet
J2	Expansion connector with all LCD controller signals for display module connection (QTouch®, TFT LCD display with touchscreen and backlight)
J19	SDHCI SD/MMC connector
J3, J4	Battery connectors
J12	Tamper connector (not populated)
J7, J8, J9, J16, J17, J20, J21, J22	Expansion connectors with Arduino R3 compatible PIO signals
J24, J25, J26	Xplained Pro Expansion connectors
J10	EDBG JTAG (not populated)
J18	ISC interface
J5	Class-D amplifier output

6.3 Function Blocks

6.3.1 Processor

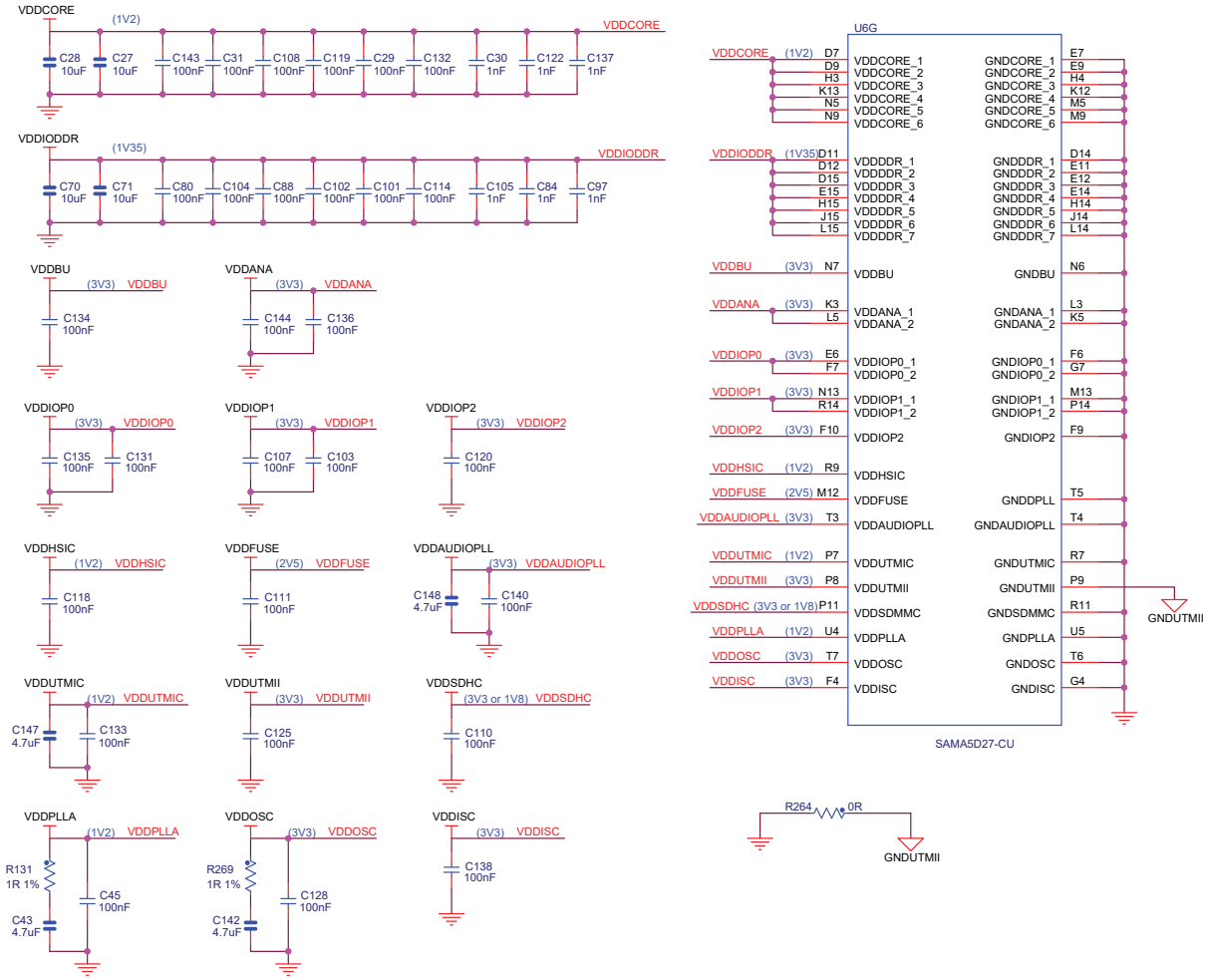
The SAMA5D2 Series is a high-performance, power-efficient MPU based on the ARM Cortex-A5 processor. Refer to the SAMA5D2 Series data sheet for more information.

6.3.2 Power Supply Topology and Power Distribution

6.3.2.1 Power Supplies

Detailed information on the device power supplies is provided in the tables “SAMA5D2 Power Supplies” and “Power Supply Connections” in the SAMA5D2 Series data sheet.

Figure 6-2. Processor Power Lines Supplies



6.3.2.2 Power-Up and Power-Down Considerations

Power-up and power-down considerations are described in section “Power Considerations” of the SAMA5D2 Series data sheet.

WARNING The power-up sequence provided in the SAMA5D2 Series data sheet must be respected for reliable operation.

6.3.2.3 ACT8945A Power Management IC

The ACT8945A is a complete, cost-effective and highly-efficient ActivePMU™ power management solution, optimized to provide a single-chip power solution and voltage sequencing for SAMA5D2/SAMA5D3/SAMA5D4 and SAM9 series MPUs. It also meets the control requirements of these devices.

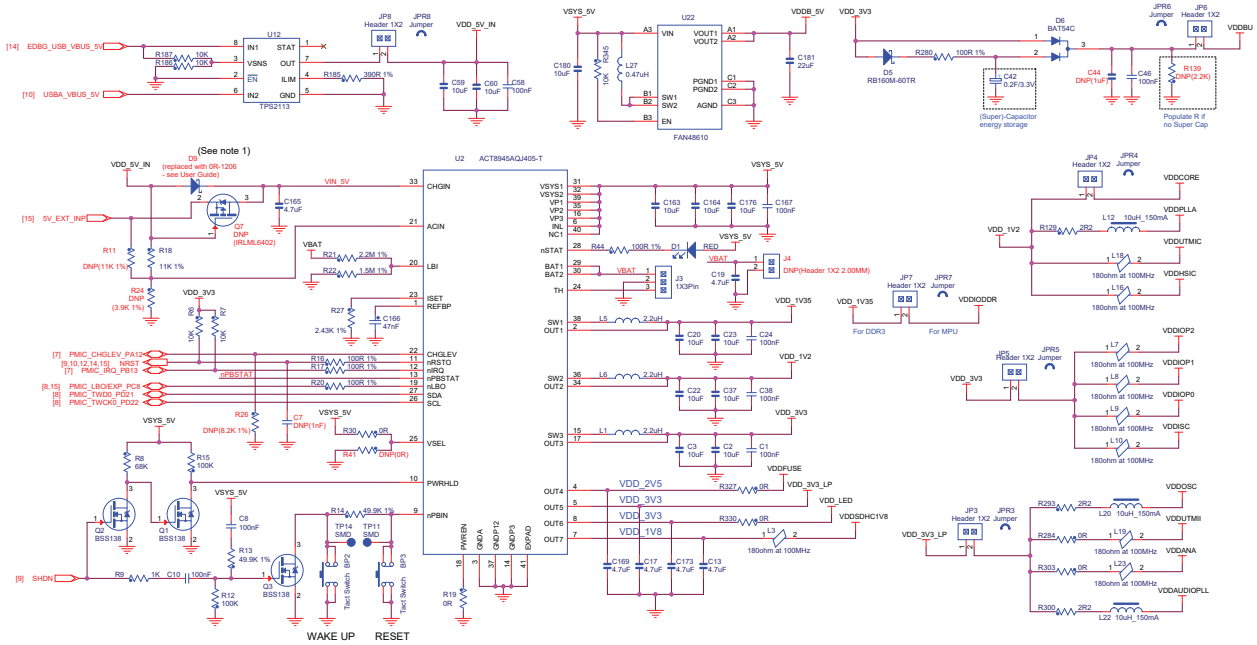
The ACT8945A features three step-down DC-DC converters and four low-noise, low-dropout linear regulators along with a complete battery charging solution featuring the advanced ActivePath™ system-power selection function.

WARNING Refer to the ACT8945A data sheet at www.active-semi.com/ for more details.

The three DC-DC converters utilize a high efficiency, fixed-frequency (2 MHz), current-mode PWM control architecture that requires a minimum number of external components. Two DC-DC converters are capable of

supplying up to 1100 mA of output current, while the third supports up to 1200 mA. All four low-dropout linear regulators are high performance, low-noise regulators that supply up to 320 mA of output current.

Figure 6-3. Board Power Management



Note: Occasional board start-up problems occurred when powered from a USB source with a weak VBUS level below 4.8V. To avoid the voltage drop and resulting start-up problems, production boards were assembled with a 0 Ω resistor in place of the Schottky diode D9 shown here.

6.3.2.3.1 Supply Group Configuration

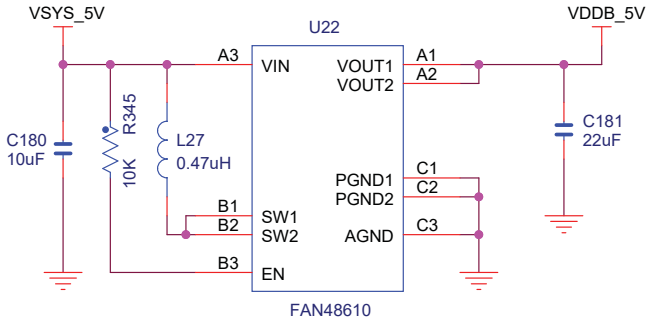
The ACT8945A provides:

- All power supplies required by the SAMA5D2 device:
  - 1.2V VDDCORE, VDDPLLA, VDDUTMIC, VDDHSIC
  - 1.35V VDDIODDR
  - 2.0V VDDBU
  - 3.3V VDDIOP, VDDISC
  - 1.8V or 3.3V VDDSDHC (= VDDSDMMC)
  - 2.5V VDDFUSE
  - 3.3V VDDOSC, VDDUTMII, VDDANA, VDDAUDIOPLL
- Power supplies to external chips on the main board:
  - 2.5V VDDLED
  - 4.8V VSYS_5V

6.3.2.4 Power Boost 5V

To generate a true 5V voltage from the PMIC output (4.8V typical), a FAN48610 low-power boost regulator is integrated into the design. This feeds the 5V USB host and the 5V LCD.

Figure 6-4. Power Boost 5V



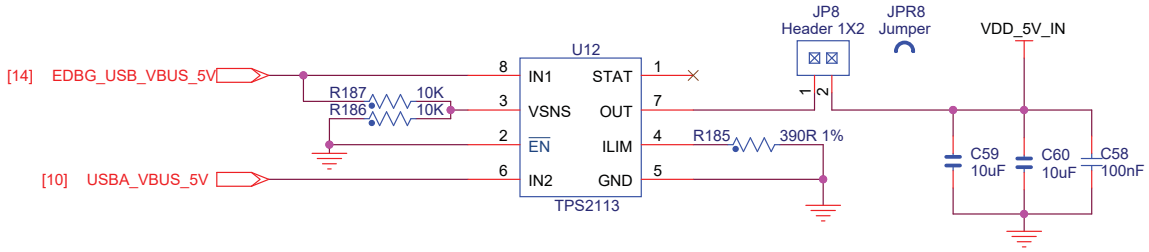
6.3.2.5 Input Power Options

There are several power options for the SAMA5D2C-XULT board.

USB-powered operation is the default configuration, where the USB device port is connected to a PC or a 5V DC supply. The USB supply is sufficient to power the board in most applications. It is important to note that when the USB supply is used, the USB-B Host port has limited power. If USB Host port is required for the application, it is recommended that an external DC supply be used.

The figure below provides the schematics of power options.

Figure 6-5. Input Powering Scheme



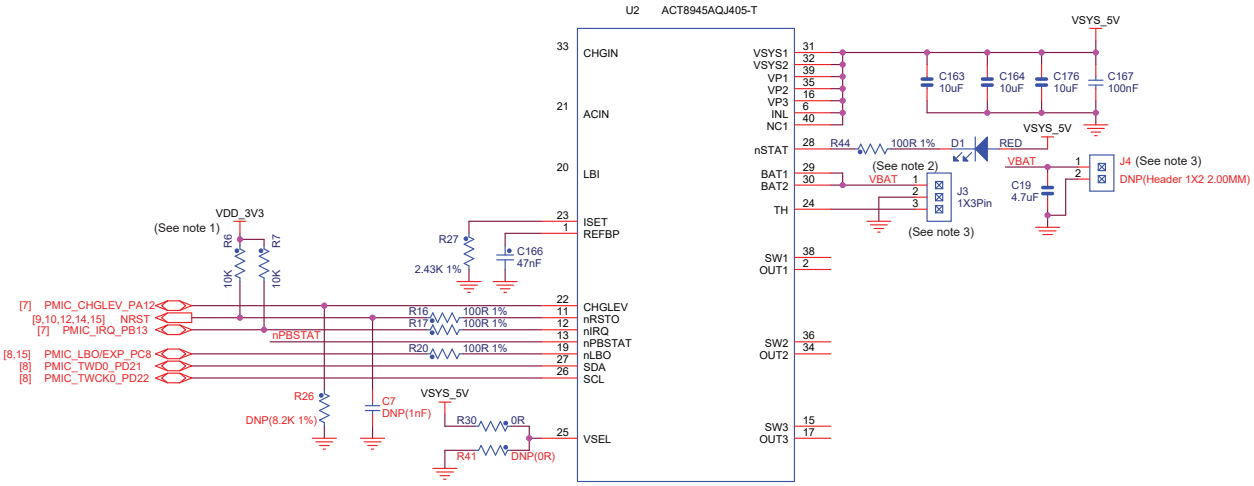
Note: USB-powered operation eliminates additional wires and batteries. It is the preferred mode of operation for any project that requires only a 5V source at up to 500 mA.

6.3.2.6 Battery Supply Source

The ACT8945A features an advanced battery charger that incorporates the ActivePath architecture for system power selection. This combination of circuits provides a complete, advanced battery-management system that automatically selects the best available input supply, manages charge current to ensure system power availability, and provides a complete, high accuracy (±0.5%), thermally regulated, full-featured single-cell linear Li+ charger.

The ActivePath circuitry monitors the state of the input supply, the battery, and the system, and automatically reconfigures itself to optimize the power system. If a valid input supply is present, ActivePath powers the system from the input while charging the battery in parallel. This allows the battery to charge as quickly as possible, while supplying the system. If a valid input supply is not present, ActivePath powers the system from the battery. Finally, if the input is present and the system current requirement exceeds the capability of the input supply, ActivePath allows system power to be drawn from both the battery and the input supply.

Figure 6-6. Battery Powering Scheme



Notes:

1. Refer to errata NRST.
2. If the battery does not have a pack embedded thermistor (i.e., battery temperature monitoring), the TH pin should be connected to ground => short J3 pins 2 and 3.
3. If no battery is connected on connector J3 or J4, it is recommended that the charging function be disabled in the ACT8945 chip. To do so, write the SUSCHG bit to '1' in APCH register (REG 0x71, SUSCHG = 1).

6.3.2.6.1 Charger Input Interrupts

To facilitate input supply detection and eliminate the size and cost of external detection circuitry, the charger has the ability to generate interrupts based upon the status of the input supply. This function is capable of generating an interrupt when the input is connected, disconnected, or both, when the charger state machine transitions.

6.3.2.6.2 Charge Status Indicator

The charger provides a charge-status indicator output, nSTAT. nSTAT is an open-drain output which sinks current when the charger is in an active-charging state, and is high-Z otherwise. nSTAT features an internal 8 mA current limit, and is capable of directly driving an LED (D1).

6.3.2.6.3 Precision Voltage Detector

The low battery input (LBI) connects to one input of a precision voltage comparator, which can be used to monitor a system voltage such as the battery voltage. An external resistive-divider network can be used to set voltage monitoring thresholds. The output of the comparator is present at the open-drain low battery indicator output (nLBO) and connected to the red LED D1.

Table 6-3. PIOs Used to Control the Battery Charger

PIO	Function
PA12	CHGLEV: Charge Current Selection Input
PB13	nIRQ: Open-Drain Interrupt Output. nIRQ is asserted any time an unmasked fault condition exists or a charger interrupt occurs.
PC8	nLBO: Low Battery Indicator Output. nLBO is asserted low whenever the voltage at LBI is lower than1.2V; it is high-Z otherwise.

Figure 6-7. Battery Connector J3 and Optional J4

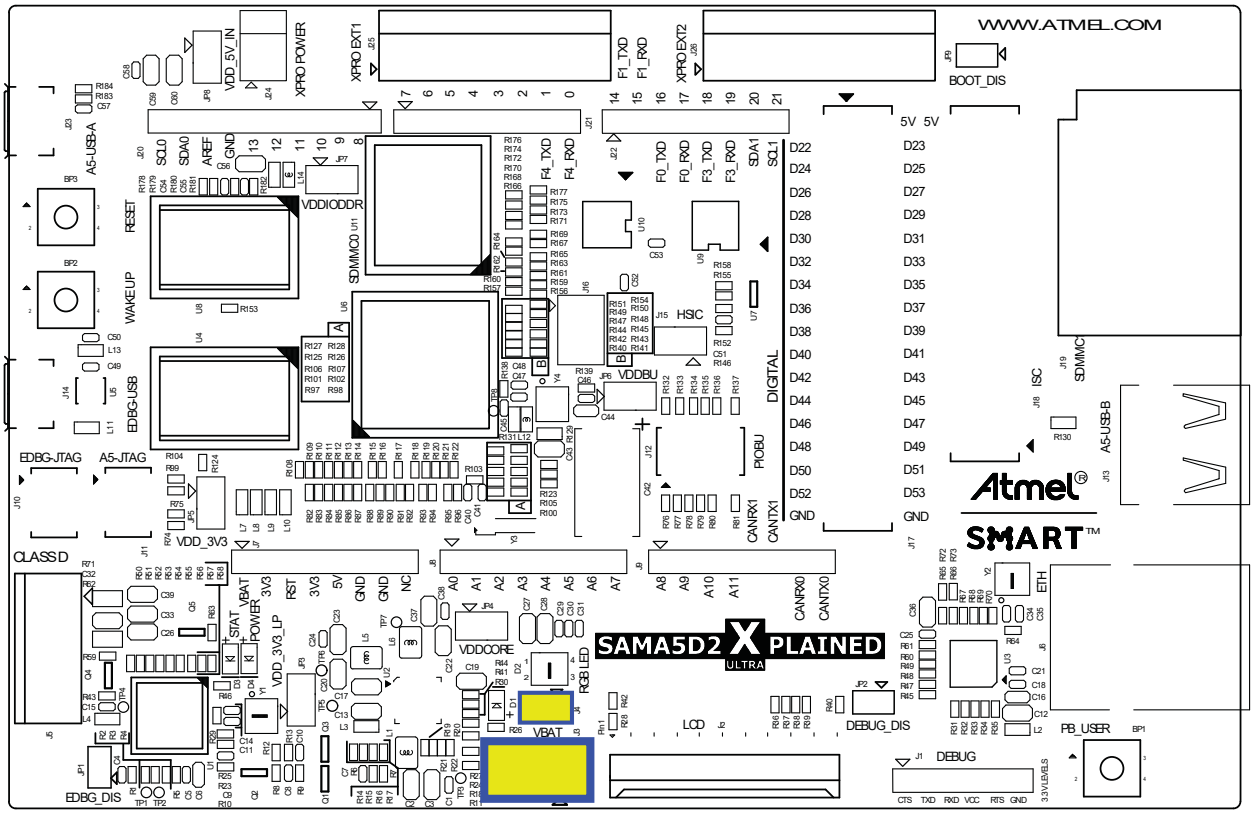


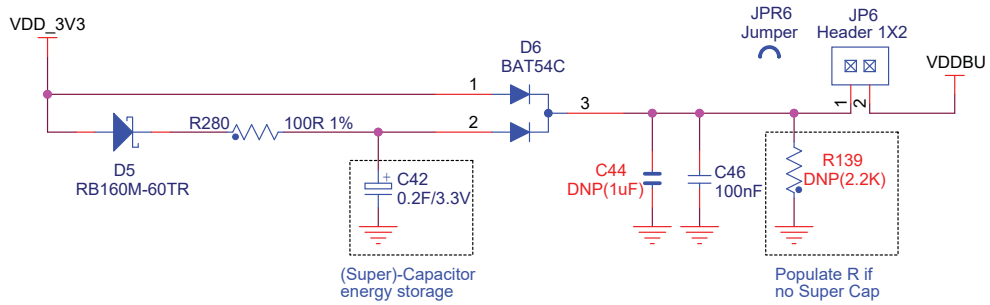
Table 6-4. Battery J3 Signal Descriptions

Pin	Mnemonic	Signal Description
1	VBAT	Battery I/O (exploitation and charging). Connect this pin directly to the battery anode (+ terminal)
2	GND	Common ground
3	TH	Temperature Sensing Input. Connect to battery thermistor. TH is pulled up with a 102 µA (typical) current internally.

6.3.2.7 Backup Power Supply

The SAMA5D2C-XULT board requires a power source to permanently power the backup part of the SAMA5D2 device (refer to the SAMA5D2 Series data sheet). A super capacitor sustains such permanent power to VDDBU when all system power sources are off.

Figure 6-8. VDDBU Powering Scheme Option



6.3.2.8 Power Supply Control

In the ACT8945A, three DC-DC converters (1.8V, 1.2V, 3.3V) and two LDO outputs are available.

All ACT8945A outputs can be controlled by the TWI interface through software.

The three DC-DC outputs can be enabled or disabled by the SAMA5D2 SHDN output:

- SHDN = 0: The DC-DC output is disabled.
- SHDN = 1: The DC-DC output is enabled.

Two push buttons are also available:

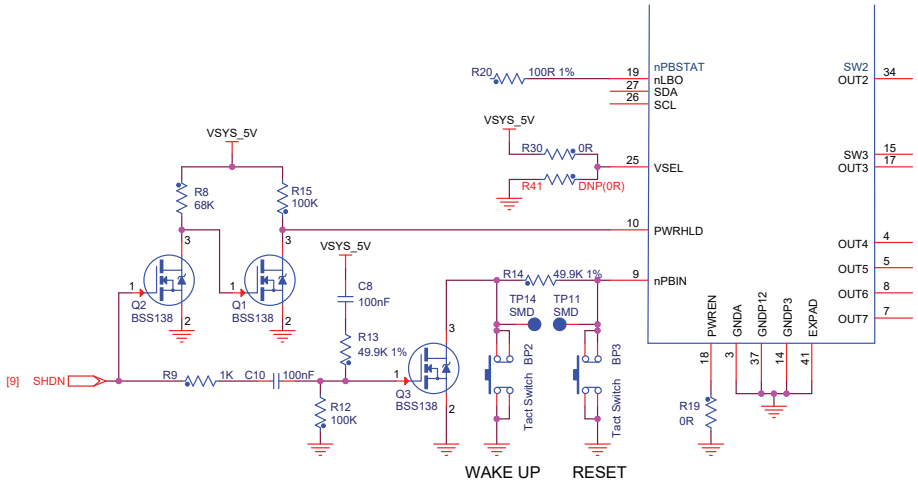
- Wake-up push button: When pressed, the ACT8945A power outputs are restarted if the ACT8945A is in Shutdown mode.
- Reset push button: When pressed, the ACT8945A transfers the reset signal to the MPU.

6.3.3 Reset Circuitry

The reset sources for the SAMA5D2C-XULT board are:

- Power-on Reset from the Power Management Unit (PMIC)
- Push button reset BP3
- External reset from Arduino connectors
- JTAG or EDBG reset from an in-circuit emulator

Figure 6-9. Reset/Wake-up and Shutdown Control

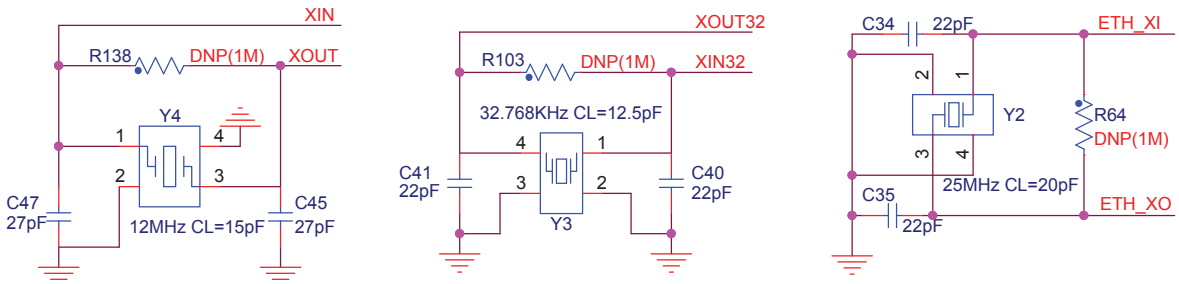


6.3.4 Clock Circuitry

The SAMA5D2C-XULT board includes four clock sources:

- Two clocks are alternatives for the SAMA5D2 processor (12 MHz, 32 kHz)
- One crystal oscillator used for the Ethernet RMII chip (25 MHz)
- One crystal oscillator used for the EDBG (12 MHz)

Figure 6-10. Clock Circuitry



6.3.5 Memory

6.3.5.1 Memory Organization

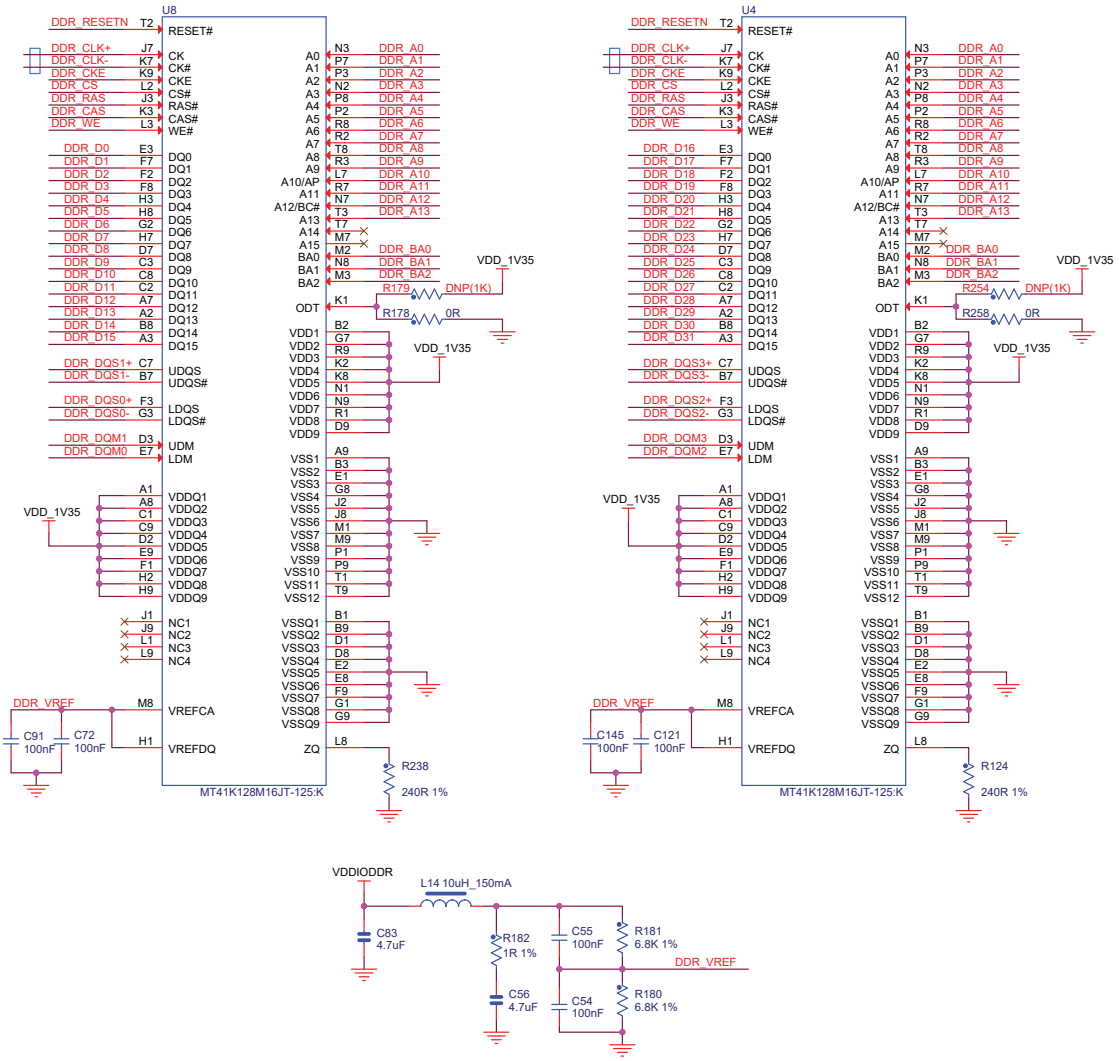
The SAMA5D2 features a DDR/SDR memory interface and an External Bus Interface (EBI) to allow interfacing to a wide range of external memories and to almost any kind of parallel peripheral.

This section describes the memory devices that equip the SAMA5D2C-XULT board.

6.3.5.2 DDR3/SDRAM

Two DDR3L/SDRAM (MT41H128M16JT-125-K - 2 Gbit = 16 Mbit x 16 x 8 banks) are used as main system memory and total 4 Gbit of SDRAM on the board. The memory bus is 32 bits wide and operates with a frequency of up to 166 MHz.

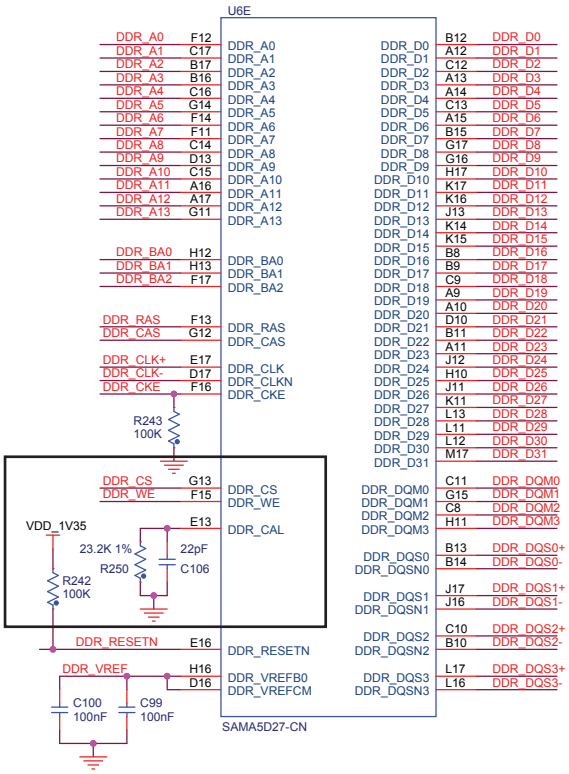
Figure 6-11. DDR3L



6.3.5.3 DDR_CAL Analog Input

One specific analog input, DDR_CAL, is used to calibrate all DDR I/Os.

Figure 6-12. DDR Signals and CAL Analog Input



6.3.5.4 eMMC

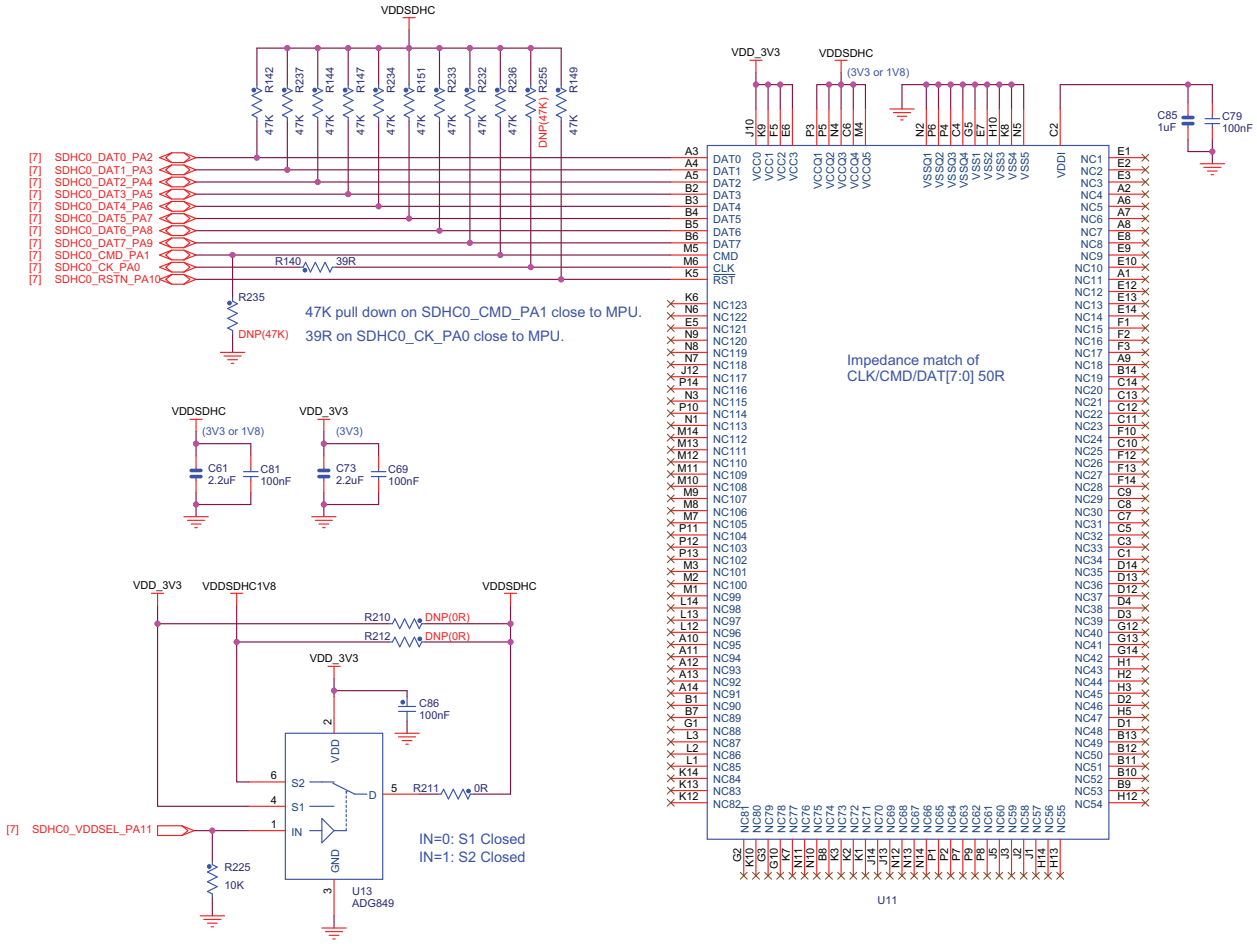
The Secure Digital Multimedia Card (SDMMC) Controller supports the Embedded MultiMedia Card (e.MMC) Specification V4.41, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 specification

One MTFC4GACAJCN-4M 4 Gb eMMC is connected to the processor through the SDMMC0 port.

Table 6-5. SDMMC Reference Documents

Name	Link
SD Host Controller Simplified Specification V3.00	www.sdcard.org
SDIO Simplified Specification V3.00	www.sdcard.org
Physical Layer Simplified Specification V3.01	www.sdcard.org
Embedded MultiMedia Card (e.MMC) Electrical Standard 4.51	www.jedec.org

Figure 6-13. eMMC



6.3.5.5 CS Disable

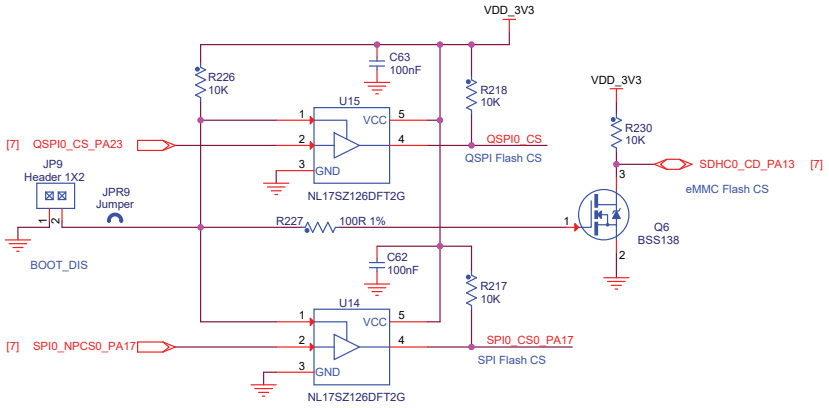
The SAMA5D2 device boots according to the following sequence:

1. SD CARD connected on SDHC1
2. eMMC connected on SDHC0
3. Serial Flash connected on SPI0_IOSET1 (Chip Select 0: NPCS0)
4. Optional QSPI Flash connected on QSPI0_IOSET3 (Chip Select 0: CS0)

In this sequence, the first device found with bootable contents is selected as the boot source. The others are disregarded. (see **Note** below)

An on-board jumper (JP9) controls the selection (CS#) of the on-board bootable memory components (eMMC and Serial Flash) using a non-inverting 3-state buffer.

Figure 6-14. CS Disable



The rule of operation is:

- JP9 = OFF (default) → enable normal boot from serial Flash memories mounted on board
- JP9 = ON → booting from optional serial Flash memories is disabled

Refer to the SAMA5D2 Series data sheet for more information on standard boot strategies and sequencing.

Note: The errata in the SAMA5D2 data sheet state that booting from SD/MMC devices is nondeterministic. In order to have a known behavior regardless of SD/MMC data contents, we recommend SDMMC0/SDMMC1 boot bits be disabled in the Boot Configuration Word fuse.

6.3.6 Additional Memories

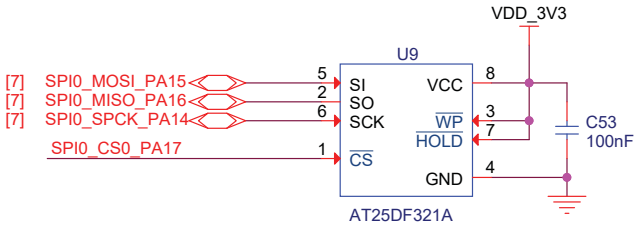
6.3.6.1 Serial Flash

The SAMA5D2 provides two high-speed Serial Peripheral Interface (SPI) controllers. One port is used to interface with the on-board serial serial Flash.

The four main signals used in the SPI are Clock, Data In, Data Out, and Chip Select. The SPI is a serial interface similar to the I^2C bus interface but with three main differences:

- It operates at a higher speed.
- Transmit and receive data lines are separate.
- Device access is chip select-based instead of address-based.

Figure 6-15. Serial Flash



6.3.6.2 QSPI Serial Flash

The SAMA5D2 provides two Quad Serial Peripheral Interfaces (QSPI). One port is used to interface with the optional on-board QSPI serial Flash.

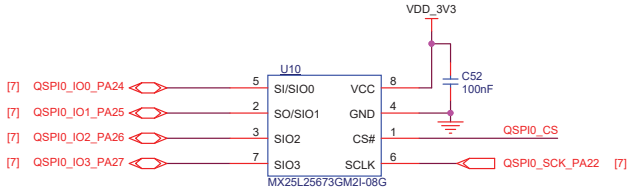
The Quad SPI Interface (QSPI) is a synchronous serial data link that provides communication with external devices in Master mode.

The QSPI can be used in SPI mode to interface to serial peripherals (such as ADCs, DACs, LCD controllers, CAN controllers and sensors), or in Serial Memory mode to interface to serial Flash memories.

The QSPI allows the system to execute code directly from a serial Flash memory (XIP) without code shadowing to RAM. The serial Flash memory mapping is seen in the system as other memories (ROM, SRAM, DRAM, embedded Flash memory, etc.).

With the support of the Quad SPI protocol, the QSPI allows the system to use high-performance serial Flash memories which are small and inexpensive, in place of larger and more expensive parallel Flash memories.

Figure 6-16. QSPI Serial Flash



6.3.6.3 Serial EEPROM with Unique MAC Address

The SAMA5D2C-XULT board embeds one Microchip AT24MAC402/602 EEPROM using a TWI1 interface.

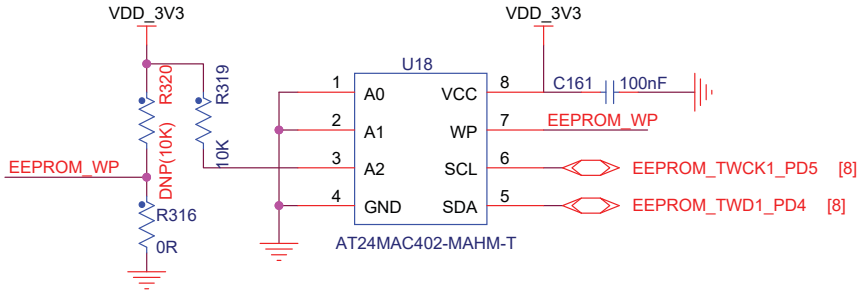
The AT24MAC402/602 provides 2048 bits of Serial Electrically-Erasable Programmable Read-Only Memory (EEPROM) organized as 256 words of eight bits each and is accessed via an I^2C-compatible (2-wire) serial interface. In addition, the AT24MAC402/602 incorporates an easy and inexpensive method to obtain a globally unique MAC or EUI address (EUI-48 or EUI-64).

The EUI-48/64 addresses can be assigned as the actual physical address of a system hardware device or node, or it can be assigned to a software instance. These addresses are factory-programmed by Microchip and guaranteed unique. They are permanently write-protected in an extended memory block located outside of the standard 2-Kbit memory array.

In addition, the AT24MAC402/602 provides the value-added feature of a factory-programmed, also guaranteed unique 128-bit serial number located in the extended memory block (same area as the EUI address values).

⚠WARNING The EEPROM device is also used as a “software label” to store board information such as chip type, manufacturer name and production date, using the last two 16-byte blocks in memory. **To preserve the ease of board identification by software, the information contained in these blocks should not be modified.**

Figure 6-17. EEPROM



6.4 PIO Usage and Interface Connectors

6.4.1 Secure Digital Multimedia Card Interface

6.4.1.1 Secure Digital Multimedia Card Controller (SDMMC)

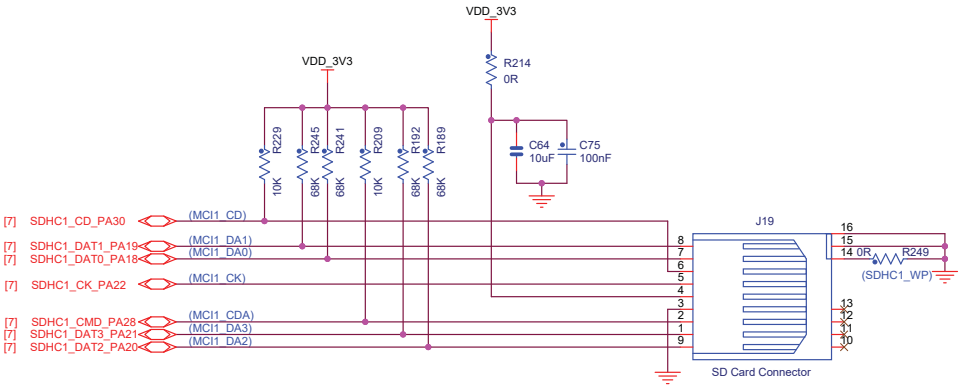
The SAMA5D2C-XULT board has two SDMMC interfaces that support the MultiMedia Card (e.MMC) Specification V4.41, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 specification.

- SDMMC0 interface is connected to the eMMC.
- SDMMC1 Interface based on a 7-pin interface (clock, command, 4-bit data, power lines).

6.4.1.2 SDMMC1 Card Connector

A standard MMC/SD card connector, connected to SDMMC1, is mounted on the top side of the board. It includes a card detection switch.

Figure 6-18. SDMMC1



Note: Refer to details on SDcard boot in CS Disable.

Standard SD Socket J19

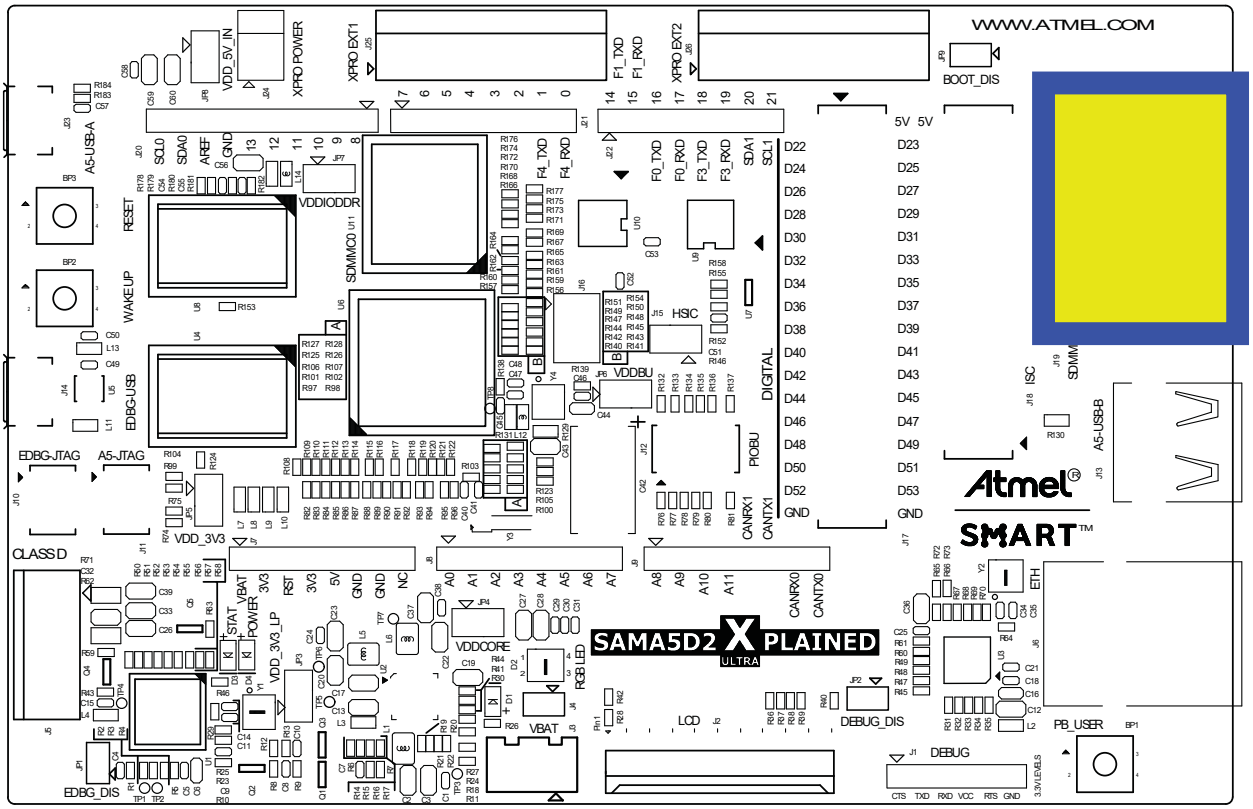


Table 6-6. Standard SD Socket J19 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	DAT3	PA21	Data Bit 3
2	CDA	PA28	Command Line
3	GND	–	Common ground
4	VCC	–	Supply Voltage 3.3V

.....continued			
Pin	**Mnemonic**	**PIO**	**Signal Description**
5	CLK	PA22	Clock / Command Line
6	CD	PA30	Card Detect
7	DAT0	PA18	Data Bit 0
8	DAT1	PA19	Data Bit 1
9	DAT2	PA20	Data Bit 2
10	GND	–	Common ground

6.4.2 Communication Interfaces

The SAMA5D2C-XULT board is equipped with GMAC and USB Host/Device communication interfaces.

6.4.2.1 Ethernet 10/100 (GMAC) Port

The SAMA5D2C-XULT board contains a MICREL PHY device (KSZ8081) operating at 10/100 Mb/s. The board supports RMII interface modes. The Ethernet interface consists of two pairs of low-voltage differential pair signals designated from GRX± and GTX± plus control signals for link activity indicators. These signals can be used to connect to a 10/100 Base-T RJ45 connector integrated on the SAMA5D2C-XULT board.

Additionally, for monitoring and control purposes, LED functionality is carried on the RJ45 connectors to indicate activity, link, and speed status information.

For more information about the Ethernet controller device, refer to the MICREL KSZ8081RN controller data sheet.

Figure 6-19. Ethernet (GMAC)

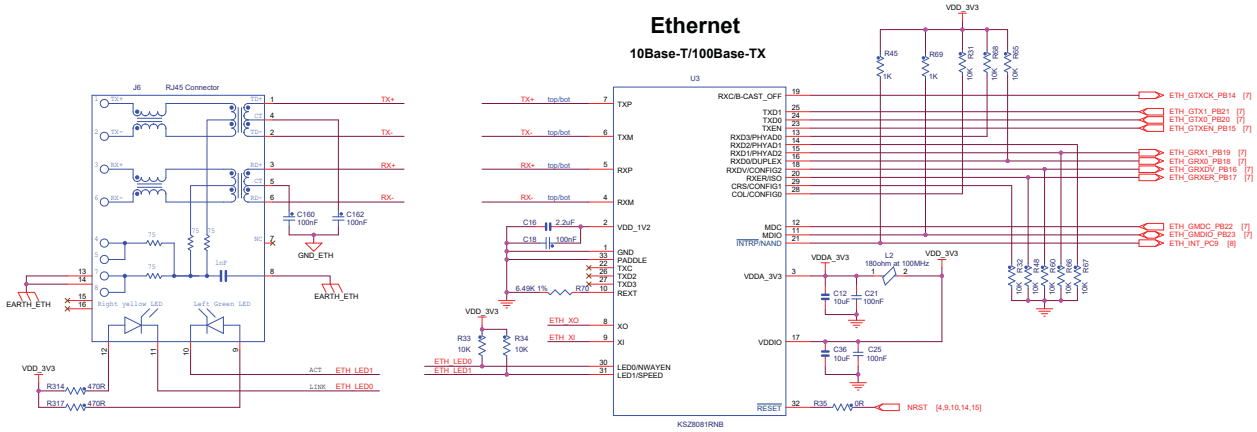


Figure 6-20. ETH RJ45 Connector J6

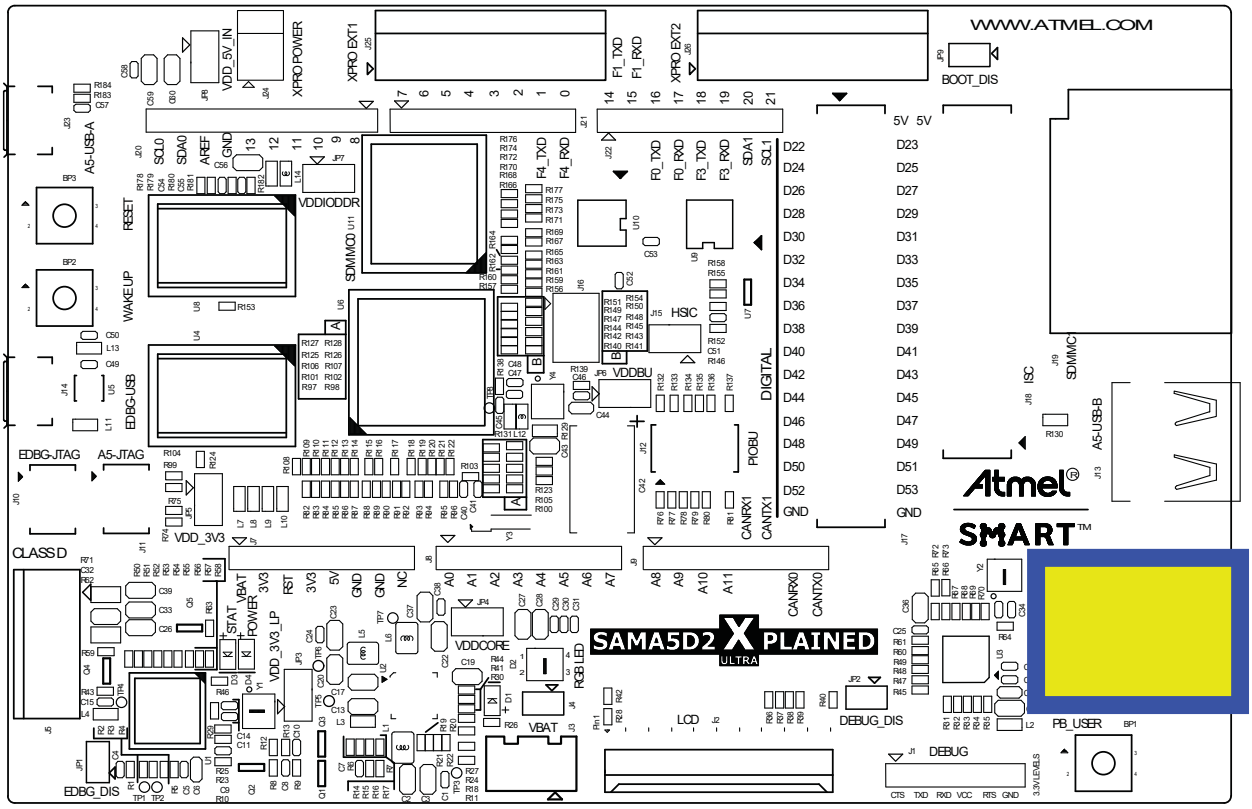


Table 6-7. ETH RJ45 Connector Signal Descriptions

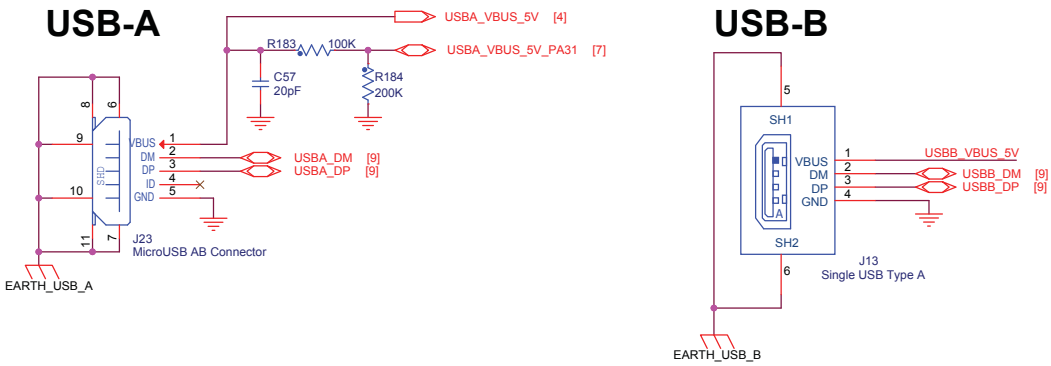
Pin	Mnemonic	Signal Description
1	TX+	Transmit
2	TX-	Transmit
3	RX+	Receive
4	Decoupling capacitor	–
5	Decoupling capacitor	–
6	RX-	Receive
7	NC	–
8	EARTH / GND	Common ground
9	ACT LED	LED activity
10	ACT LED	LED activity
11	LINK LED	LED link connection
12	LINK LED	LED link connection
13	EARTH / GND	Common ground
14	EARTH / GND	Common ground
15	NC	–
16	NC	–

6.4.2.2 USB Host/Device A, B

The SAMA5D2C-XULT board features three USB communication ports:

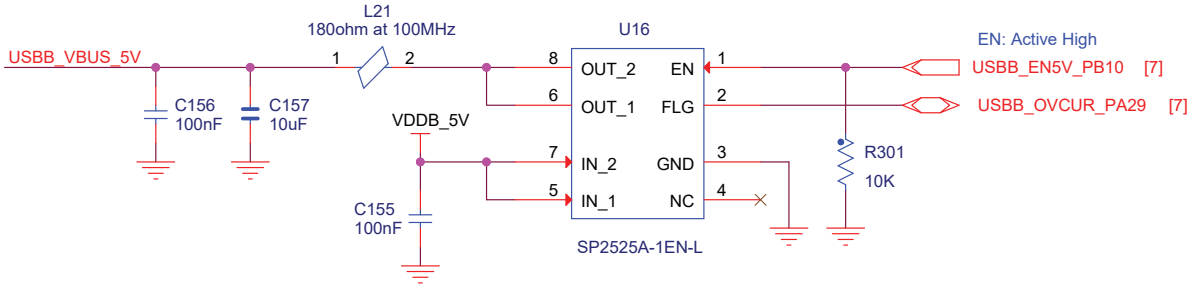
- USB-B Host High- and Full-speed Interface
  - One USB host type A connector
- USB-A Device Interface
  - One USB device standard Micro-AB connector. This port has a VBUS detection function made through the resistor ladder R183 and R184.
- UBC-C High-speed Host Port
  - One USB high-speed host port with a High-Speed Inter-Chip (HSIC) interface. This port is connected to a single 2-pin jumper.

Figure 6-21. USB-B Host & USB-A Device Interface



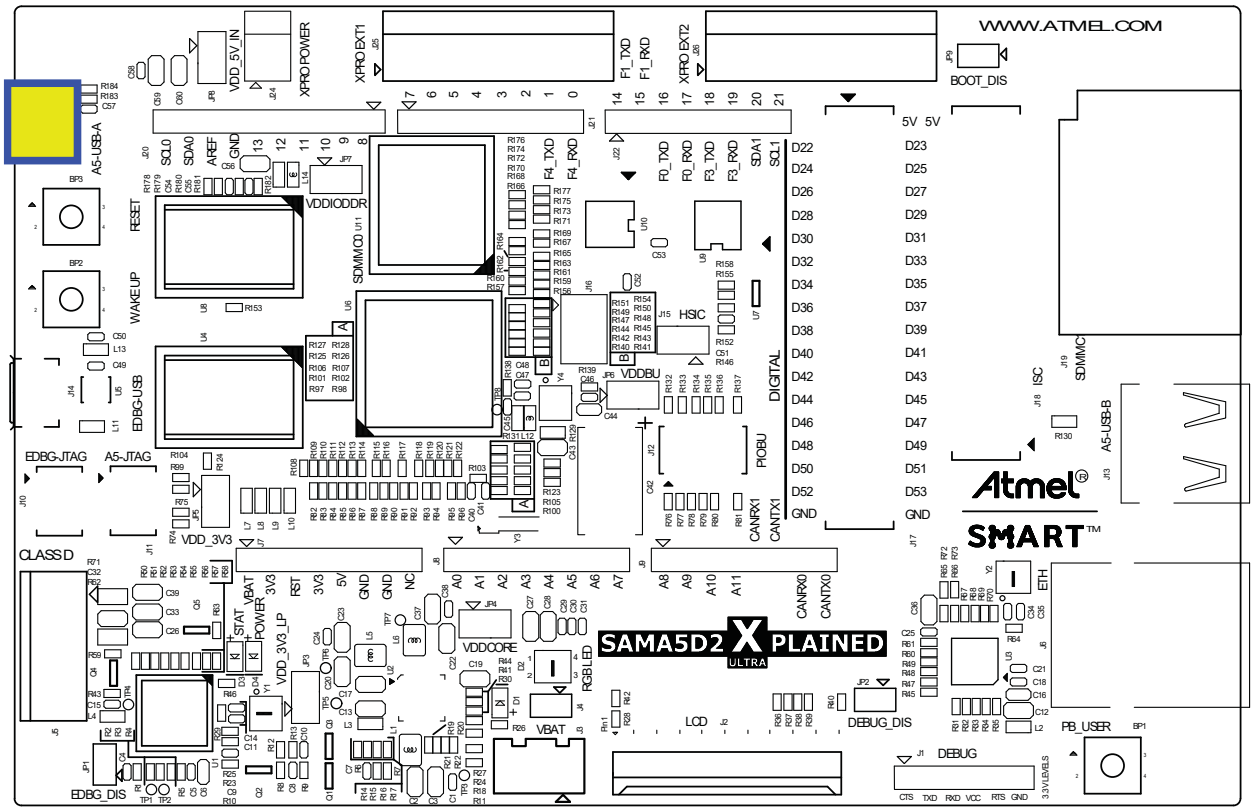
The USB-B Host port is equipped with 500 mA high-side power switch for self-powered and bus-powered applications.

Figure 6-22. USB Power Switch



6.4.3 USB-A Micro-AB Connector J23

Figure 6-23. USB-A Connector J23



6.4.4 USB-B Type B Connector J13

The USB-B host port A (J13) features a VBUS insert detection function through the ladder-type resistors R26 and R27.

Figure 6-24. USB B Connector J13

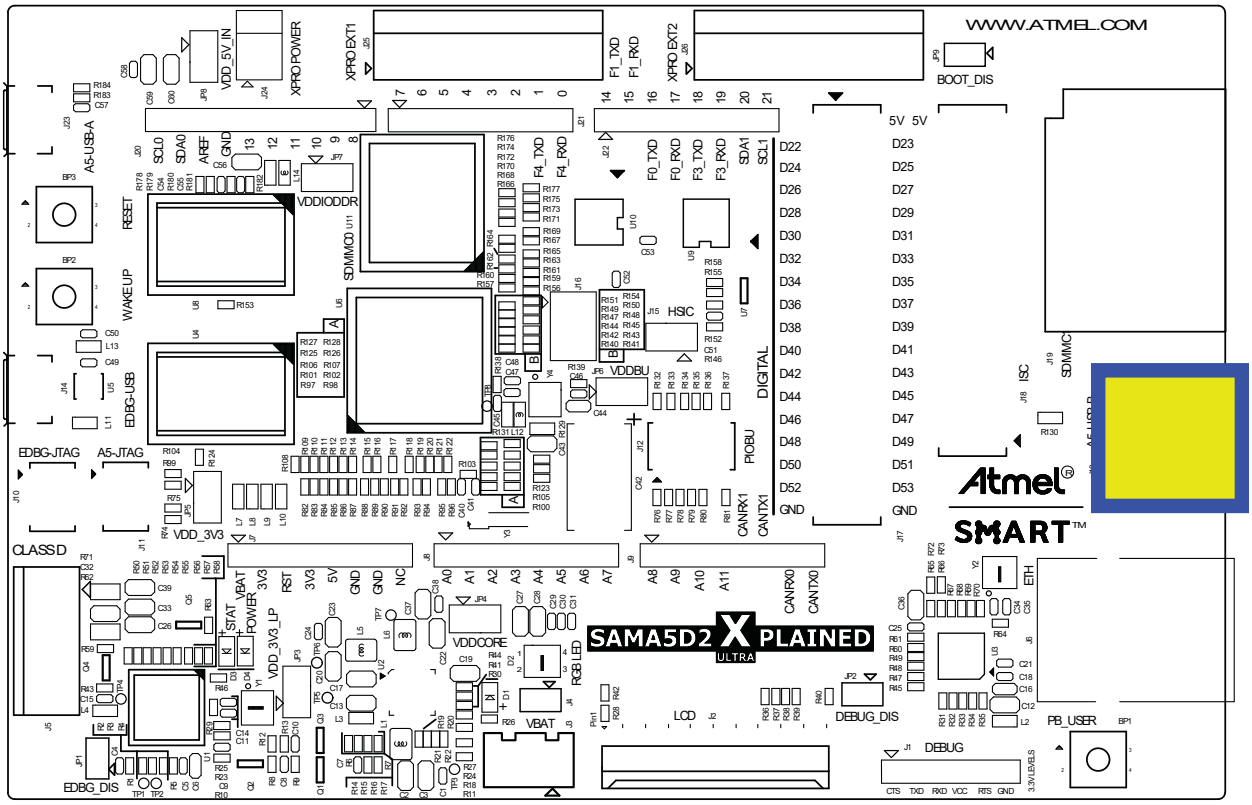


Table 6-8. USB-A & USB-B Connector Signal Descriptions

Pin	Mnemonic	Signal Description
1	VBUS	5V power
2	DM	Data minus
3	DP	Data plus
4	ID	On-the-go identification
5	GND	Common ground

6.4.5 LCD TFT Interface

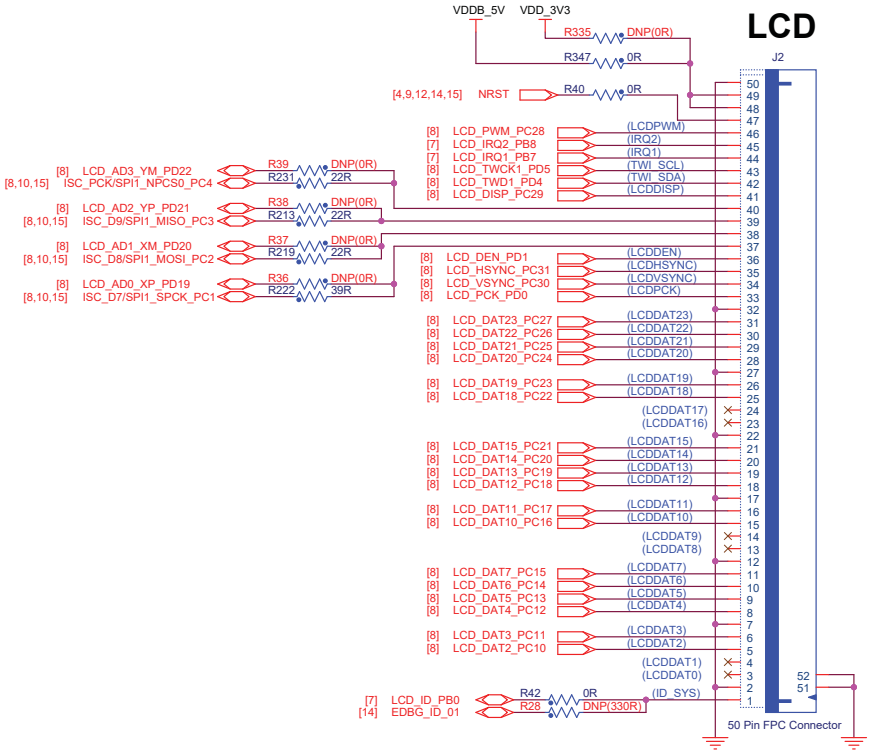
6.4.5.1 LCD

The SAMA5D2C-XULT board provides 18 bits of data and control signals to the LCD interface. Other signals are used to control the LCD and are available on connector J2: TWI, SPI, two GPIOs for interrupt, 1-Wire and power supply lines.

6.4.5.2 LCD Expansion Header

J2 is a 1.27mm pitch 50-pin header. It gives access to the LCD signals.

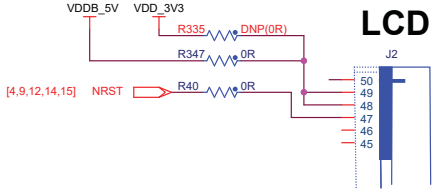
Figure 6-25. LCD Expansion Header Interface Schematic



6.4.5.3 LCD Power

In order to operate correctly out of the processor with various LCD modules, two voltage lines are available: 3.3V and 5 VCC (default), both selected by 0R resistors R335 and R347.

Figure 6-26. LCD Power



6.4.5.4 LCD Connector J2

Figure 6-27. LCD Connector J2

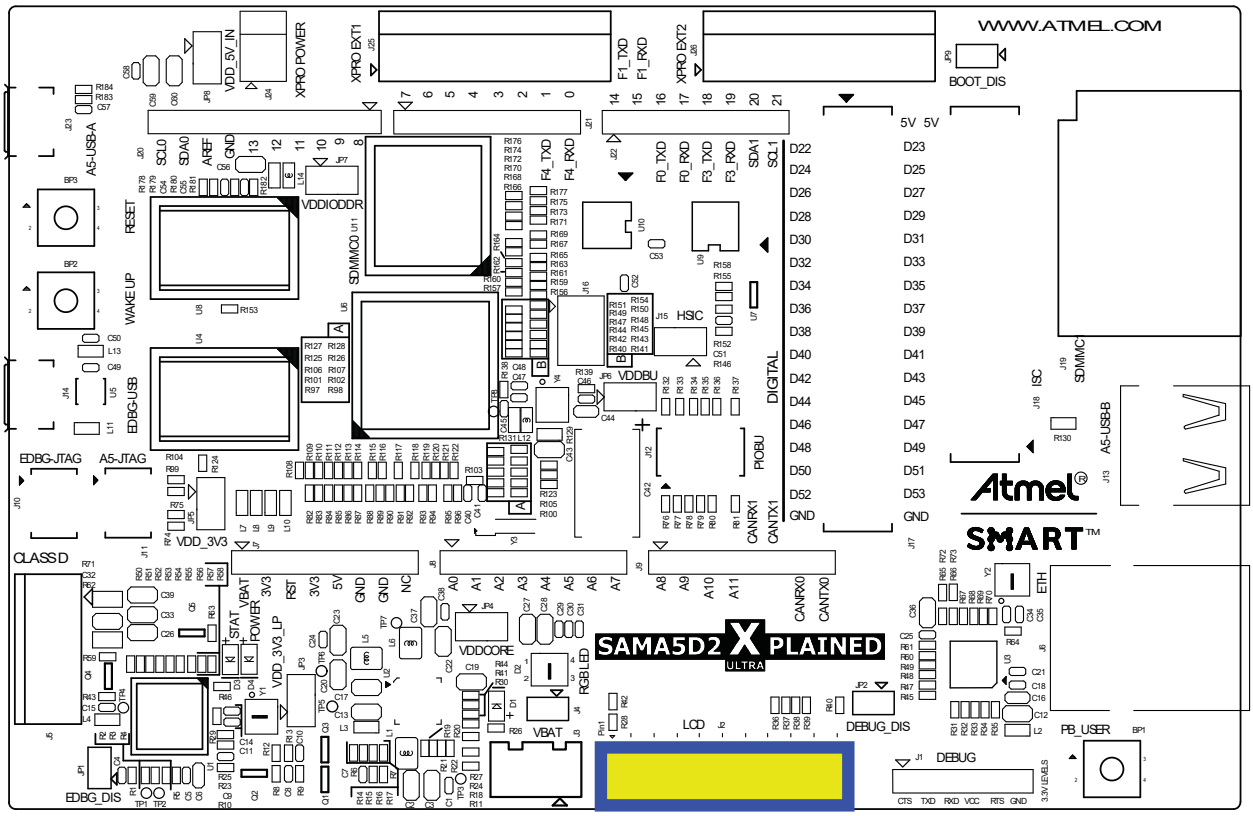


Table 6-9. LCD Connector J2 Signal Descriptions

Pin	Signal	PIO	Signal	RGB Interface Function	Alternate
1	ID_SYS	PB0/ ID00	ID	Extension module identification	EDBG_ID_01
2	–	GND	GND	GND	–
3	–	–	–	–	–
4	–	–	–	–	–
5	LCDDAT2	PC10	D2	Data line	–
6	LCDDAT3	PC11	D3	Data line	–
7	–	GND	GND	GND	–
8	LCDDAT4	PC12	D4	Data line	–
9	LCDDAT5	PC13	D5	Data line	–
10	LCDDAT6	PC14	D6	Data line	–
11	LCDDAT7	PC15	D7	Data line	–
12	–	GND	GND	GND	–
13	–	–	–	–	–
14	–	–	–	–	–
15	LCDDAT10	PC16	D10	Data line	–

.....continued

Pin	Signal	PIO	Signal	RGB Interface Function	Alternate	
16	LCDDAT11	PC17	D11	Data line	–	
17	–	GND	GND	GND	–	
18	LCDDAT12	PC18	D12	Data line	–	
19	LCDDAT13	PC19	D13	Data line	–	
20	LCDDAT14	PC20	D14	Data line	–	
21	LCDDAT15	PC21	D15	Data line	–	
22	–	GND	GND	GND	–	
23	–	–	–	–	–	
24	–	–	–	–	–	
25	LCDDAT18	PC22	D18	Data line	–	
26	LCDDAT19	PC23	D19	Data line	–	
27	–	GND	GND	GND	–	
28	LCDDAT20	PC24	D20	Data line	–	
29	LCDDAT21	PC25	D21	Data line	–	
30	LCDDAT22	PE26	D22	Data line	–	
31	LCDDAT23	PE27	D23	Data line	–	
32	–	GND	GND	GND	–	
33	LCDPCK	PD0	PCLK	Pixel clock	–	
34	LCDVSYNC	PC30	VSYNC/CS	Vertical synchronization	–	
35	LCDHSYNC	PC31	HSYNC/WE	Horizontal synchronization	–	
36	LCDDEN	PD1	DATA_ENABLE/RE	Data enable	–	
37	SPI1_SPCK	PC1	SPI_SCK	–	AD3/YM	PD22
38	SPI1_MOSI	PC2	SPI_MOSI	–	AD2/YP	PD21
39	SPI1_MISO	PC3	SPI_MISO	–	AD1/XM	PD20
40	SPI1_NPCS0	PC4	SPI_CS	–	AD0/XP	PD19
41	LCDDISP	PA29	ENABLE	Display enable signal	–	
42	TWD1	PD4	TWI_SDA	I2C data line (maXTouch®)	–	
43	TWCK1	PD5	TWI_SCL	I2C clock line (maXTouch)	–	
44	GPIO	PB7	IRQ1	maXTouch interrupt line	–	
45	GPIO	PB8	IRQ2	Interrupt line for other I2C devices	–	
46	LCDPWM	PC28	PWM	Backlight control	–	
47	RESET	–	RESET	Reset for both display and maXTouch	–	
48	Main_5V/3V3	VCC	VCC	3.3V or 5V supply (0R)	–	
49	Main_5V/3V3	VCC	VCC	3.3V or 5V supply (0R)	–	
50	GND	GND	GND	GND	–	

6.4.6 ISC

The Image Sensor Controller (ISC) system manages incoming data from a parallel or serial csi-2 based CMOS/CCD sensor. It supports a single active interface. It supports the ITU-R BT 656/1120 422 protocol with a data width of 8 bits or 10 bits and raw Bayer format. The internal image processor includes adjustable white balance, color filter array interpolation, color correction, gamma correction, 12-bit to 10-bit compression, programmable color space conversion, horizontal and vertical chrominance subsampling module.

Figure 6-28. ISC J18

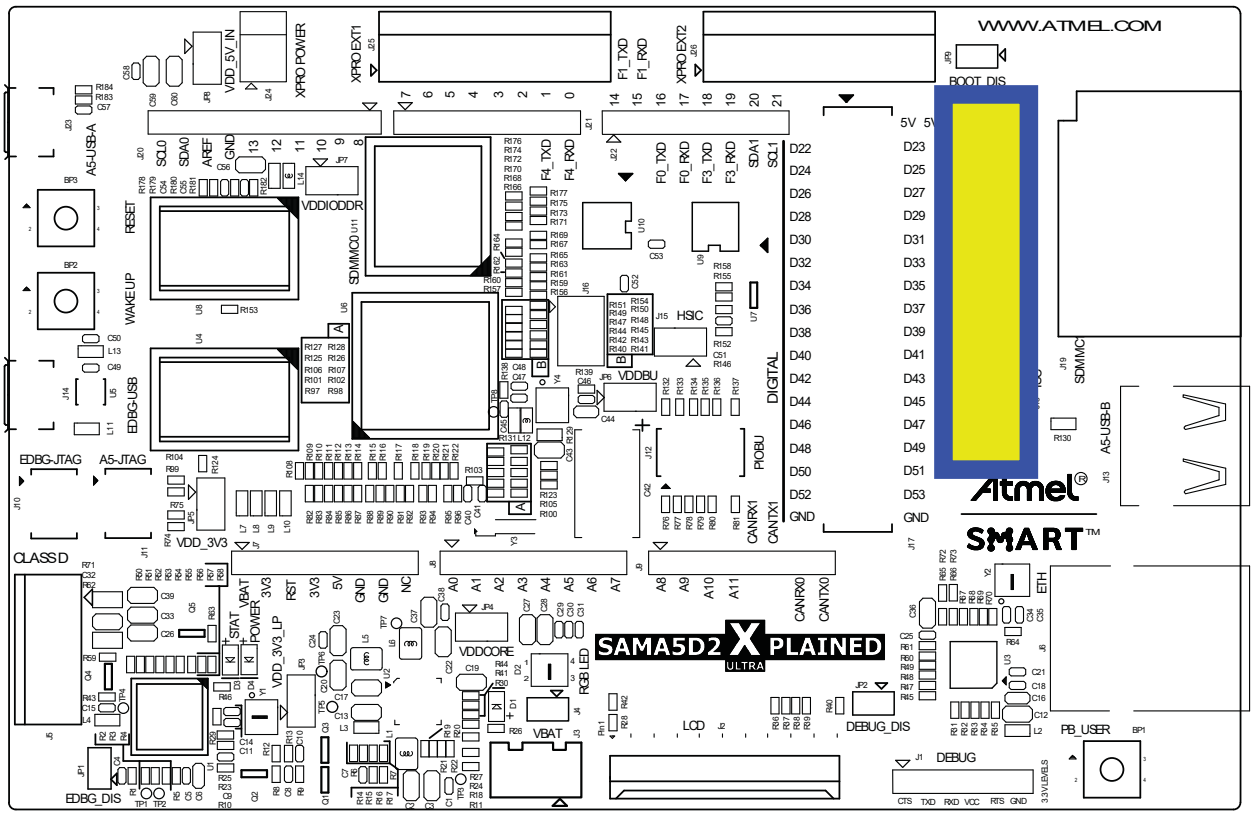


Table 6-10. ISC J18 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	3V3	–	ISC Power Supply
2	GND	–	Ground
3	3V3	–	ISC Power Supply
4	GND	–	Ground
5	ISC_RST	PB11	Reset ISC module
6	ISC_PWD	PB12	Power Down module
7	TWCK1	PD5	TWI Clock
8	TWD1	PD4	TWI Data
9	GND	–	Ground
10	ISC_MCK	PC7	ISC Master Clock
11	GND	–	Ground
12	ISC_VSYNC	PC5	ISC Vertical Synchronization

.....continued			
Pin	**Mnemonic**	**PIO**	**Signal Description**
13	GND	–	Ground
14	ISC_HSYNC	PC6	ISC Horizontal Synchronization
15	GND	–	Ground
16	ISC_PCK	PC4	Clock
17	GND	–	Ground
18	ISC_D4	PB30	Image data D0
19	ISC_D5	PB31	Data D1
20	ISC_D6	PC0	Data D2
21	ISC_D7	PC1	Data D3
22	ISC_D8	PC2	Data D4
23	ISC_D9	PC3	Data D5
24	ISC_D10	PB24	Data D6
25	ISC_D11	PB25	Data D7
26	ISC_D0	PB26	RFU
27	ISC_D1	PB27	RFU
28	ISC_D2	PB28	RFU
29	ISC_D3	PB29	RFU
30	GND	–	Ground

⚠WARNING The connector ISC J18 has been laid out to be compatible with previous evaluation kits and existing extensions in 8-bit modes. Hence, the 8-bit image data [7:0] are aligned with ISC_D[11:4] in the table above. Refer to the SAMA5D2 Series data sheet for an in-depth description of the ISC bussing scheme. A summary is also provided below.

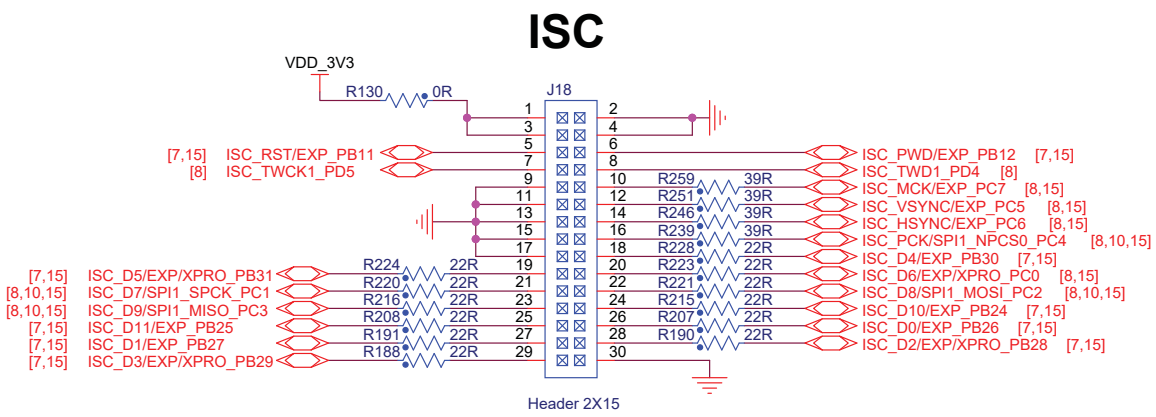
The table below shows how ISC_DATA[11:0] is routed to image data D[11:0] in relation to the bit mode.

Table 6-11. ISC Interface - ISC_DATA to Image Data

Interface	12-bit	11-bit	10-bit	9-bit	8-bit
isc_data[11](MSB)	D[11]	D[10]	D[9]	D[8]	D[7]
isc_data[10]	D[10]	D[9]	D[8]	D[7]	D[6]
isc_data[9]	D[9]	D[8]	D[7]	D[6]	D[5]
isc_data[8]	D[8]	D[7]	D[6]	D[5]	D[4]
isc_data[7]	D[7]	D[6]	D[5]	D[4]	D[3]
isc_data[6]	D[6]	D[5]	D[4]	D[3]	D[2]
isc_data[5]	D[5]	D[4]	D[3]	D[2]	D[1]
isc_data[4]	D[4]	D[3]	D[2]	D[1]	D[0]
isc_data[3]	D[3]	D[2]	D[1]	D[0]	Not Used

.....continued					
Interface	**12-bit**	**11-bit**	**10-bit**	**9-bit**	**8-bit**
isc_data[2]	D[2]	D[1]	D[0]	Not Used	Not Used
isc_data[1]	D[1]	D[0]	Not Used	Not Used	Not Used
isc_data[0]	D[0]	Not Used	Not Used	Not Used	Not Used

Figure 6-29. ISC J18 Header



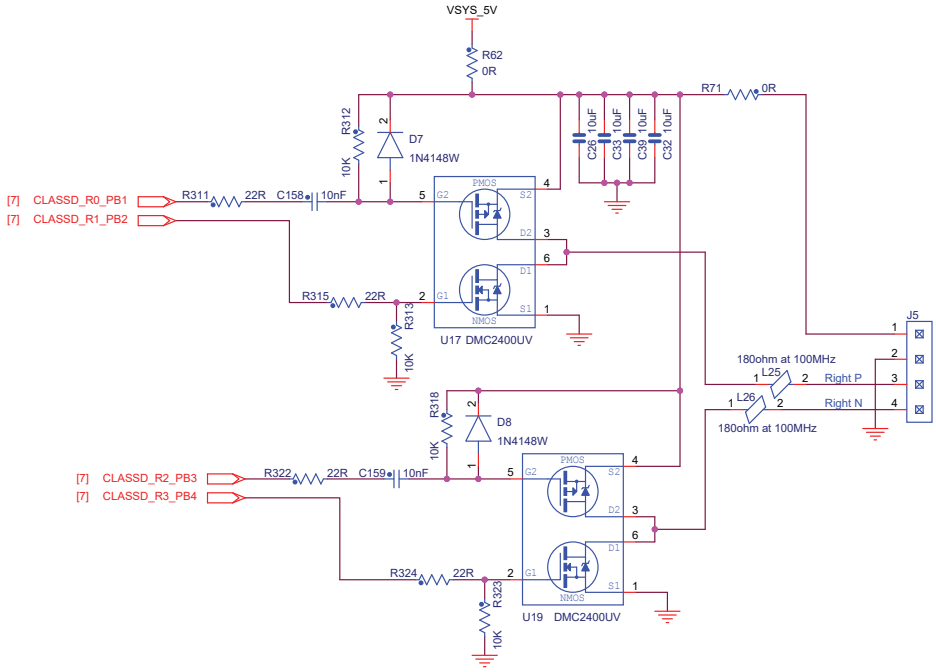
6.4.7 Audio Class D Amplifier

The Audio Class D Amplifier (CLASSD) is a digital input, Pulse Width Modulated (PWM) output stereo Class D amplifier. It features a high-quality interpolation filter embedding a digitally controlled gain, an equalizer and a de-emphasis filter.

On its input side, the CLASSD is compatible with most common audio data rates. On the output side, its PWM output can drive either:

- high-impedance single-ended or differential output loads (Audio DAC application) or,
- external MOSFETs through an integrated non-overlapping circuit (Class D power amplifier application).

Figure 6-30. Audio PWM Class D MOSFET Mono Amplifier



CLASSD Output Connector J5

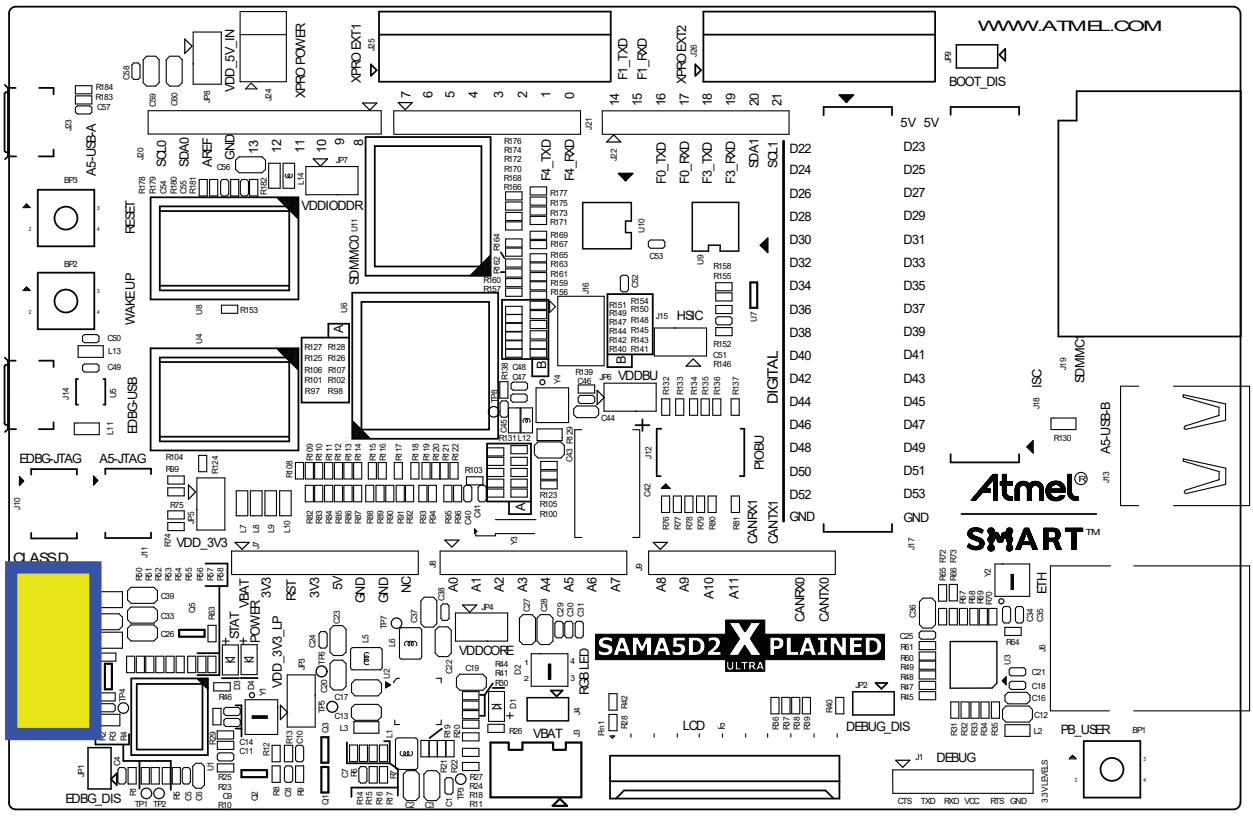


Table 6-12. CLASSD Output Connector J5 Signal Descriptions

Pin	Mnemonic	Signal Description
1	VSYS_5V	Power
2	GND	GND
3	OUTPUT RIGHT P	Positive Level
4	OUTPUT RIGHT N	Negative Level

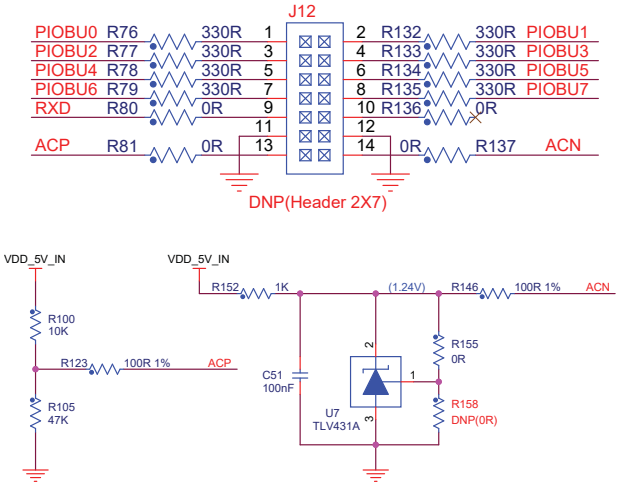
6.4.8 Tamper Interface

The SAMA5D2C-XULT board features eight tamper pins for static or dynamic intrusion detections, UART reception, and two analog pins for comparison.

For information on intrusion detection for SAMA5D23 and SAMA5D28, refer to the document “SAMA5D2 Security Module”, document no. 44036. This document is available under Non-Disclosure Agreement (NDA).

Contact a Microchip sales representative for further details.

Figure 6-31. Tamper Pin Connector J12



6.4.9 Tamper Connector

Figure 6-32. Tamper Connector J12

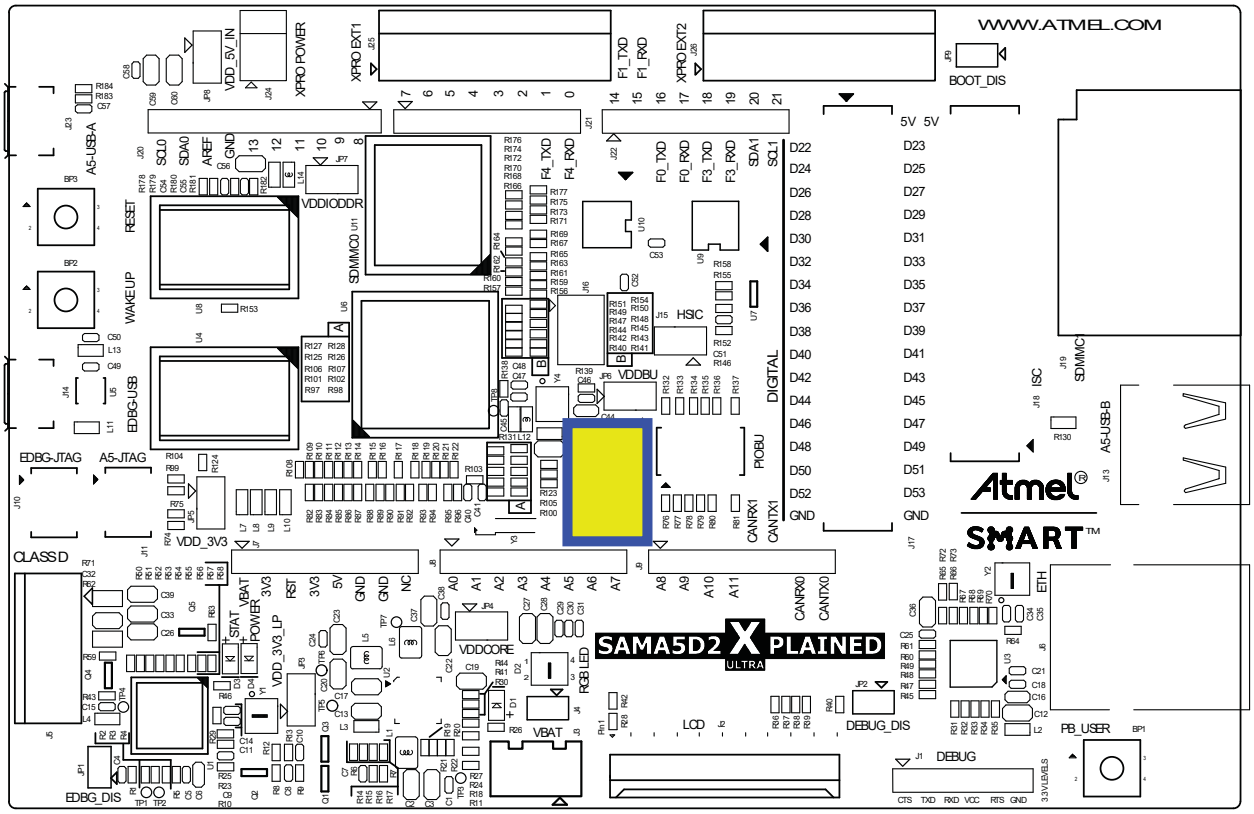


Table 6-13. Tamper Connector J12 Signal Descriptions

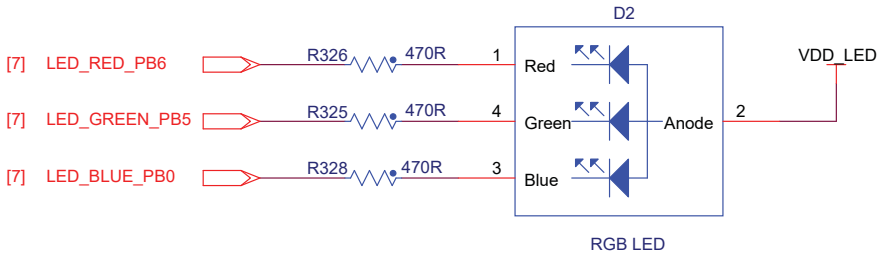
Signal	Pin No.		Signal
PIOBU0	1	2	PIOBU1
PIOBU2	3	4	PIOBU3
PIOBU4	5	6	PIOBU5

.....continued			
Signal	**Pin No.**		**Signal**
PIOBU6	7	8	PIOBU7
RXD	9	10	NC
GND	11	12	GND
ACP	13	14	ACN

6.4.10 RGB LED

There is one RGB LED on the SAMA5D2C-XULT board; it can be controlled by the user. The three LED cathodes are controlled via GPIO PWM pins.

Figure 6-33. RGB LED Indicators

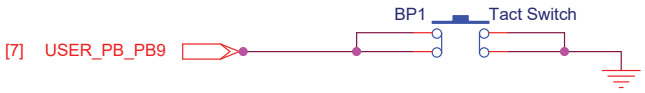


6.4.11 Push Button Switches

The SAMA5D2C-XULT board features three push buttons:

- One board Reset button (BP3) connected to the PMIC ACT8945A. When pressed and released, it causes a Power-on Reset of the board.
- One wake-up push button connected to the PMIC ACT8945A, used to exit the processor from Low-power mode (BP2).
- One User momentary push button (BP1).

Figure 6-34. User Push Buttons (BP1)



6.4.12 Debug Interfaces

The SAMA5D2C-XULT board includes a JTAG, a Debug serial COM port and an EDBG interface port, to provide debug level access to the SAMA5D2.

6.4.12.1 Debug JTAG

A 10-pin JTAG header is provided on the SAMA5D2C-XULT board to facilitate the software development and debugging by using various JTAG emulators. The interface signals have a voltage level of 3.3V.

Figure 6-35. JTAG Interface

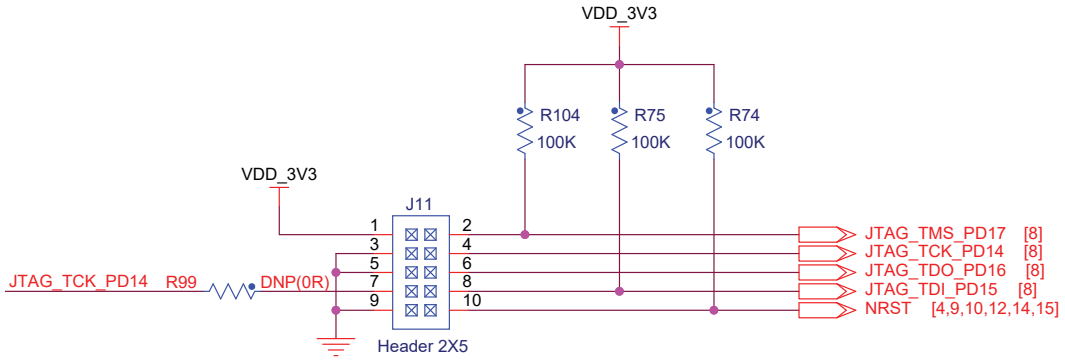


Figure 6-36. JTAG J11

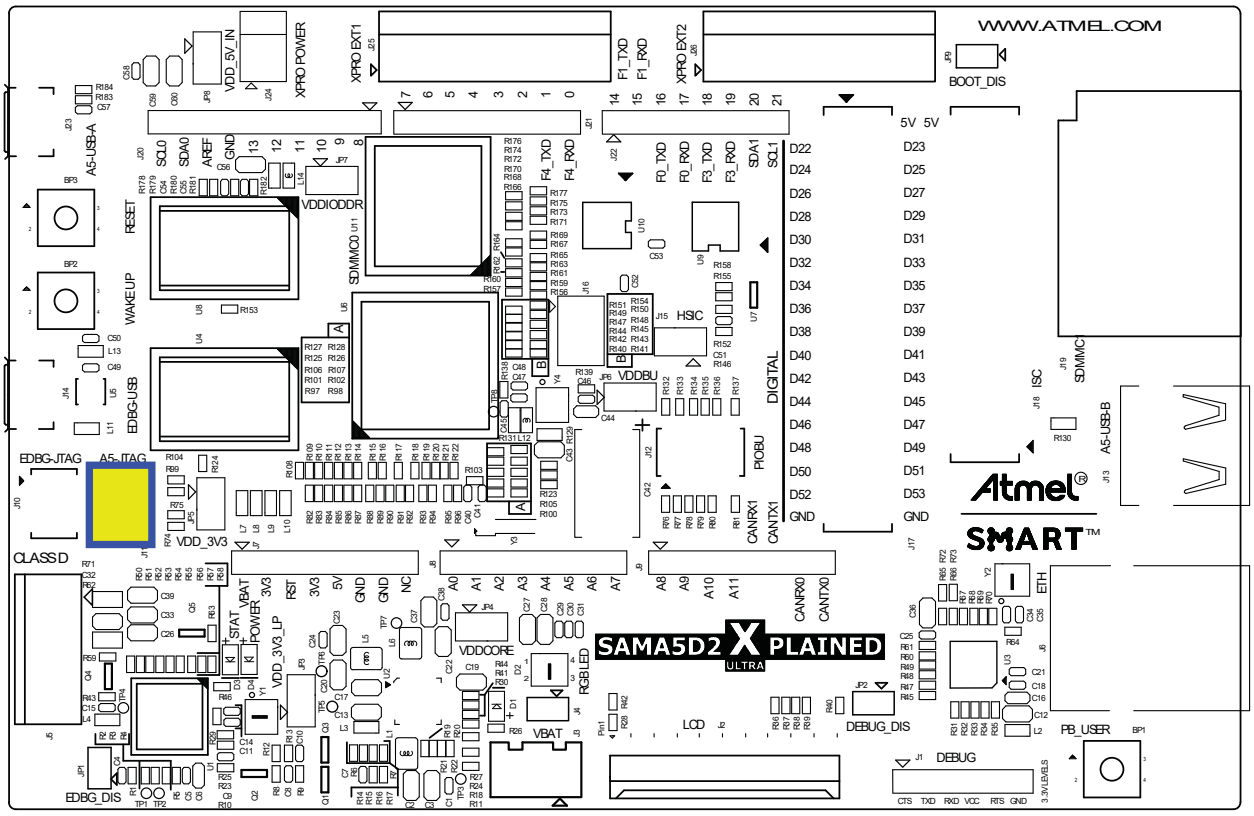


Table 6-14. JTAG/ICE Connector J11 Signal Descriptions

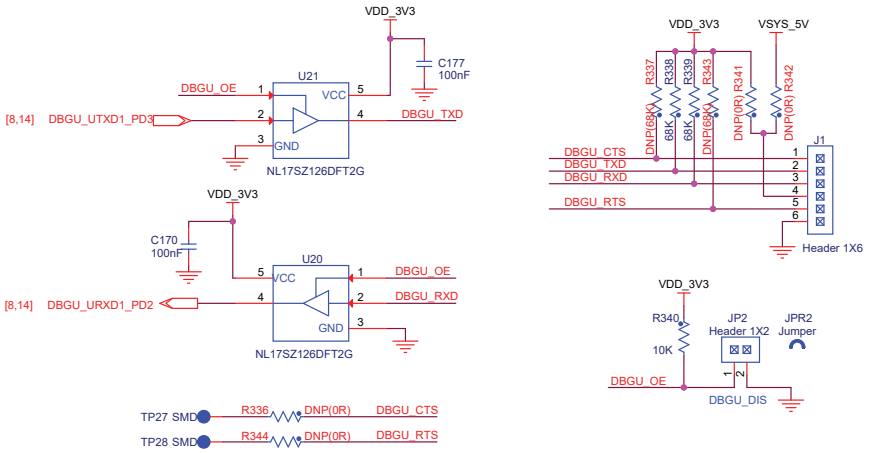
Pin	Mnemonic	Signal Description
1	VTref. 3.3V power	This is the target reference voltage (main 3.3V).
2	TMS TEST MODE SELECT	JTAG mode set input into target CPU
3	GND	Common ground
4	TCK TEST CLOCK – Output timing signal, for synchronizing test logic and control register access	JTAG clock signal into target CPU
5	GND	Common ground
6	TDO JTAG TEST DATA OUTPUT – Serial data input from the target	JTAG data output from target CPU

.....continued		
Pin	**Mnemonic**	**Signal Description**
7	RTCK – Input Return test clock signal from the target	Some targets having too slow of a system clock must synchronize the JTAG inputs to internal clocks. In present case such synchronization is unneeded and TCK merely looped back into RTCK.
8	TDI TEST DATA INPUT – Serial data output line, sampled on the rising edge of the TCK signal	JTAG data input into target CPU
9	GND	Common ground
10	nSRST RESET	Active-low reset signal. Target CPU reset signal.

6.4.12.2 Serial Console Port

The SAMA5D2C-XULT board has a dedicated serial port for debugging, which is accessible through the 6-pin male header J1. Various interfaces can be used as USB/Serial DBGU port bridge, such as FTDI TTL-232R USB to TTL serial cable or basic breakout board for the RS232/USB converter.

Figure 6-37. Debug Com Port for Console



A jumper (JP2) is available to disable the Debug communication interface.

R341 and R342 are optional (not implemented) resistors that can be used for power selection. Power can be delivered either by the SAMA5D2C-XULT board or by the debug interface tool. To avoid malfunction between the debug interface (e.g., FTDI) and the on-board power system, ensure that the selected voltage level corresponds to application requirements. The console baud rate is set to 115200 by default.

Figure 6-38. DEBUG Connector J1

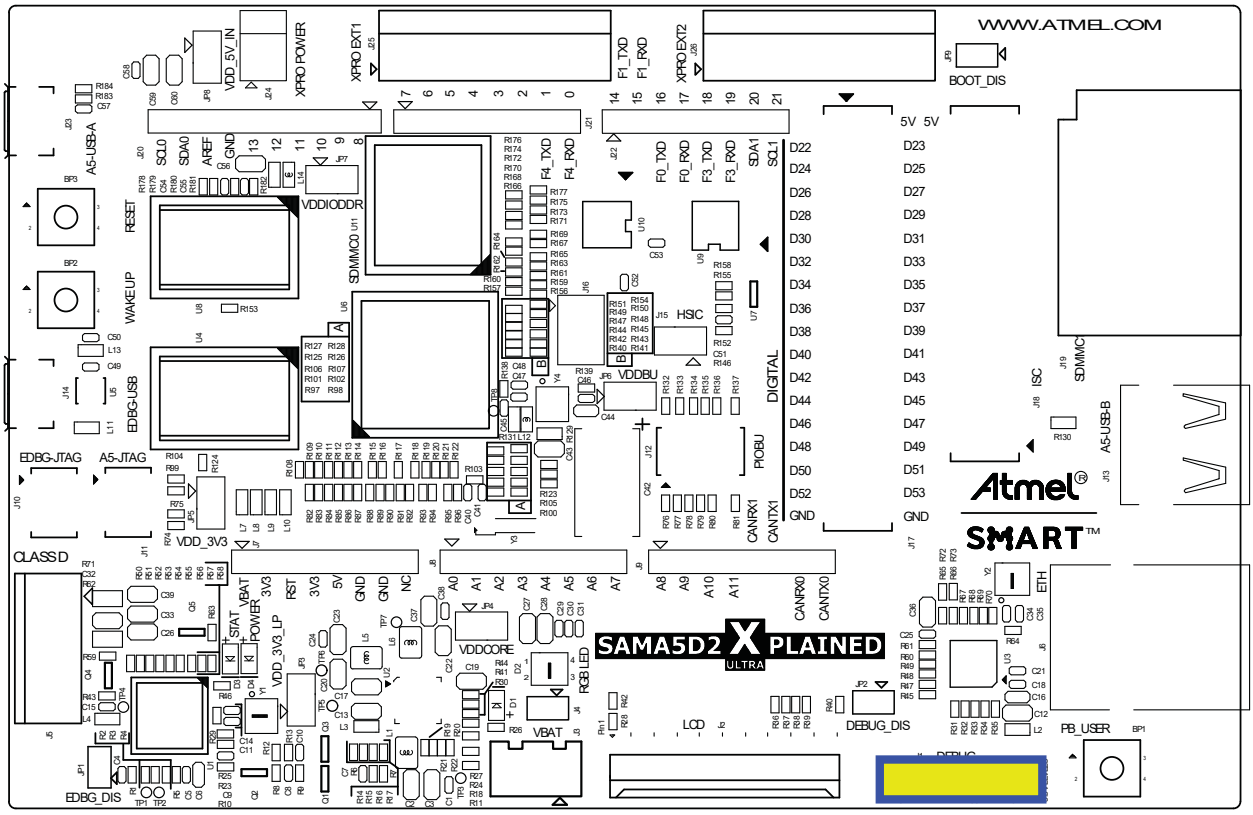


Table 6-15. DEBUG Connector J1 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	CTS	RFU	Handshake input
2	TXD1 (Transmitted Data)	PD3	RS232 serial data output signal
3	RXD1 (Received Data)	PD2	RS232 serial data input signal
4	Power	–	5V/3.3V (selected by resistors)
5	RTS	RFU	Handshake output
6	GND	–	Common ground

⚠WARNING When using a console connected to the DEBUG interface J1, the jumper JP2 DEBUG_DIS should be OFF.

6.4.13 Embedded Debugger (EDBG) Interface

The Embedded Debugger (EDBG)[1] is an intuitive plug-and-play solution which adds full programming and debugging support to embedded hardware kits containing Microchip microcontrollers and microprocessors. It enables seamless integration between the target hardware and the Atmel Studio front end.

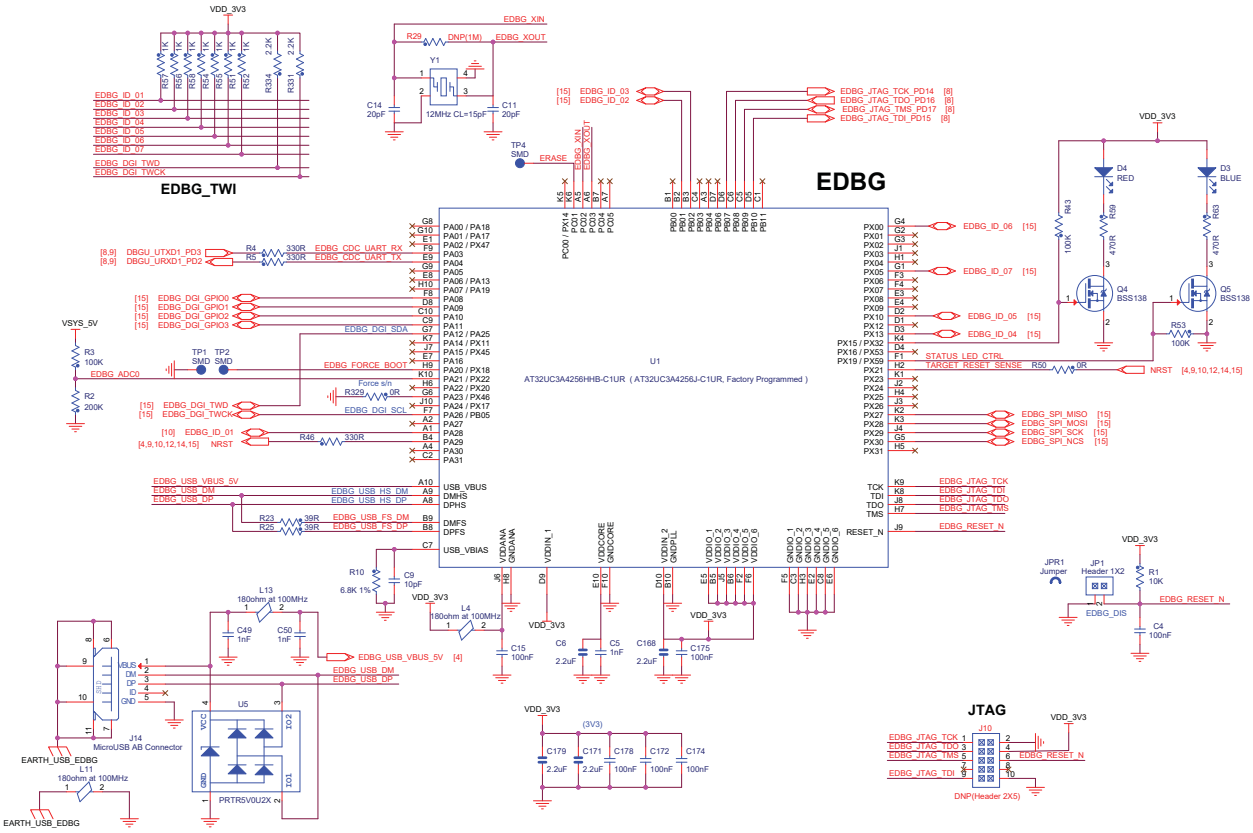
1 Device and Ordering Information—The EDBG is a factory-programmed AT32UC3A4256J-C1UR standard microcontroller with ordering code AT32UC3A4256HHB-C1UR. For more information, contact your local Microchip sales representative.

In addition to the Virtual COM port which provides a UART bridge to the target device, the EDBG provides a Data Gateway Interface, through which the target device and host PC can communicate, facilitating high-level application debugging, monitoring, graphing and logging of system information in real-time.

The EDBG is based on the AT32UC3A4256J high-performance low-power 32-bit AVR microcontroller running at up to 60 MHz. The device includes an on-chip USB 2.0 high-speed hardware module with dedicated DMA channels, making it ideal for data communications.

By default, the EDBG is in Reset state and not usable. To use the EDBG interface, remove the jumper JP1. To avoid any conflicts with the debug signals, do not use the JTAG and EDBG at the same time.

Figure 6-39. EDBG Interface



6.4.14 CDC Debug Interface

This feature is enabled only if pin J9 (RESET_N) of the microcontroller is not tied to ground. The pin is normally pulled high and controlled by jumper JP1.

- Jumper JP1 not installed: The CDC device is enabled.
- Jumper JP1 installed: The CDC device is disabled.

WARNING The default baud rate CDC is 57600 (57600/N/8/1).

WARNING When using a console with the EDBG-CDC, the jumper JP2 DEBUG_DIS should be ON.

6.4.15 EDBG USB Type Micro-AB

Figure 6-40. EDBG USB Type Micro-AB Connector J14

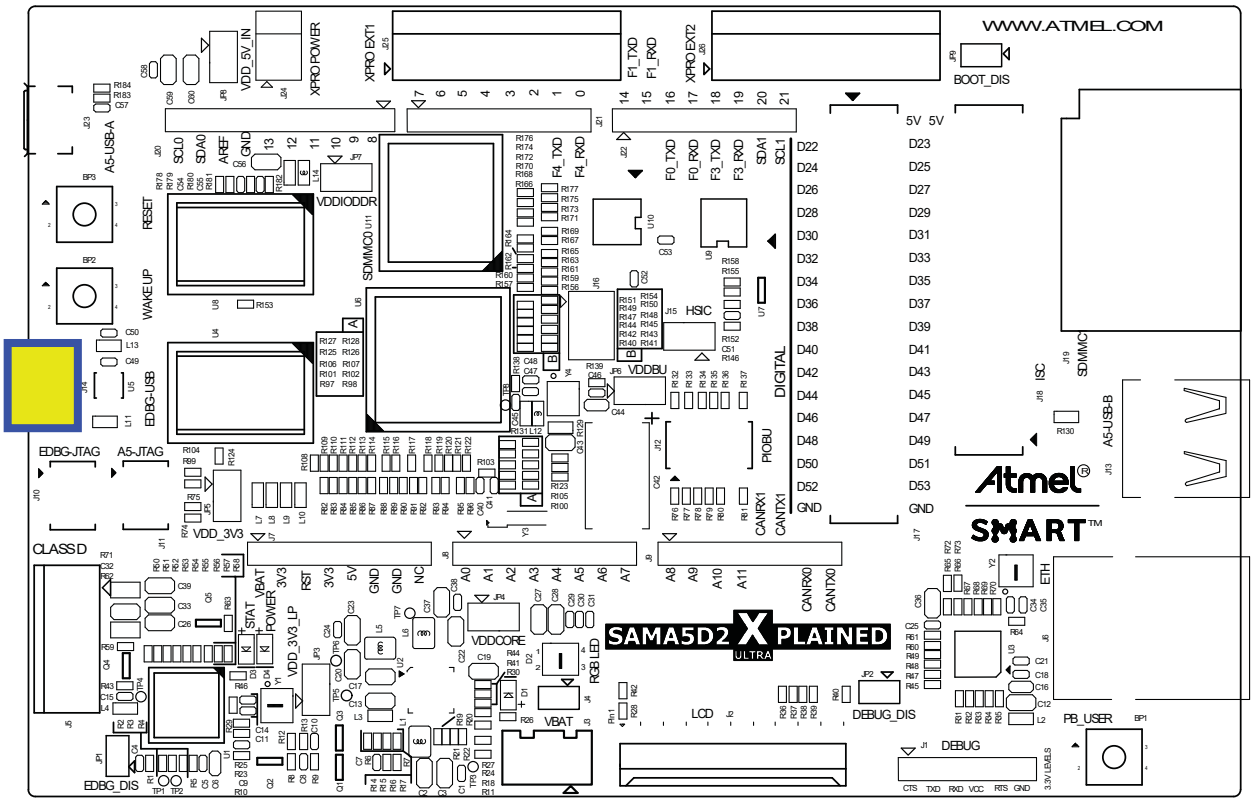


Table 6-16. USB Connector J14 Signal Descriptions

Pin	Mnemonic	Signal Description
1	VBUS	5V power
2	DM	Data minus
3	DP	Data plus
4	ID	On-the-go identification (not connected)
5	GND	Common ground

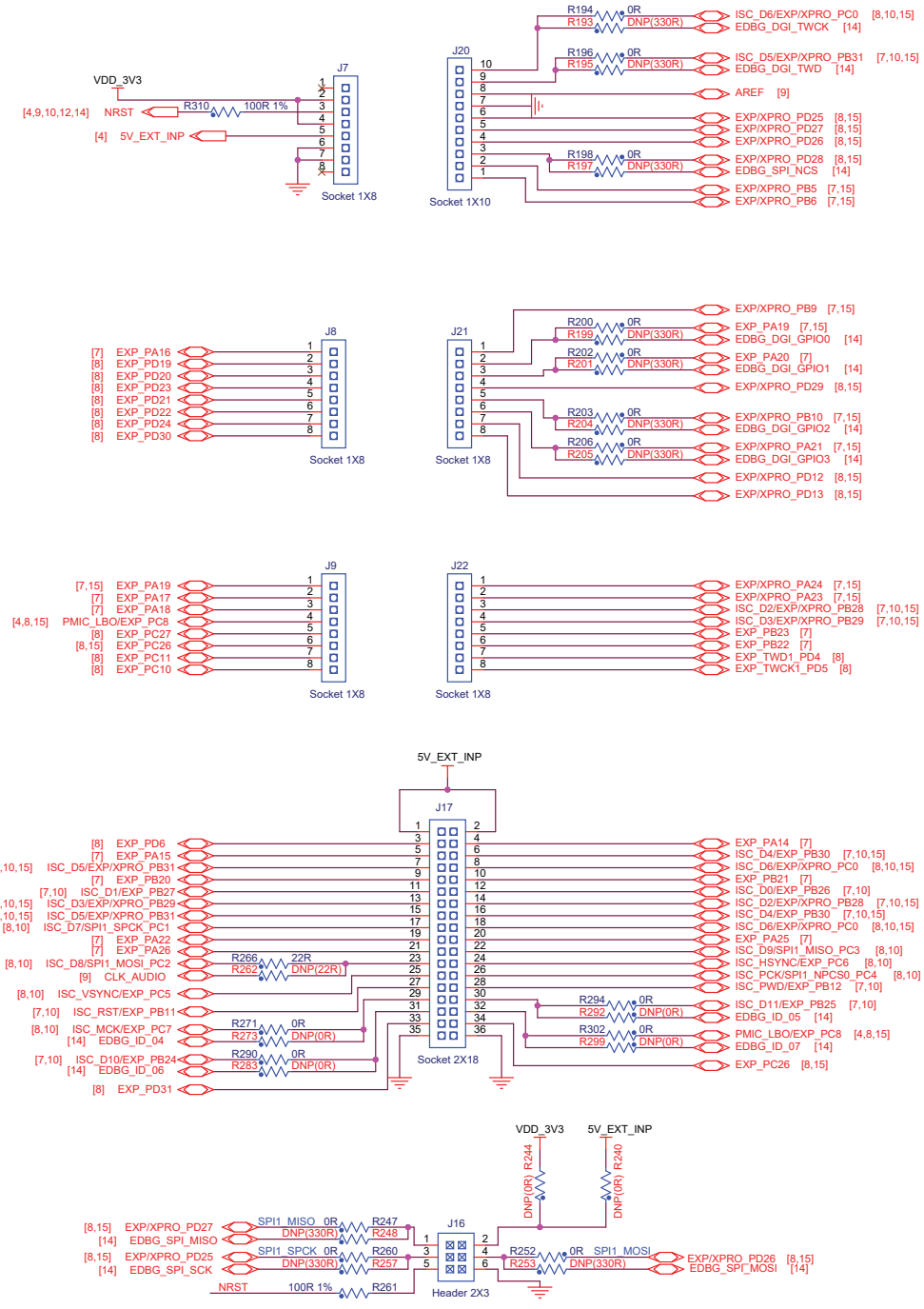
6.5 PIO Usage on Expansion Connectors

6.5.1 Arduino Connectors

Five 8-pin, one 6-pin, one 10-pin and one 36-pin headers (J7, J8, J9, J16, J17, J20, J21, J22) are provided on the SAMA5D2C-XULT board to enable the PIO connection of various expansion cards. These headers' physical and electrical implementation match the Arduino R3 extension ("shields") system.

Due to I/O multiplexing, different signals can be provided on each pin.

Figure 6-41. Expansion Boards Connectors



6.5.1.1 Functions Available Through the Arduino Headers

The multiplexing of the SAMA5D27 I/Os (standard parallel I/O and up to three peripheral functions per pin) makes it possible to route alternate signals via Arduino extension headers. To enable these signals, SAMA5D27 PIO multiplexing must be properly configured. For more details, refer to Board Schematics and the section PIO Controller (PIO) in the SAMA5D2 Series data sheet.

The tables below, together with the connector schematics, provide the alternate signals available for use with Arduino connectors.

Figure 6-42. J7 Connector

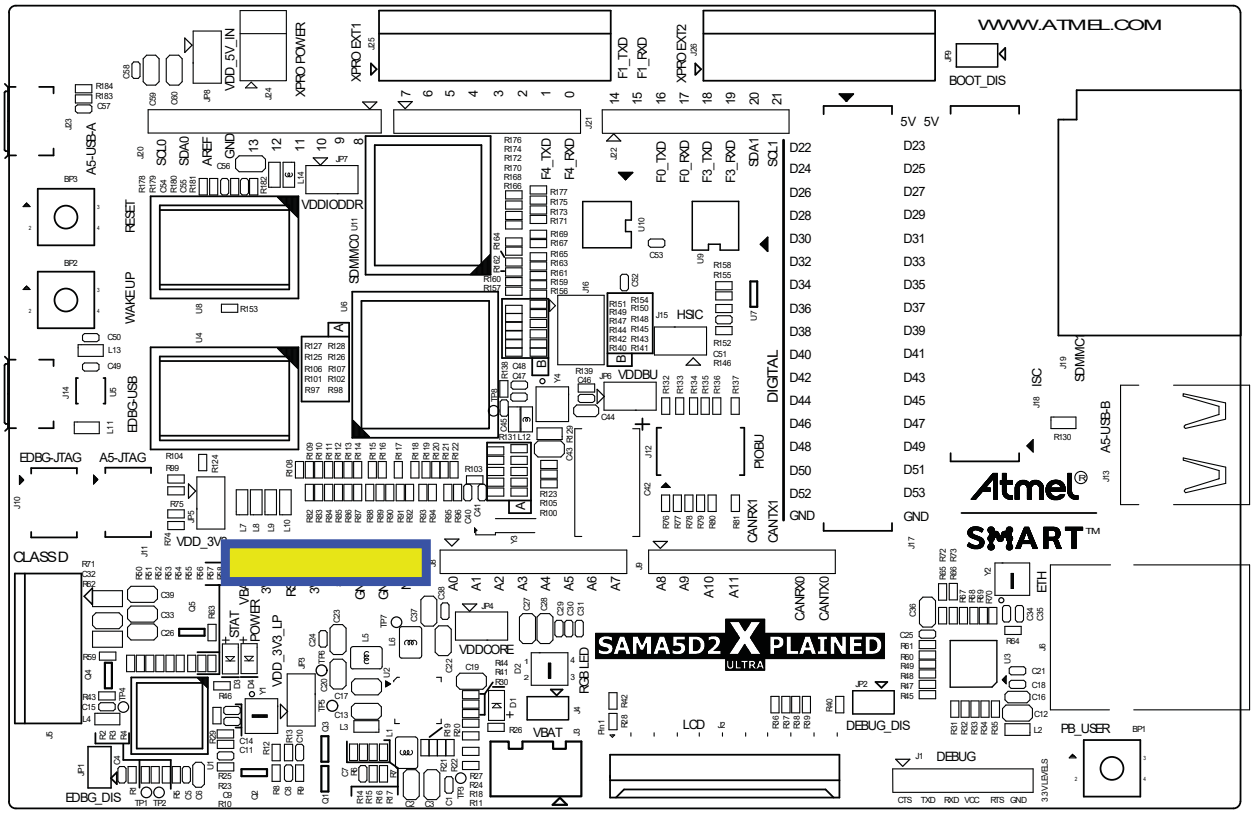


Table 6-17. J7 Connector Signals

Pin No.	Signal	Function
1	VBAT	NC
2	3V3	(IOREF)
3	RST	–
4	3V3	–
5	5V	–
6	GND	–
7	GND	–
8	VIN	NC

Figure 6-43. J8 Connector

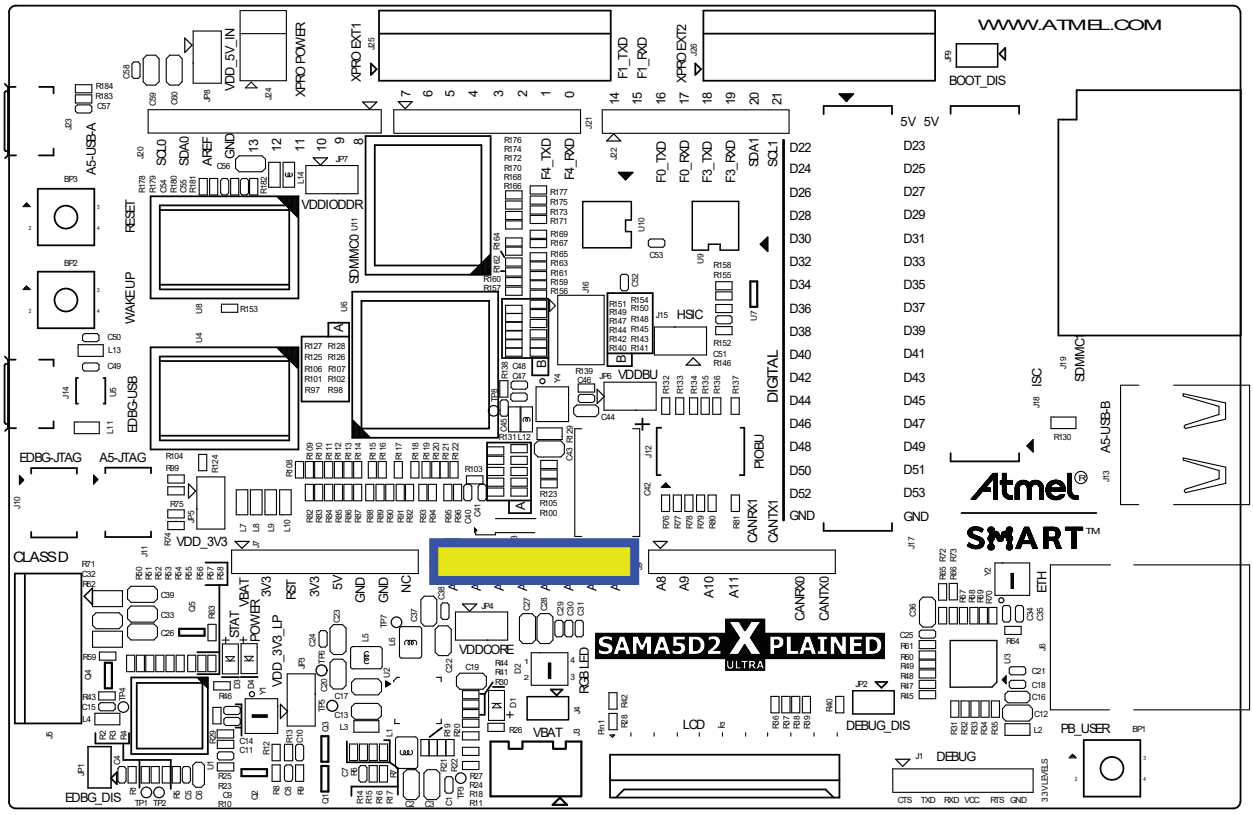


Table 6-18. J8 Connector Signals

Pin		SAMA5D27 PIO Muxing Alternates						
No.	Type							
1	PA16	SPI0_MISO	TD1	QSPI0_IO0	I2SWS1	FLEXCOM3_IO4	D11	–
2	PD19	PCK0	TWD1	URXD2	–	I2SCK0	ISC_D11	AD0
3	PD20	TIOA2	TWCK1	UTXD2	–	I2SMCK0	ISC_PCK	AD1
4	PD23	URXD2	–	FLEXCOM4_IO3	–	I2SDO0	ISC_FIELD	AD4
5	PD21	TIOB2	TWD0	FLEXCOM4_IO1	–	I2SWS0	ISC_VSYNC	AD2
6	PD22	TCLK2	TWCK0	FLEXCOM4_IO2	–	I2SDI0	ISC_HSYNC	AD3
7	PD24	UTXD2	–	FLEXCOM4_IO4	–	–	–	AD5
8	PD30	SPI1_NPCS2	TMS	FLEXCOM2_O1	TIOB3	TWCK0	–	AD11

Figure 6-44. J9 Connector

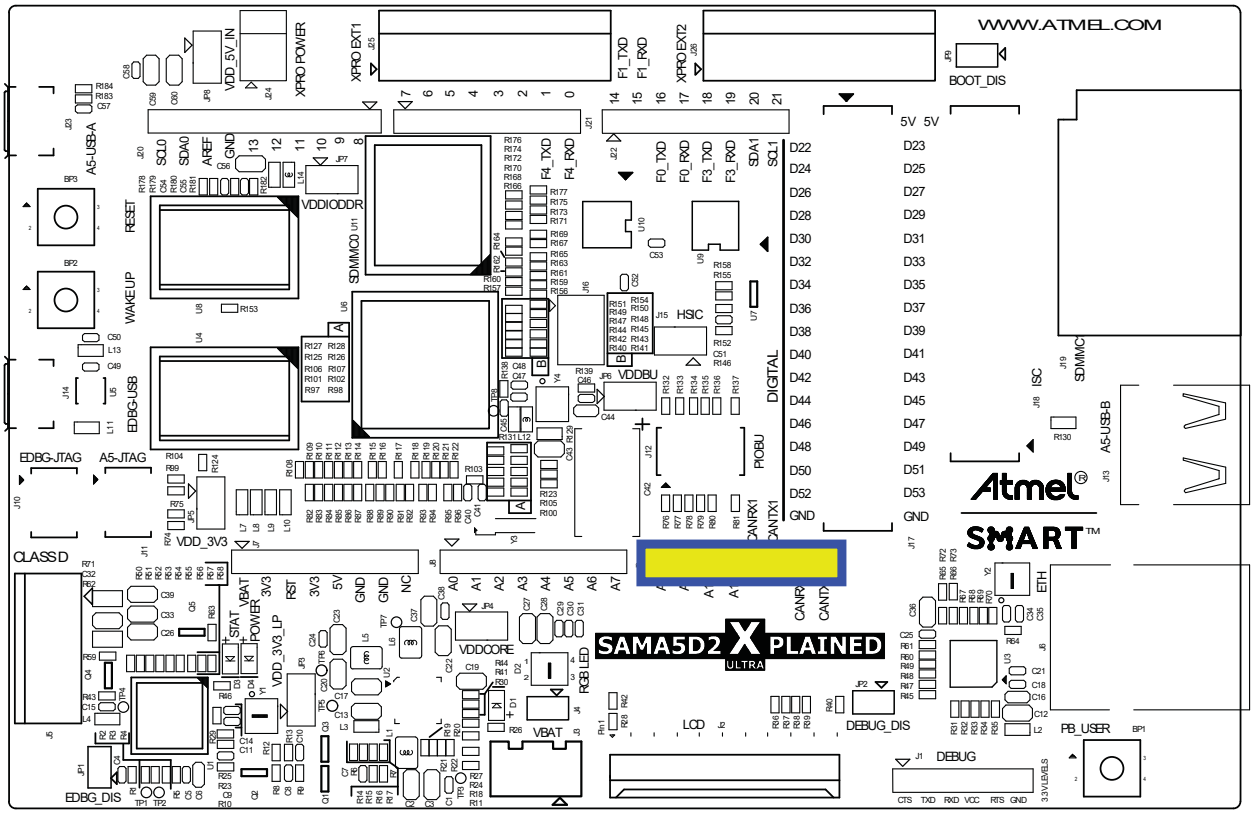


Table 6-19. J9 Connector Signals

Pin		SAMA5D27 PIO Muxing Alternates					
No.	Type						
1	PA19	SPI0_NPCS2	RF1	QSPI0_IO3	TIOA0	SDHC1_DAT1	D14
2	PA17	SPI0_NPCS0	RD1	QSPI0_IO1	I2SDI1	FLEXCOM3_O1	D12
3	PA18	SPI0_NPCS1	RK1	QSPI0_IO2	I2SDO1	SDHC1_DAT0	D13
4	PC8	LCDDEN	NANDRDY	FIQ	PCK0	UTXD1	ISC_FIELD
5	PC27	LCDDAT23	GTX3	PCK1	CANRX1	TWD0	A16
6	PC26	LCDDAT22	–	GTX2	CANTX1	–	A15
7	PC11	LCDDAT3	GTXEN	ISC_D2	TCLK4	CANRX0	A0/NBS0
8	PC10	LCDDAT2	GTXCK	ISC_D1	TIOB4	CANTX0	–

Figure 6-45. J20 Connector

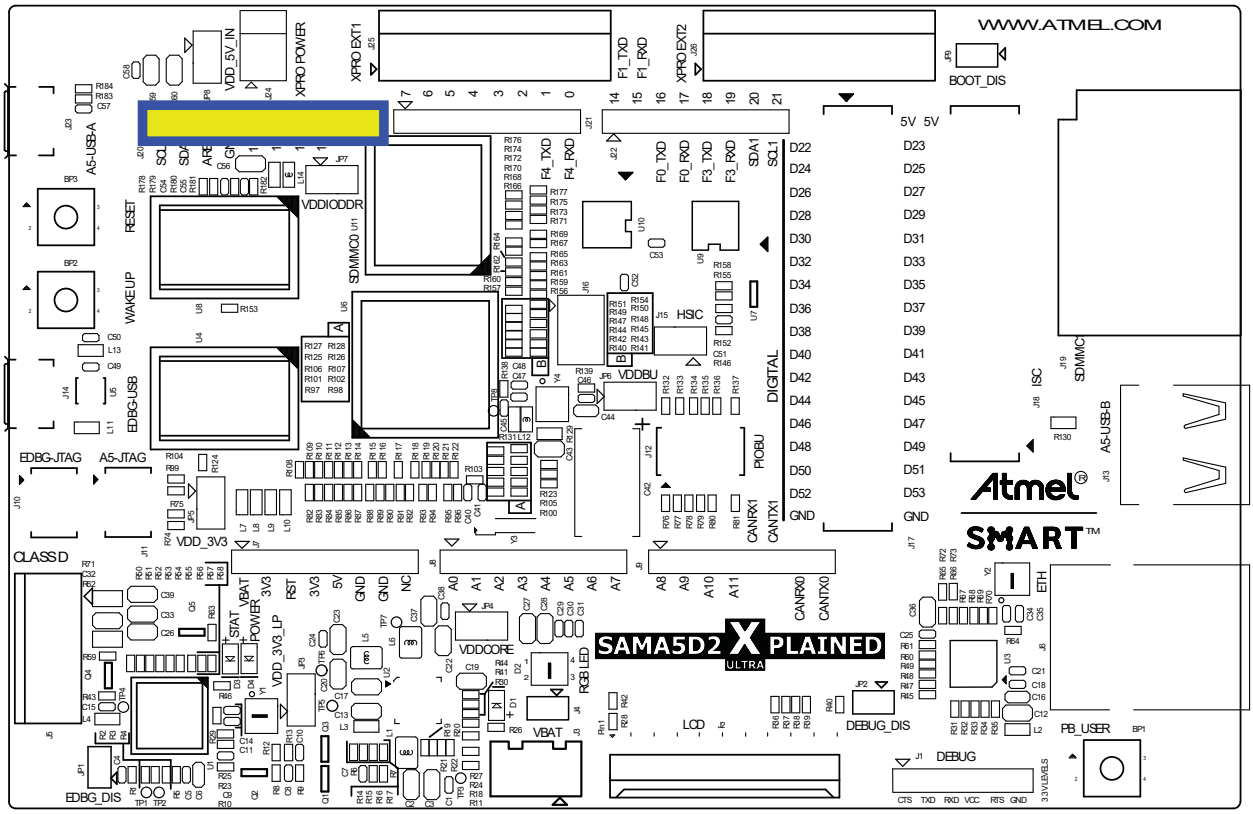


Table 6-20. J20 Connector Signals

Pin		SAMA5D27 PIO Muxing Alternates					
No.	Type						
10	PC0	LCDDAT21	A23	FLEXCOM0_O1	TWCK0	–	ISC_D6
9	PB31	LCDDAT20	A20	FLEXCOM0_IO4	TWD0	–	ISC_D5
8	AREF	–	–	–	–	–	–
7	GND	–	–	–	–	–	–
6	PD25	SPI1_SPCK		FLEXCOM4_O1	–	–	AD6
5	PD27	SPI1_MISO	TCK	FLEXCOM2_IO2	–	–	AD8
4	PD26	SPI1_MOSI	–	FLEXCOM2_IO1	–	–	AD7
3	PD28	SPI1_NPCS0	TDI	FLEXCOM2_IO3	–	–	AD9
2	PB5	TCLK2	D10	PWMH2	QSPI1_SCK	PTCPORT5	GTSUCOMP
1	PB6	TIOA2	D11	PWML2	QSPI1_CS	PTCPORT6	GTXER

Figure 6-46. J21 Connector

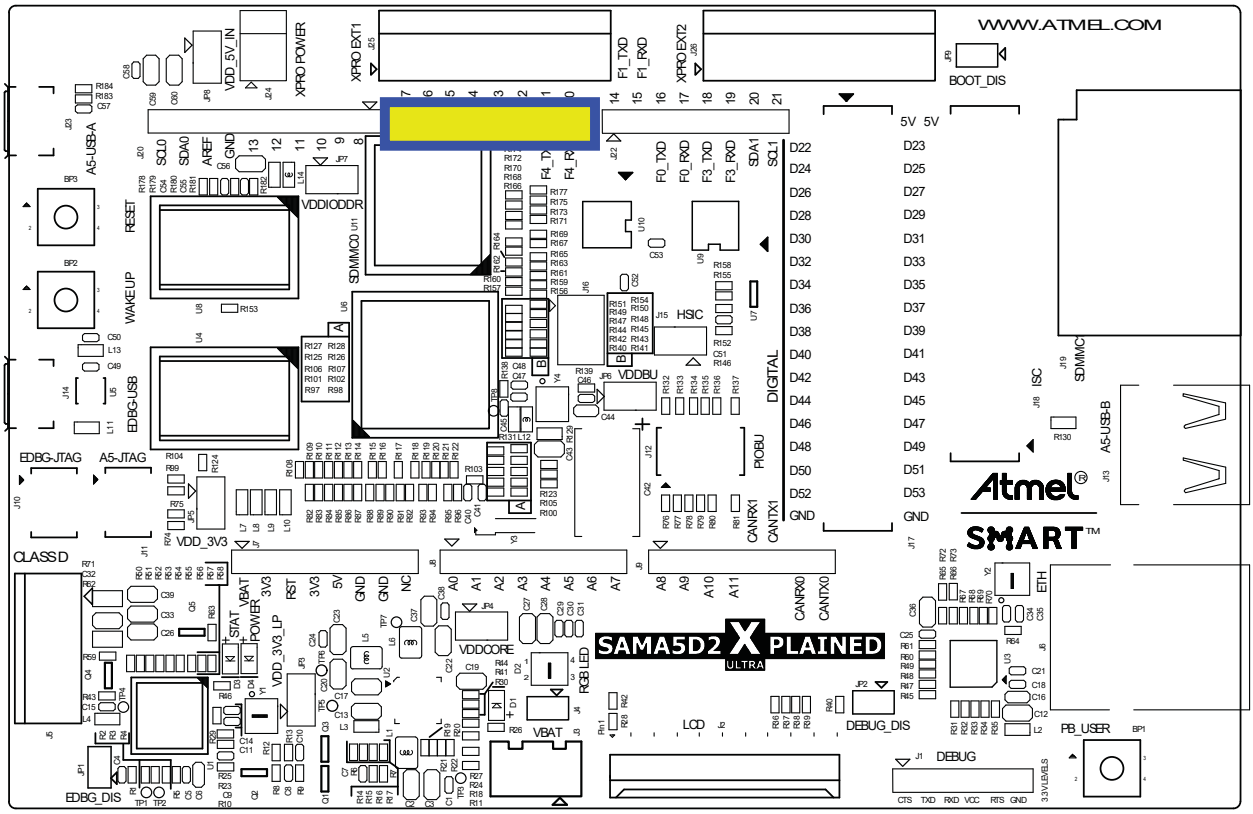


Table 6-21. J21 Connector Signals

Pin		SAMA5D27 PIO Muxing Alternates					
No.	Type						
1	PB9	TIOA3	D14	PWMFI1	QSPI1_IO2	–	GCOL
2	PA19	SPI0_NPCS2	RF1	QSPI0_IO3	TIOA0	SDHC1_DAT1	D14
3	PA20	SPI0_NPCS3	–	–	TIOB0	SDHC1_DAT2	D15
4	PD29	SPI1_NPCS1	TDO	FLEXCOM2_IO4	TIOA3	TWD0	AD10
5	PB10	TIOB3	D15	PWMEXTRG1	QSPI1_IO3	–	GRX2
6	PA21	IRQ	PCK2		TCLK0	SDHC1_DAT3	NANDRDY
7	PD12	TIOB1	FLEXCOM4_IO0	UTMI_LS1	GRXER	ISC_D5	ISC_D0
8	PD13	TCLK1	FLEXCOM4_IO1	UTMI_CRDCPSEL0	GRX0	ISC_D6	ISC_D1

Figure 6-47. J22 Connector

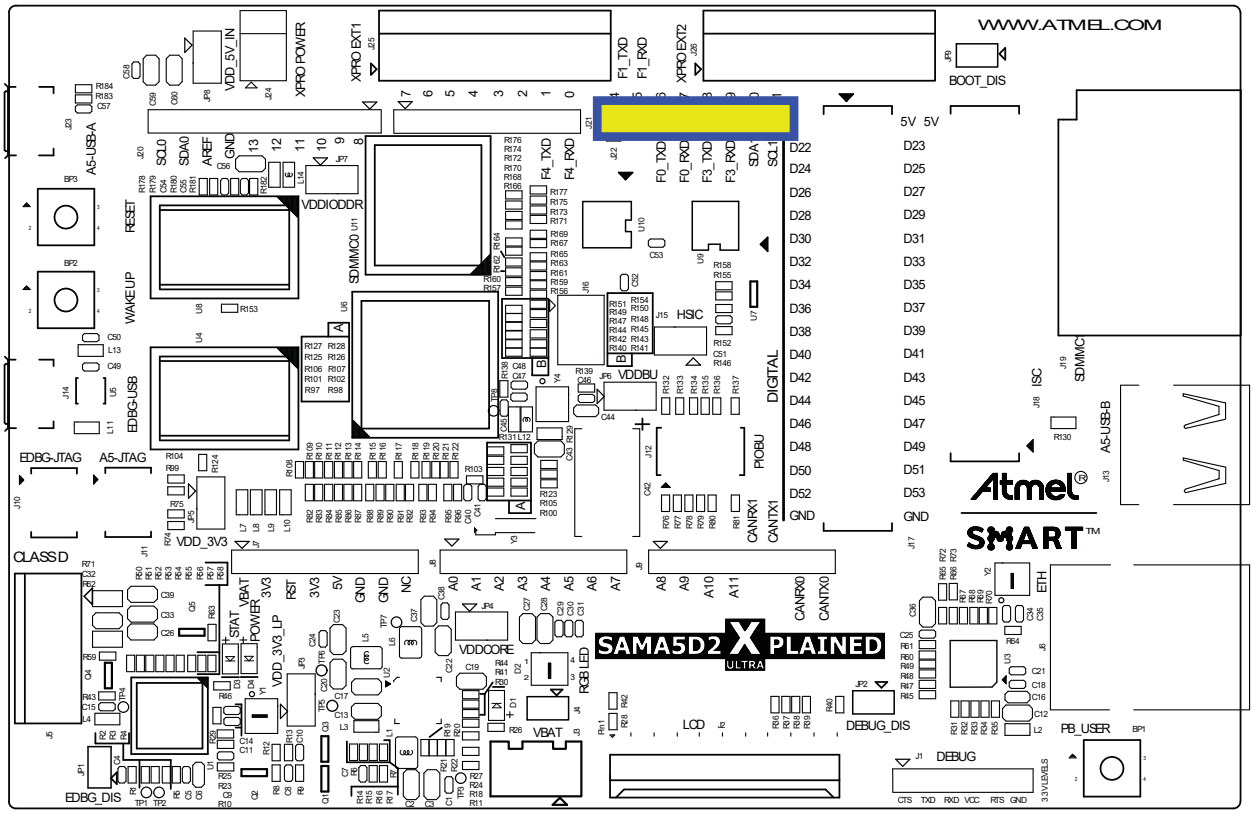


Table 6-22. J22 Connector Signals

Pin		SAMA5D27 PIO Muxing Alternates					
No.	Type						
1	PA24	FLEXCOM1_IO0	D2	TDO	SPI1_MISO	–	QSPI0_IO0
2	PA23	FLEXCOM1_IO1	D1	TDI	SPI1_MOSI	–	QSPI0_CS
3	PB28	LCDDAT17	A17	FLEXCOM0_IO0	TIOA5	–	ISC_D2
4	PB29	LCDDAT18	A18	FLEXCOM0_IO1	TIOB5	–	ISC_D3
5	PB23	LCDDAT12	A12	RD0	TIOB2	FLEXCOM3_IO1	GMDIO
6	PB22	LCDDAT11	A11	TD0	TIOA2	FLEXCOM3_IO2	GMDC
7	PD4	TWD1	URXD2	–	GCOL	ISC_D10	NCS0
8	PD5	TWCK1	UTXD2	–	GRX2	ISC_D9	NCS1

Figure 6-48. J17 Connector

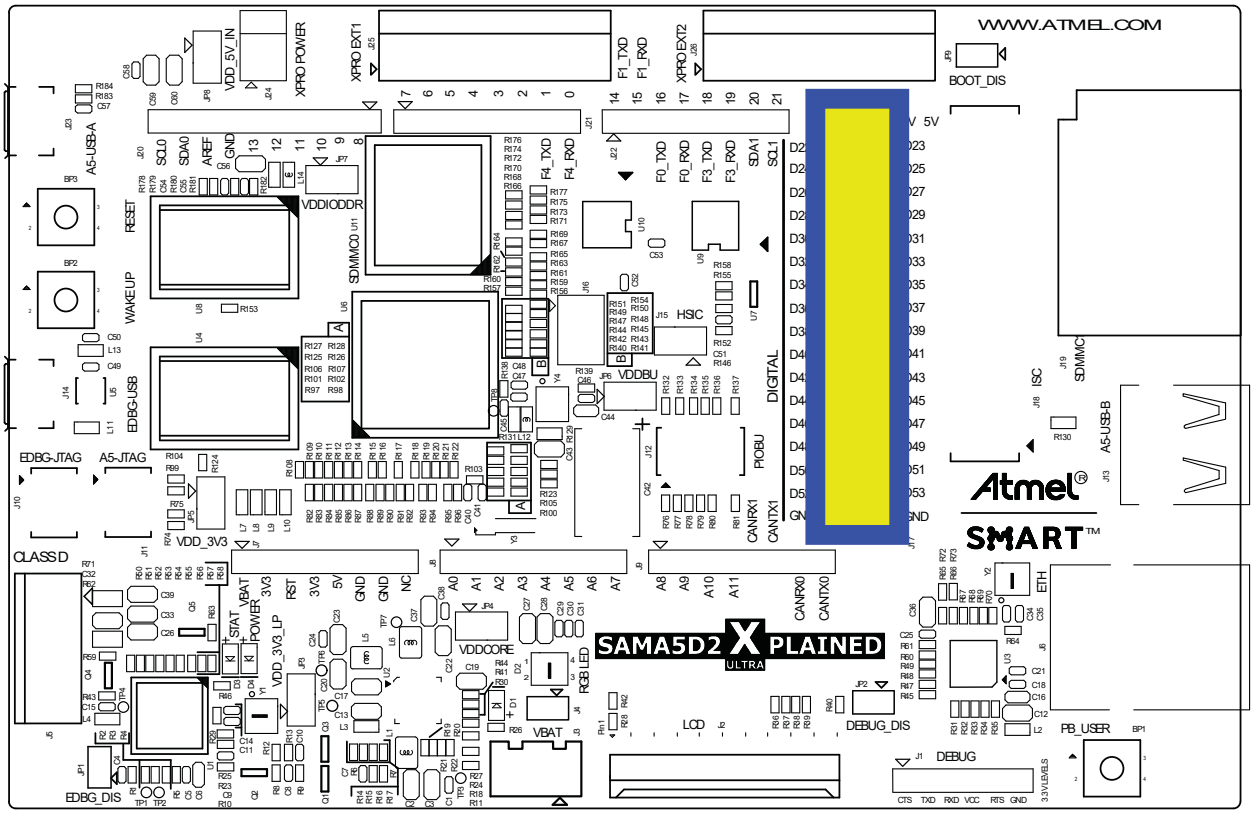


Table 6-23. J17 Connector Signals

Pin		SAMA5D27 PIO Muxing Alternates					
No.	Type						
1	5V	–	–	–	–	–	–
2	5V	–	–	–	–	–	–
3	PD6	TCK	PCK1	–	GRX3	ISC_D8	NCS2
4	PA14	SPI0_SPCK	TK1	QSPI0_SCK	I2SMCK1	FLEXCOM3_IO3	D9
5	PA15	SPI0_MOSI	TF1	QSPI0_CS	I2SCK1	FLEXCOM3_IO1	D10
6	PB30	LCDDAT19	A19	FLEXCOM0_IO3	TCLK5	–	ISC_D4
7	PB31	LCDDAT20	A20	FLEXCOM0_IO4	TWD0	–	ISC_D5
8	PC0	LCDDAT21	A23	FLEXCOM0_O1	TWCK0	–	ISC_D6
9	PB20	LCDDAT9	A9	TK0	TIOB3	PCK1	GTX0
10	PB21	LCDDAT10	A10	TF0	TCLK3	FLEXCOM3_IO3	GTX1
11	PB27	LCDDAT16	A16	UTXD0	PDMCLK0	–	ISC_D1
12	PB26	LCDDAT15	A15	URXD0	PDMDAT0	–	ISC_D0
13	PB29	LCDDAT18	A18	FLEXCOM0_IO1	TIOB5	–	ISC_D3
14	PB28	LCDDAT17	A17	FLEXCOM0_IO0	TIOA5	–	ISC_D2
15	PB31	LCDDAT20	A20	FLEXCOM0_IO4	TWD0	–	ISC_D5
16	PB30	LCDDAT19	A19	FLEXCOM0_IO3	TCLK5	–	ISC_D4

.....continued

Pin		SAMA5D27 PIO Muxing Alternates					
No.	Type						
17	PC1	LCDDAT22	A24	CANTX0	SPI1_SPCK	I2SCK0	ISC_D7
18	PC0	LCDDAT21	A23	FLEXCOM0_O1	TWCK0	–	ISC_D6
19	PA22	FLEXCOM1_IO3	D0	TCK	SPI1_SPCK	SDHC1_CK	QSPI0_SCK
20	PA25	FLEXCOM1_IO4	D3	TMS	SPI1_NPCS0	–	QSPI0_IO1
21	PA26	FLEXCOM1_O1	D4	NTRST	SPI1_NPCS1	–	QSPI0_IO2
22	PC3	LCDPWM	NWAIT	TIOA1	SPI1_MISO	I2SWS0	ISC_D9
23	PC2	LCDDAT23	A25	CANRX0	SPI1_MOSI	I2SMCK0	ISC_D8
24	PC6	LCDHSYNC	NCS1	TWD1	SPI1_NPCS2		ISC_HSYNC
25	PC5	LCDVSYNC	NCS0	TCLK1	SPI1_NPCS1	I2SDO0	ISC_VSYNC
26	PC4	LCDDISP	NWR1/NBS1	TIOB1	SPI1_NPCS0	I2SDI0	ISC_PCK
27	PB11	LCDDAT0	A0/NBS0	URXD3	PDMDAT0	–	GRX3
28	PB12	LCDDAT1	A1	UTXD3	PDMCLK0	–	GTX2
29	PC7	LCDPCK	NCS2	TWCK1	SPI1_NPCS3	URXD1	ISC_MCK
30	PB25	LCDDAT14	A14	RF0	–	FLEXCOM3_IO1	ISC_D11
31	PB24	LCDDAT13	A13	RK0	TCLK2	FLEXCOM3_IO4	ISC_D10
32	PC8	LCDDEN	NANDRDY	FIQ	PCK0	UTXD1	ISC_FIELD
33	PD31	ADTRG	NTRST	IRQ	TCLK3	PCK0	–
34	PC26	LCDDAT22	–	GTX2	CANTX1		A15
35	GND	–	–	–	–	–	–
36	GND	–	–	–	–	–	–

Figure 6-49. J16 Connector

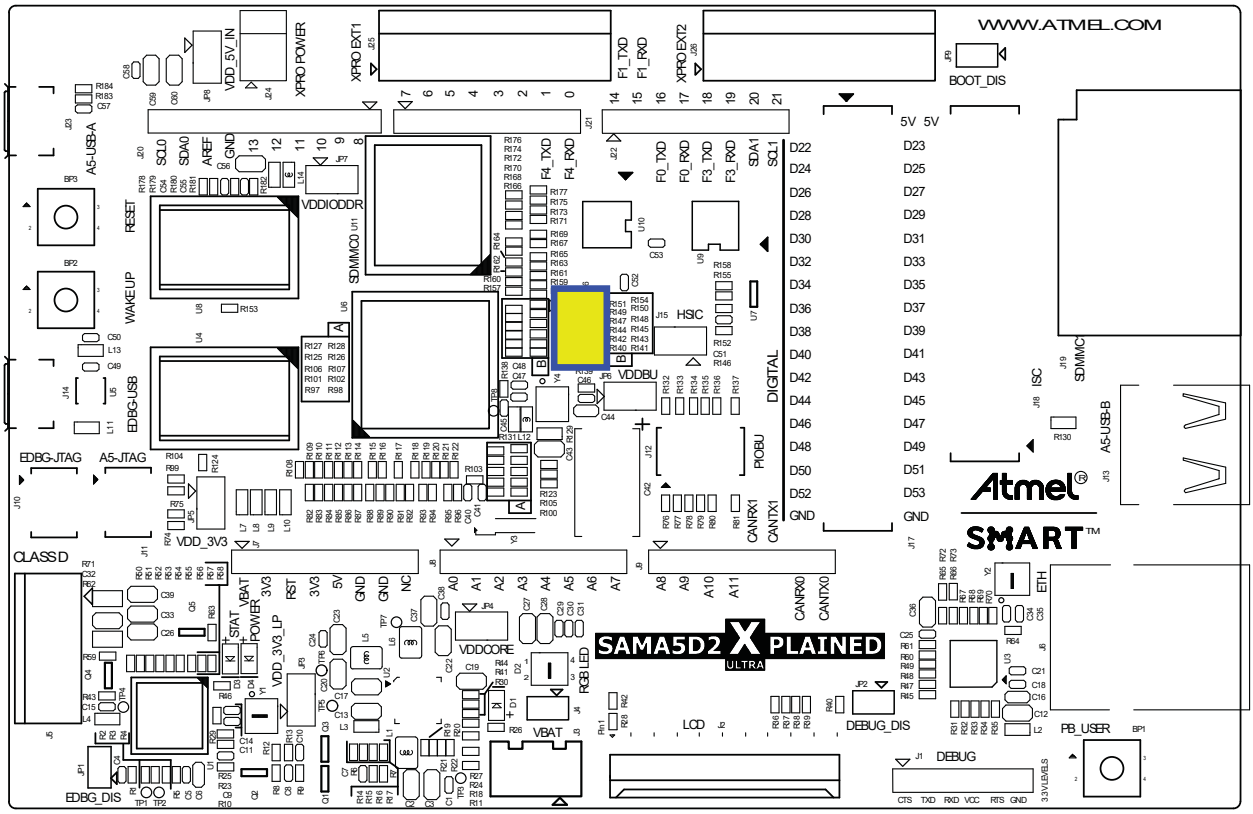


Table 6-24. J16 Connector Signals

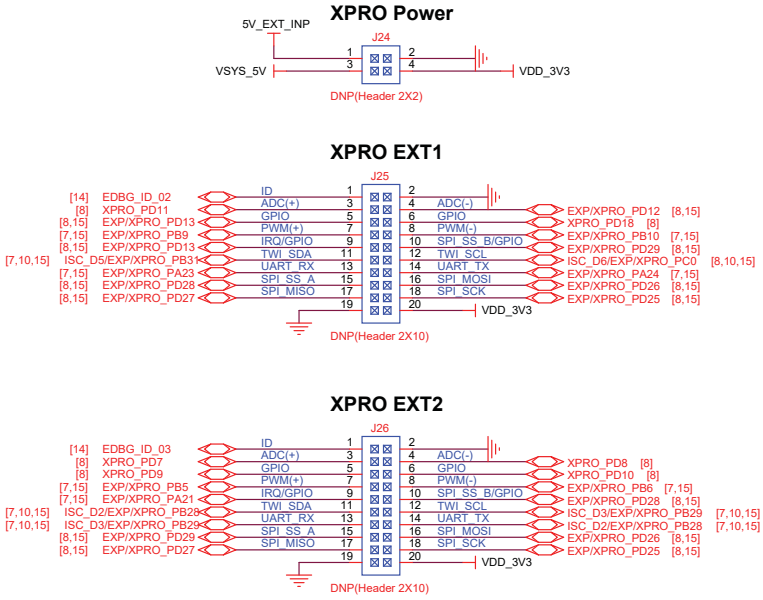
Pin		SAMA5D27 PIO Muxing Alternates					
No.	Type						
1	PD27	SPI1_MISO	TCK	FLEXCOM2_IO2	–	–	AD8
2	POWER (1)	–	–	–	–	–	–
3	PD25	SPI1_SPCK	–	FLEXCOM4_O1	–	–	AD6
4	PD26	SPI1_MOSI	–	FLEXCOM2_IO1	–	–	AD7
5	nRST	–	–	–	–	–	–
6	GND	–	–	–	–	–	–

Note: 5V/3.3V selected by resistors

6.5.2 XPRO

The SAMA5D2C-XULT board features three connectors to interface with standard Xplained PRO extensions.

Figure 6-50. XPRO Connectors Schematics



The standard extension headers include common signals.

Figure 6-51. XPRO Connectors

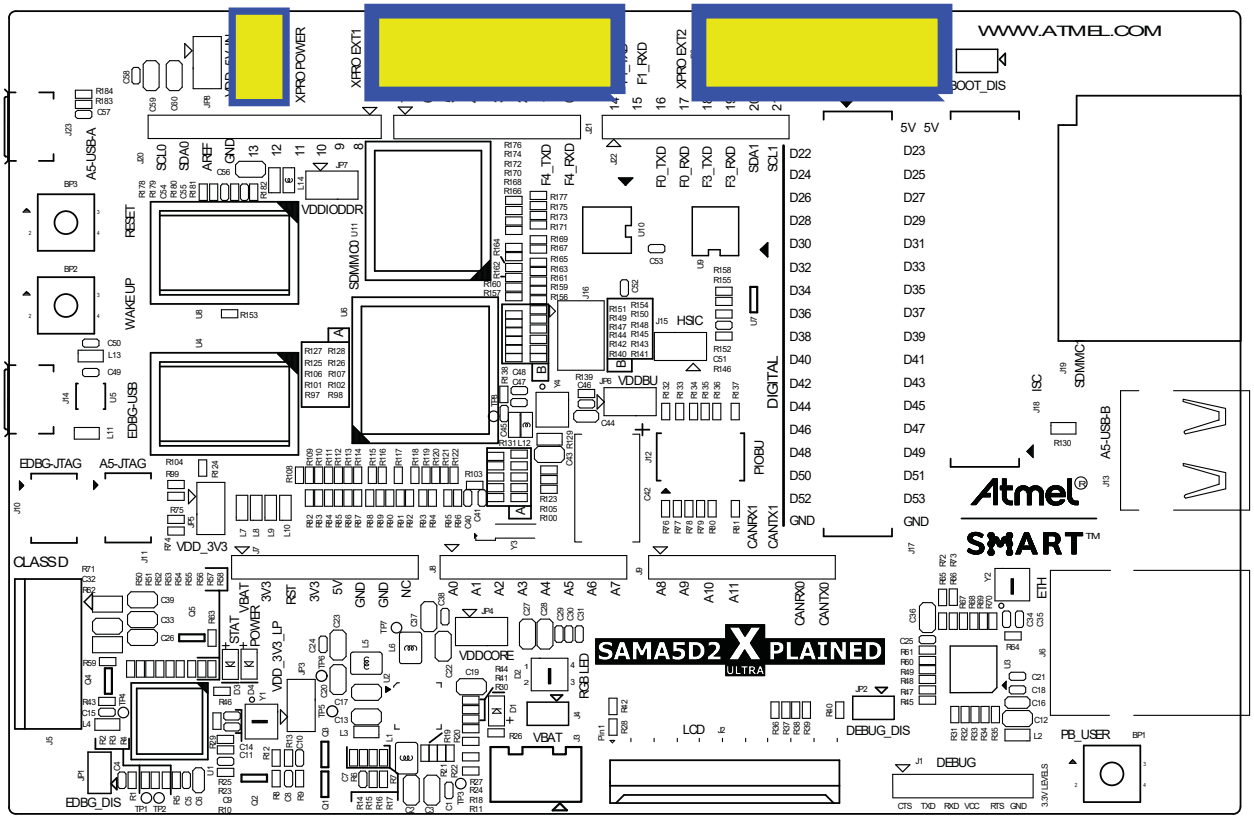


Table 6-25. XPRO Power Connector J24 Signal Descriptions

Signal	Pin No.		Signal
EXP_5V	1	2	GND

.....continued

Signal	Pin No.		Signal
VDD_5V	3	4	VSYS_3V3

Table 6-26. XPRO EXT1 Connector J25 Signal Descriptions

Pin		XPRO Signal	SAMA5D27 PIO Muxing Alternates						
No.	Type								
1	-	EDBG_ID_02	–	–	–	–	–	–	–
2	GND	–	–	–	–	–	–	–	–
3	PD11	ADC(+)	TIOA1	PCK2	UTMI_LS0	GRXDV	ISI_D4	ISI_MCK	PTCCOL0
4	PD12	ADC(-)	TIOB1	FLEXCOM4_IO0	UTMI_LS1	GRXER	ISI_D5	ISI_D4	PTCCOL1
5	PD13	GPIO	TCLK1	FLEXCOM4_IO1	UTMI_CDRCPSEL0	GRX0	ISI_D6	ISI_D5	PTCCOL2
6	PD18	GPIO	NTRST	–	–	GMDIO	ISI_FIELD	ISI_D10	PTCCOL7
7	PB9	PWM(+)	TIOA3	D14	PWMFI1	QSPI1_IO2	–	GCOL	–
8	PB10	PWM(-)	TIOB3	D15	PWMEXTRG1	QSPI1_IO3	–	GRX2	–
9	PD13	IRQ/GPIO	TCLK1	FLEXCOM4_IO2	UTMI_CDRCPSEL0	GRX0	ISI_D6	ISI_D5	PTCCOL2
10	PD29	SPI_SS_B/GPIO	SPI1_NPCS1	TDO	FLEXCOM2_IO4	TIOA3	TWD0	–	AD10
11	PB31	TWI_SDA	LCDDAT20	A20	FLEXCOM0_IO4	TWD0	–	ISI_D5	–
12	PC0	TWI_SCL	LCDDAT21	A23	FLEXCOM0_O1	TWCK0	–	ISI_D6	–
13	PA23	UART_RX	FLEXCOM1_IO2	D1	TDI	SPI1_MOSI	–	QSPI0_CS	–
14	PA24	UART_TX	FLEXCOM1_IO1	D2	TDO	SPI1_MISO	–	QSPI0_IO0	–
15	PD28	SPI_SS_A	SPI1_NPCS0	TDI	FLEXCOM2_IO3	–	–	–	AD9
16	PD26	SPI_MOSI	SPI1_MOSI	–	FLEXCOM2_IO1	–	–	–	AD7
17	PD27	SPI_MISO	SPI1_MISO	TCK	FLEXCOM2_IO2	–	–	–	AD8
18	PD25	SPI_SCK	SPI1_SPCK	–	FLEXCOM4_O1	–	–	–	AD6
19	GND	–	–	–	–	–	–	–	–
20	3V3	–	–	–	–	–	–	–	–

Table 6-27. XPRO EXT2 Connector J26 Signal Descriptions

Pin		XPRO Signal	SAMA5D27 PIO Muxing Alternates						
No.	Type								
1	–	EDBG_ID_03	–	–	–	–	–	–	–
2	GND	–	–	–	–	–	–	–	–
3	PD7	ADC(+)	TDI	–	UTMI_RXVAL	GTX2	ISI_D0	NWR1/NBS1	PTCROW4
4	PD8	ADC(-)	TDO	–	UTMI_RXERR	GTX3	ISI_D1	NANDRDY	PTCROW5
5	PD9	GPIO	TMS	–	UTMI_RXACT	GTXCK	ISI_D2	–	PTCROW6
6	PD10	GPIO	NTRST	–	UTMI_HDIS	GTXEN	ISI_D3	–	PTCROW7
7	PB5	PWM(+)	TCLK2	D10	PWMH2	QSPI1_SCK	PTCPORT5	GTSUCOMP	–
8	PB6	PWM(-)	TIOA2	D11	PWML2	QSPI1_CS	PTCPORT6	GTXER	–

.....continued

Pin		XPRO Signal	SAMA5D27 PIO Muxing Alternates						
No.	Type								
9	PA21	IRQ/GPIO	IRQ	PCK2	–	TCLK0	SDHC1_DAT3	NANDRDY	–
10	PD28	SPI_SS_B/GPIO	SPI1_NPCS0	TDI	FLEXCOM2_IO3	–	–	–	AD9
11	PB28	TWI_SDA	LCDDAT17	A17	FLEXCOM0_IO1	TIOA5	–	ISI_D2	–
12	PB29	TWI_SCL	LCDDAT18	A18	FLEXCOM0_IO2	TIOB5	–	ISI_D3	–
13	PB29	UART_RX	LCDDAT18	A18	FLEXCOM0_IO2	TIOB5	–	ISI_D3	–
14	PB28	UART_TX	LCDDAT17	A17	FLEXCOM0_IO1	TIOA5	–	ISI_D2	–
15	PD29	SPI_SS_A	SPI1_NPCS1	TDO	FLEXCOM2_IO4	TIOA3	TWD0	–	AD10
16	PD26	SPI_MOSI	SPI1_MOSI	–	FLEXCOM2_IO1	–	–	–	AD7
17	PD27	SPI_MISO	SPI1_MISO	TCK	FLEXCOM2_IO2	–	–	–	AD8
18	PD25	SPI_SCK	SPI1_SPCK	–	FLEXCOM4_O1	–	–	–	AD6
19	GND	–	–	–	–	–	–	–	–
20	3V3	–	–	–	–	–	–	–	–

7. Board Schematics

This section contains the following schematics:

- Block Diagram
- PIO Muxing Table
- Power Supply
- SAMA5D27 – Power
- SAMA5D27 – DDR3
- SAMA5D27 – PIOA and PIOB
- SAMA5D27 – PIOC and PIOD
- SAMA5D27 – SYS, Tamper, and Debug
- USB, ISC, and LCD
- Serial Flash, LEDS, Push Button and ClassD
- Ethernet
- SD and eMMC
- EDBG
- Expansion and XPRO Connectors

Important: Design Reuse Recommendation
In case the memory or PIO busses go to multiple destinations, series resistors must be added. These resistors must be located at the beginning of each branch, as close as possible to the MPU.

In case these connections are point-to-point, the branch resistors found in the following schematics can be removed.

In all cases, it is recommended to always perform routing simulation to check signal integrity prior to PCB manufacturing.

Figure 7-1. Block Diagram

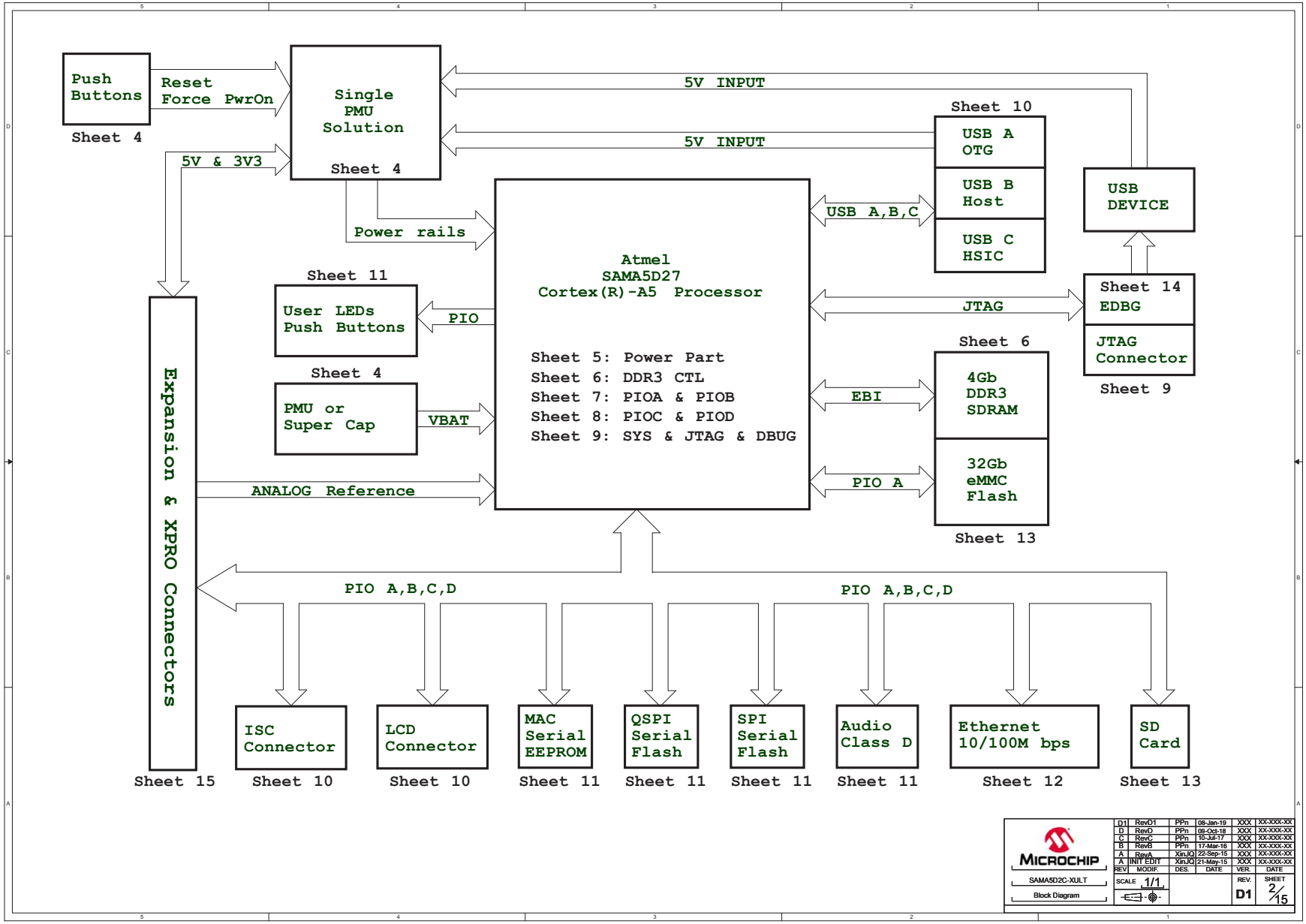


Figure 7-2. PIO Muxing Table

PIO Muxing & Jumper setting

LCD	
ID_SYS	1
GND	2
NC	3
NC	4
LCDDAT2	5
LCDDAT3	6
GND	7
LCDDAT4	8
LCDDAT5	9
LCDDAT6	10
LCDDAT7	11
GND	12
NC	13
NC	14
LCDDAT10	15
LCDDAT11	16
GND	17
LCDDAT12	18
LCDDAT13	19
LCDDAT14	20
LCDDAT15	21
GND	22
NC	23
NC	24
LCDDAT18	25
LCDDAT19	26
GND	27
LCDDAT20	28
LCDDAT21	29
LCDDAT22	30
LCDDAT23	31
GND	32
LCDPCK	33
LCDVSYNC	34
LCDHSYNC	35
LCDDEN	36
SPI1_SPCK/AD0_XP	37
SPI1_MOSI/AD1_XM	38
SPI1_MISO/AD2_YP	39
SPI1_NPCS0/AD3_YM	40
LCDDISP	41
TWD1	42
TWCK1	43
IRQ1	44
IRQ2	45
LCDPWM	46
NRST	47
VCC	48
VCC	49
GND	50

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOB	USAGE	PIOC	USAGE
PA0	SDHC0_CK	PA16	SPI0_MISO/EXP	PB0	LED_BLUE/LCD_ID	PB16	ETH_GRXDV	PC0	ISC_D6/EXP/XPRO
PA1	SDHC0_CMD	PA17	SPI0_CS0/EXP	PB1	CLASSD_R0	PB17	ETH_GRXER	PC1	ISC_D7/SPI1_SPCK/EXP
PA2	SDHC0_DAT0	PA18	SDHC1_DAT0/EXP	PB2	CLASSD_R1	PB18	ETH_GRX0	PC2	ISC_D8/SPI1_MOSI/EXP
PA3	SDHC0_DAT1	PA19	SDHC1_DAT1/EXP	PB3	CLASSD_R2	PB19	ETH_GRX1	PC3	ISC_D9/SPI1_MISO/EXP
PA4	SDHC0_DAT2	PA20	SDHC1_DAT2/EXP	PB4	CLASSD_R3	PB20	ETH_GTX0/EXP	PC4	ISC_PCK/SPI1_NPCS0/EXP
PA5	SDHC0_DAT3	PA21	SDHC1_DAT3/EXP/XPRO	PB5	LED_GREEN/EXP/XPRO	PB21	ETH_GTX1/EXP	PC5	ISC_VSYNC/EXP
PA6	SDHC0_DAT4	PA22	SDHC1_CK/QSPI0_SCK/EXP	PB6	LED_RED/EXP/XPRO	PB22	ETH_GMDC/EXP	PC6	ISC_HSYNC/EXP
PA7	SDHC0_DAT5	PA23	QSPI0_CS/EXP/XPRO	PB7	LCD_IRQ1	PB23	ETH_GMDIO/EXP	PC7	ISC_MCK/EXP
PA8	SDHC0_DAT6	PA24	QSPI0_IO0/EXP/XPRO	PB8	LCD_IRQ2	PB24	ISC_D10/EXP	PC8	PMIC_LBO/EXP
PA9	SDHC0_DAT7	PA25	QSPI0_IO1/EXP	PB9	USER_PB/EXP/XPRO	PB25	ISC_D11/EXP	PC9	ETH_INT
PA10	SDHC0_RSTN	PA26	QSPI0_IO2/EXP	PB10	USBB_EN5V/EXP/XPRO	PB26	ISC_D0/EXP	PC10	LCD_DAT2/EXP
PA11	SDHC0_VDDSEL	PA27	QSPI0_IO3	PB11	ISC_RST/EXP	PB27	ISC_D1/EXP	PC11	LCD_DAT3/EXP
PA12	PMIC_CHGLEV	PA28	SDHC1_CMD	PB12	ISC_PWD/EXP	PB28	ISC_D2/EXP/XPRO	PC12	LCD_DAT4
PA13	SDHC0_CD	PA29	USBB_OVCUR	PB13	PMIC_IRQ	PB29	ISC_D3/EXP/XPRO	PC13	LCD_DAT5
PA14	SPI0_SPCK/EXP	PA30	SDHC1_CD	PB14	ETH_GTXCK	PB30	ISC_D4/EXP	PC14	LCD_DAT6
PA15	SPI0_MOSI/EXP	PA31	USBA_VBUS Detection	PB15	ETH_GTXEN	PB31	ISC_D5/EXP/XPRO	PC15	LCD_DAT7

PIOC	USAGE	PIOD	USAGE	PIOD	USAGE
PC16	LCD_DAT10	PD0	LCD_PCK	PD16	JTAG_TDO
PC17	LCD_DAT11	PD1	LCD_DEN	PD17	JTAG_TMS
PC18	LCD_DAT12	PD2	DBGU_URXD1	PD18	XPRO
PC19	LCD_DAT13	PD3	DBGU_UTXD1	PD19	LCD_XP/EXP
PC20	LCD_DAT14	PD4	LCD/EEP/ISC/EXP_TWD1	PD20	LCD_XM/EXP
PC21	LCD_DAT15	PD5	LCD/EEP/ISC/EXP_TWCK1	PD21	LCD_YP/PMIC_TWD0/EXP
PC22	LCD_DAT18	PD6	EXP	PD22	LCD_YM/PMIC_TWCK0/EXP
PC23	LCD_DAT19	PD7	XPRO	PD23	EXP
PC24	LCD_DAT20	PD8	XPRO	PD24	EXP
PC25	LCD_DAT21	PD9	XPRO	PD25	EXP/XPRO
PC26	LCD_DAT22/EXP	PD10	XPRO	PD26	EXP/XPRO
PC27	LCD_DAT23/EXP	PD11	XPRO	PD27	EXP/XPRO
PC28	LCD_PWM	PD12	EXP/XPRO	PD28	EXP/XPRO
PC29	LCD_DISP	PD13	EXP/XPRO	PD29	EXP/XPRO
PC30	LCD_VSYNC	PD14	JTAG_TCK	PD30	EXP
PC31	LCD_HSYNC	PD15	JTAG_TDI	PD31	EXP

JUMPER DESCRIPTION		
PART	DEFAULT	FUNCTION
JP1	OPEN	Disable EDBG
JP2	OPEN	Disable Debug
JP3	CLOSE	I VDD_3V3_LP Measurement
JP4	CLOSE	I VDDCORE Measurement
JP5	CLOSE	I VDDISC+VDDIOP0/1/2 Measurement
JP6	CLOSE	I VDDBU Measurement
JP7	CLOSE	I VDDIODDR_MPU Measurement
JP8	CLOSE	I VDD_5V_IN Measurement
JP9	OPEN	Disable CS of SPI&QSPI&eMMC Memory

MICROCHIP

SAMA5D2C-XULT

PIO Muxing

REV	MODIF.	DES.	DATE	VER.
D1	RevD1	PPn	08-Jan-19	XXX
D	RevD	PPn	09-Oct-18	XXX
C	RevC	PPn	10-Jul-17	XXX
B	RevB	PPn	17-Mar-16	XXX
A	RevA	Xin.JQ	22-Sep-15	XXX
A	INIT EDIT	Xin.JQ	21-May-15	XXX

SCALE 1/1

REV. D1

SHEET 3/15

Figure 7-3. Power Supply

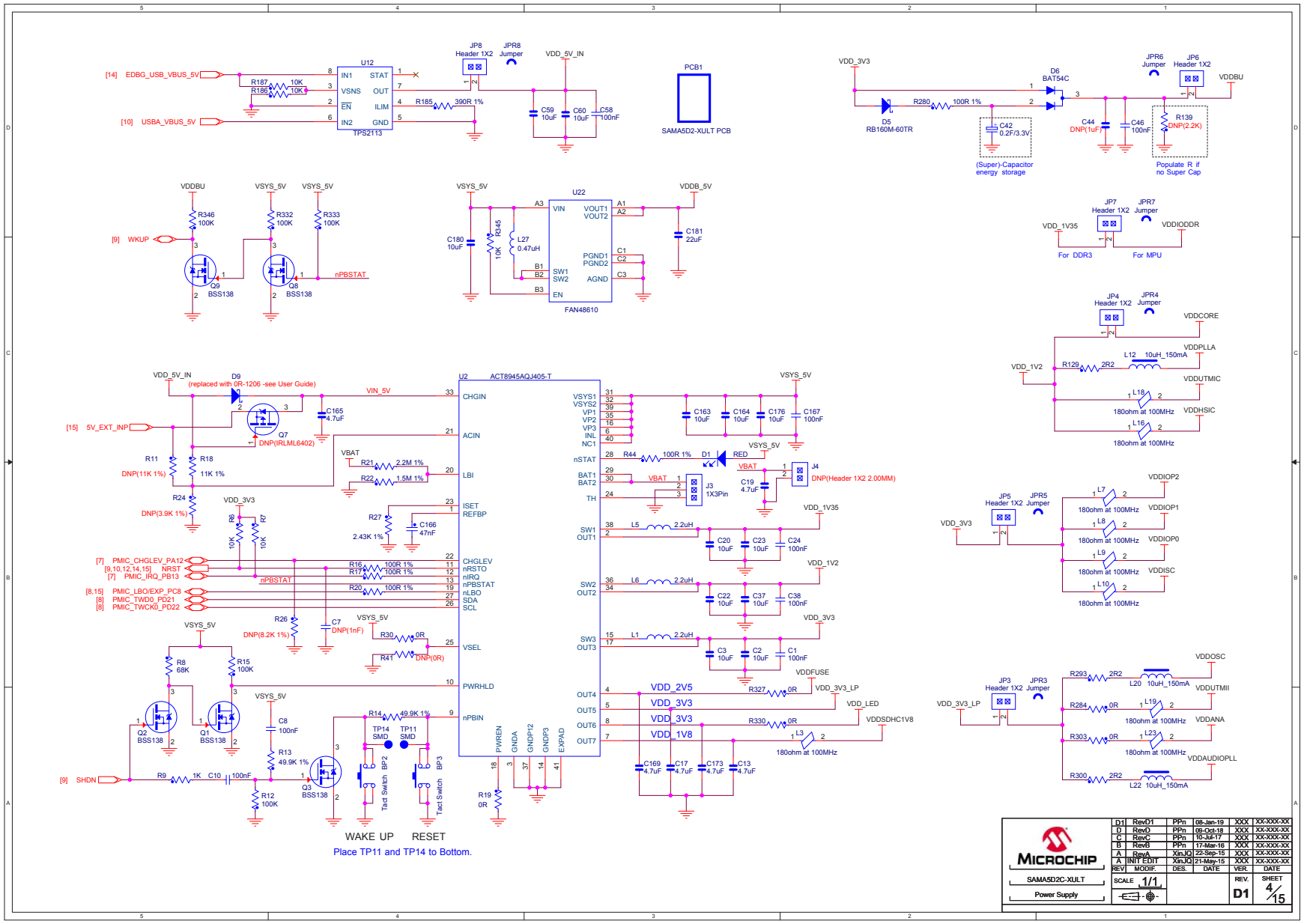


Figure 7-4. SAMA5D27 – Power

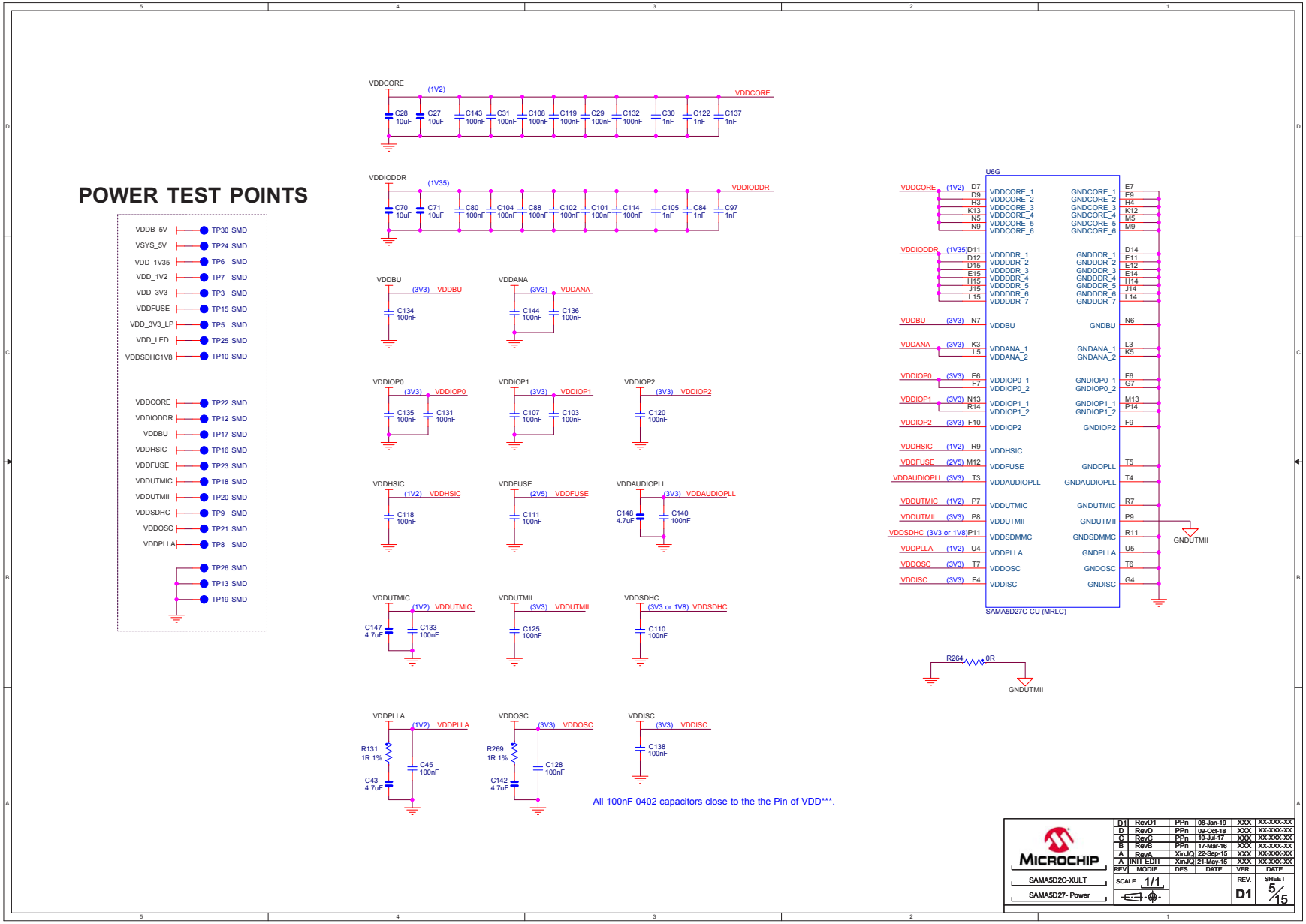


Figure 7-5. SAMA5D27 – DDR3

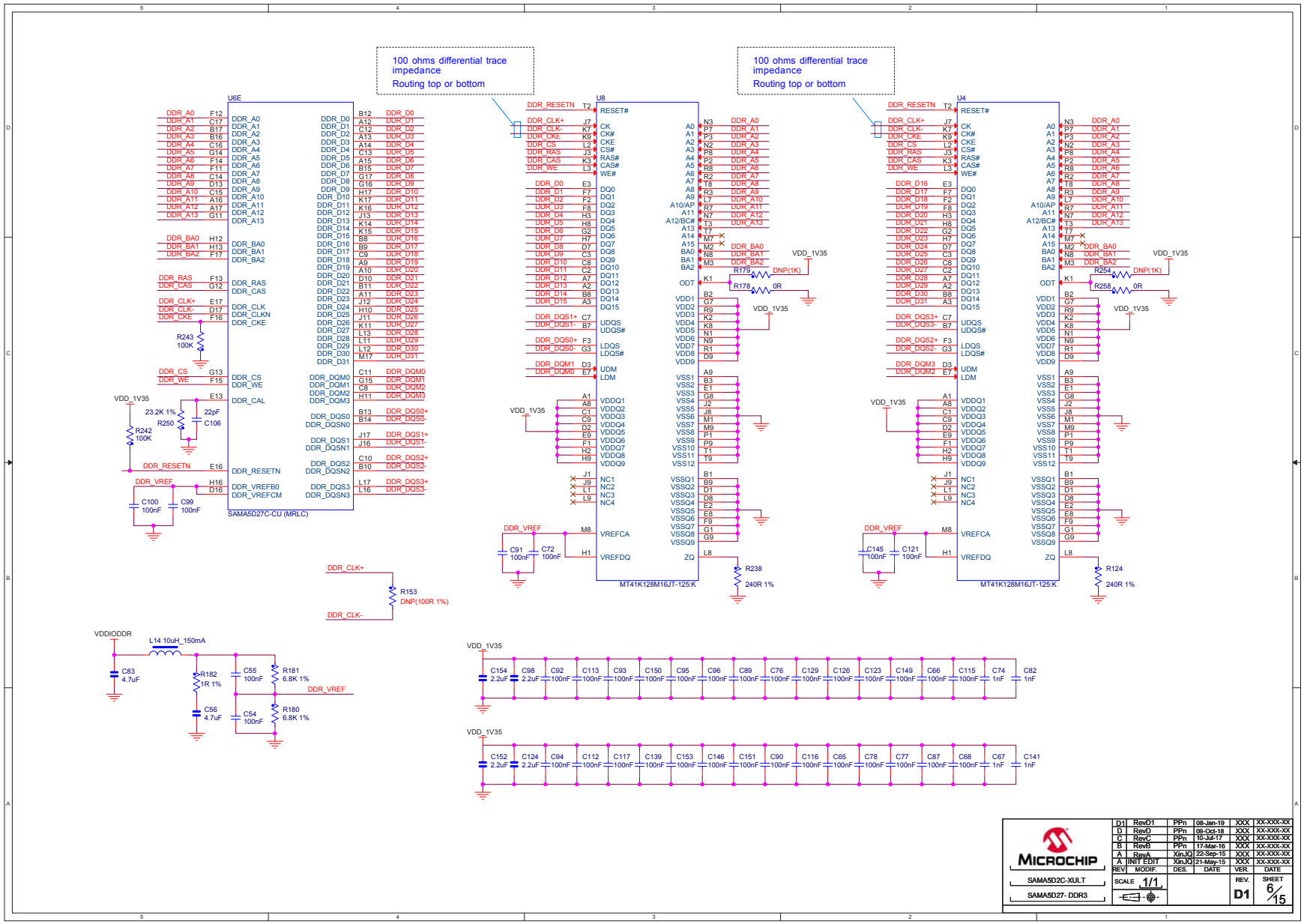


Figure 7-6. SAMA5D27 – PIOA and PIOB

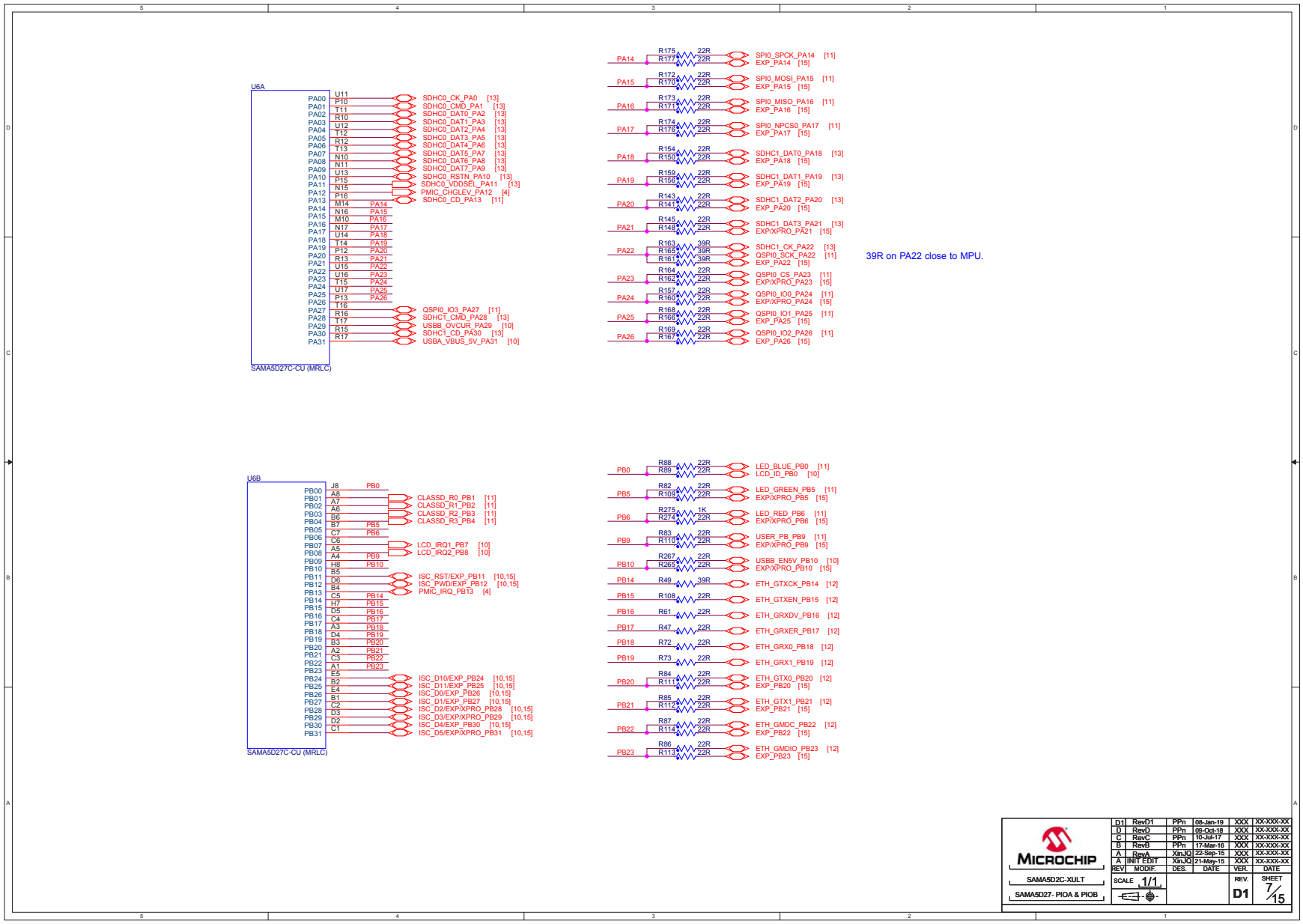


Figure 7-7. SAMA5D27 – PIOC and PIOD

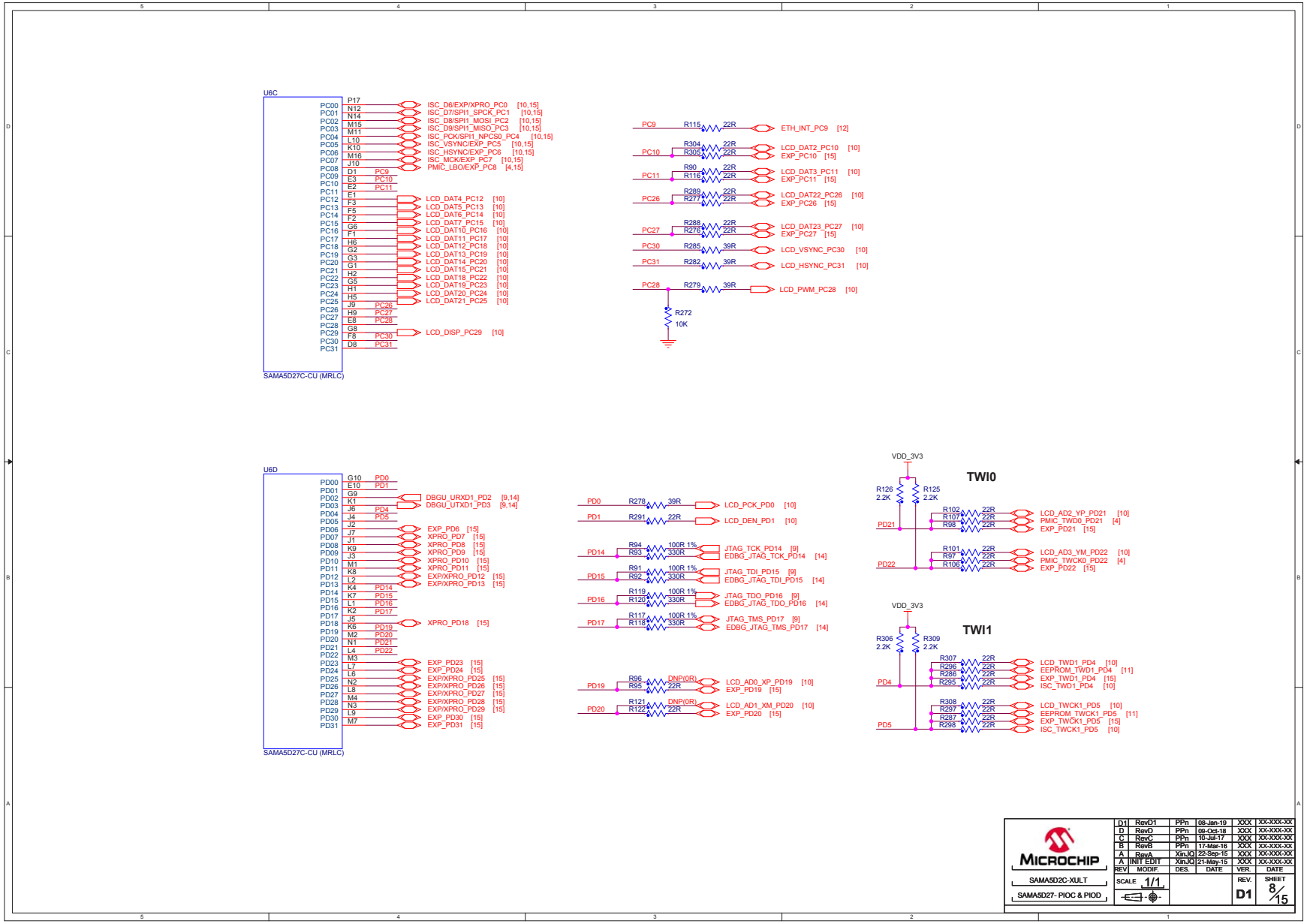


Figure 7-8. SAMA5D27 – SYS, Tamper, and Debug

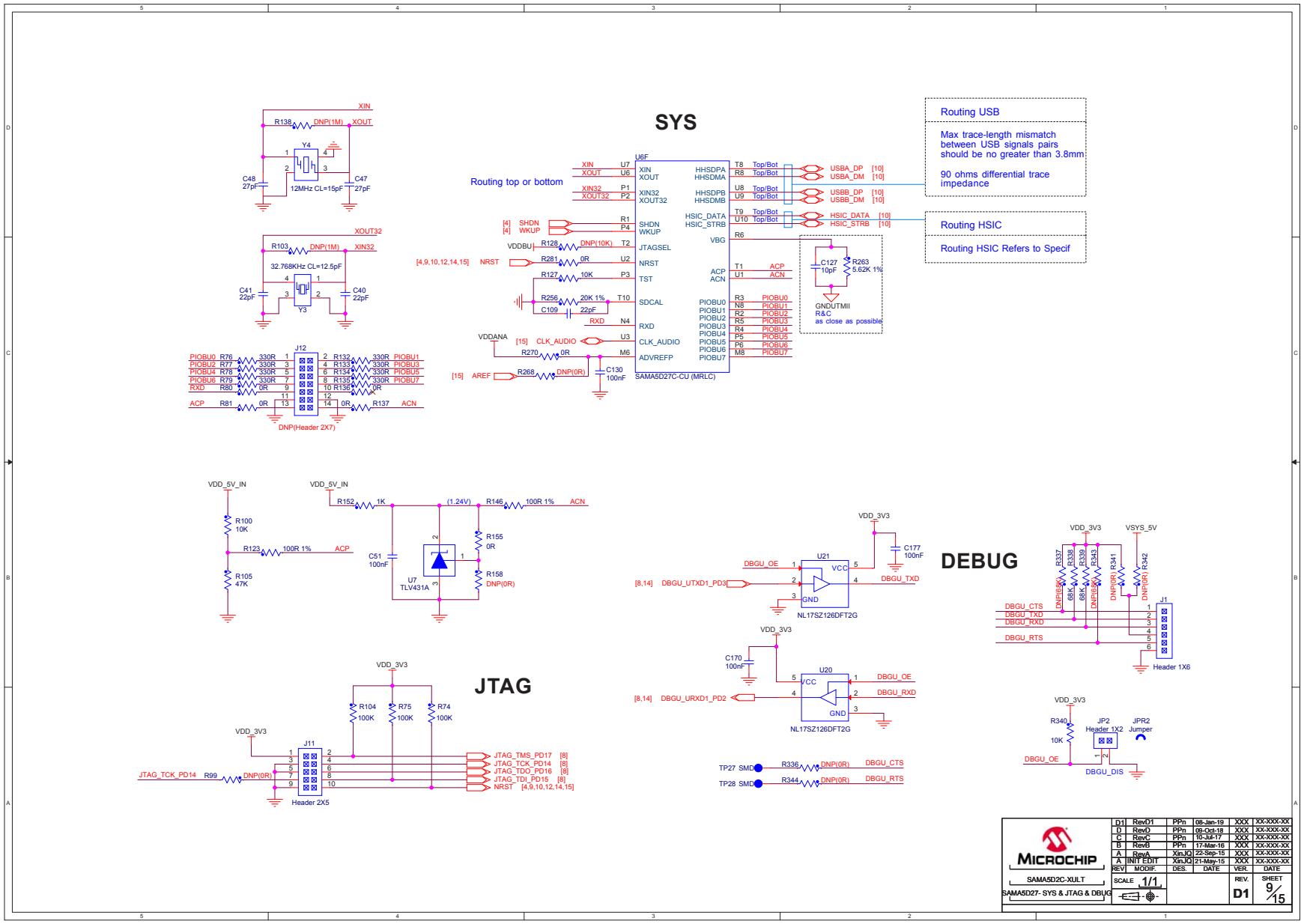


Figure 7-9. USB, ISC, and LCD

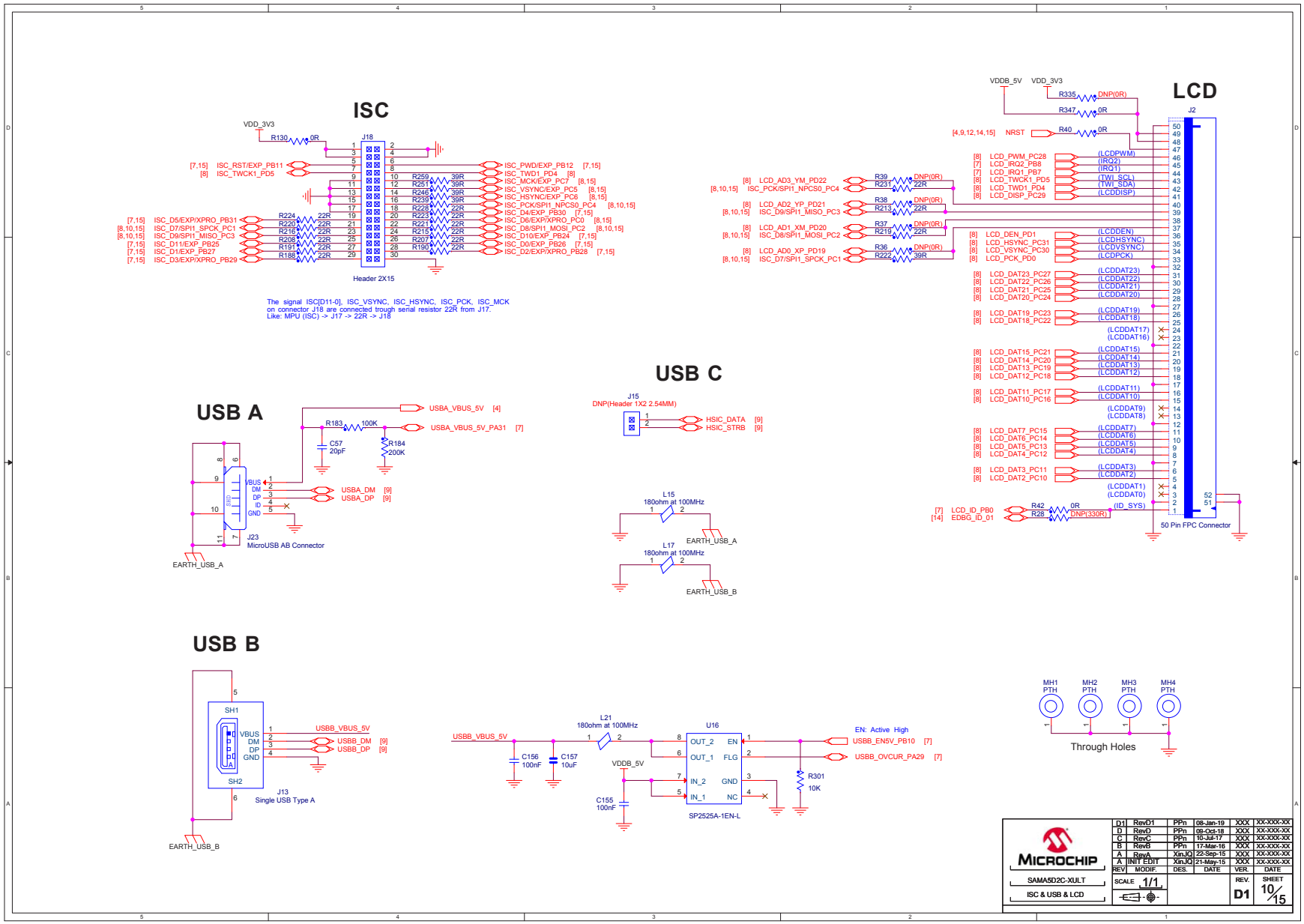


Figure 7-10. Serial Flash, LEDS, Push Button and ClassD

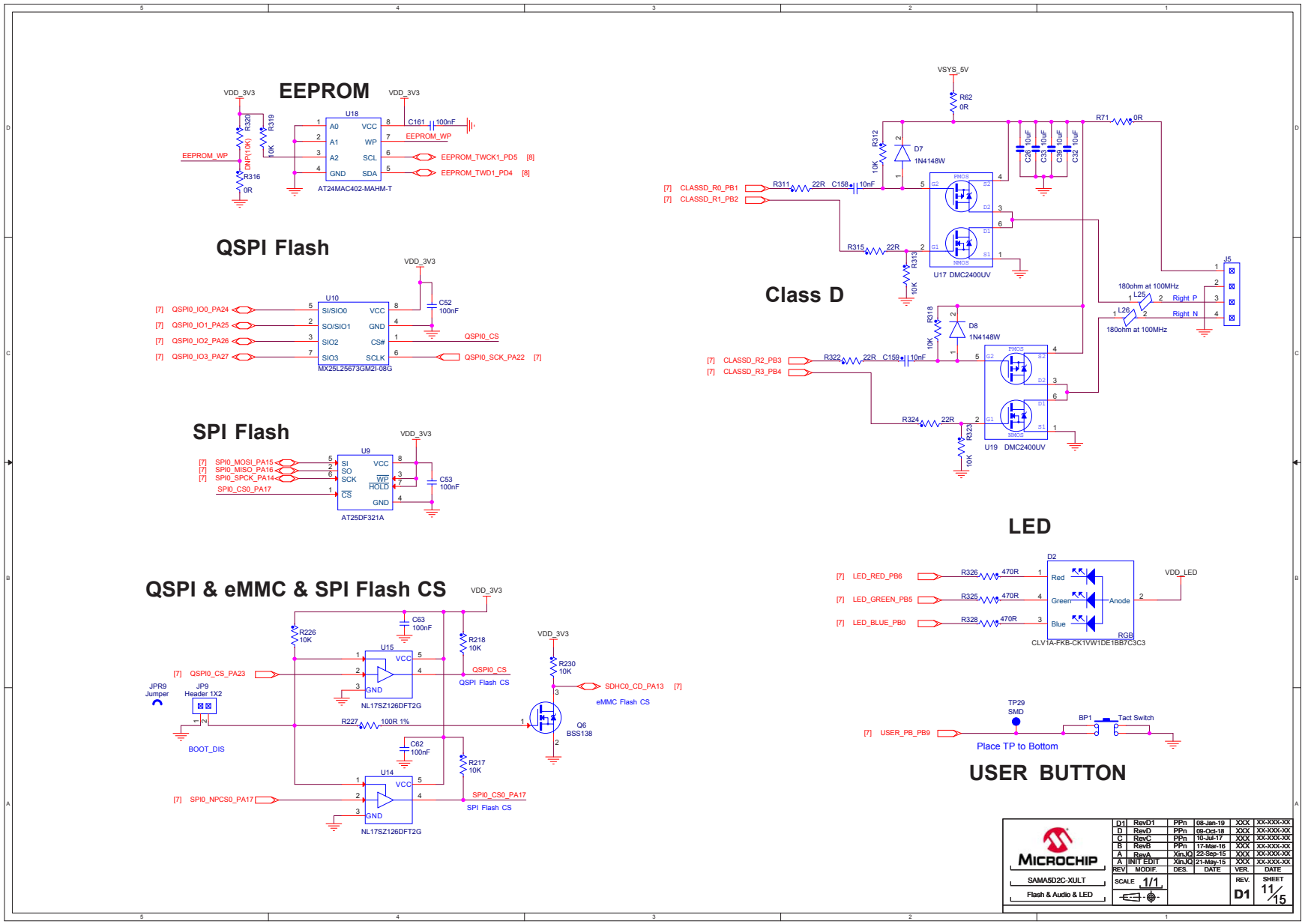


Figure 7-11. Ethernet

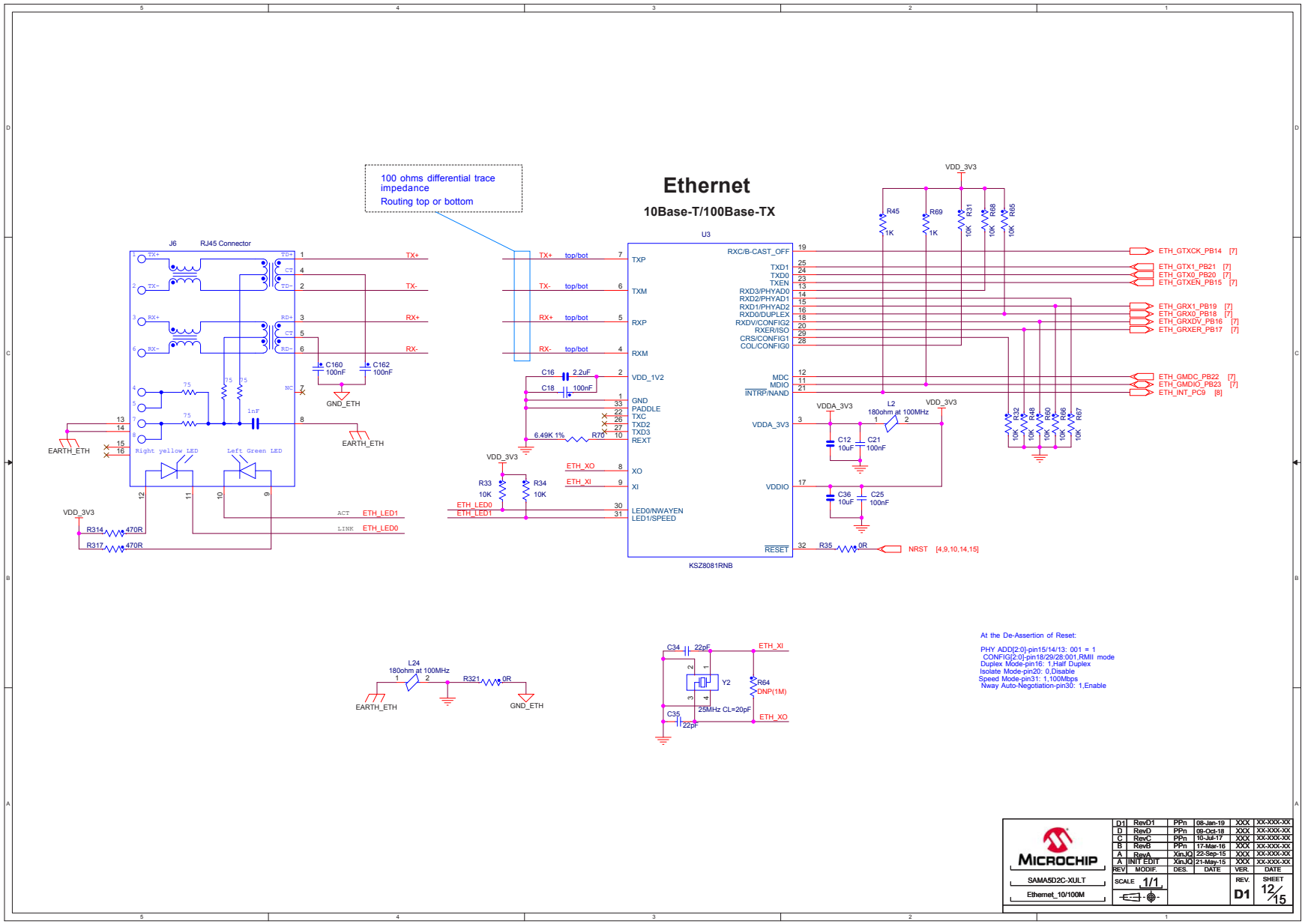


Figure 7-12. SD and eMMC

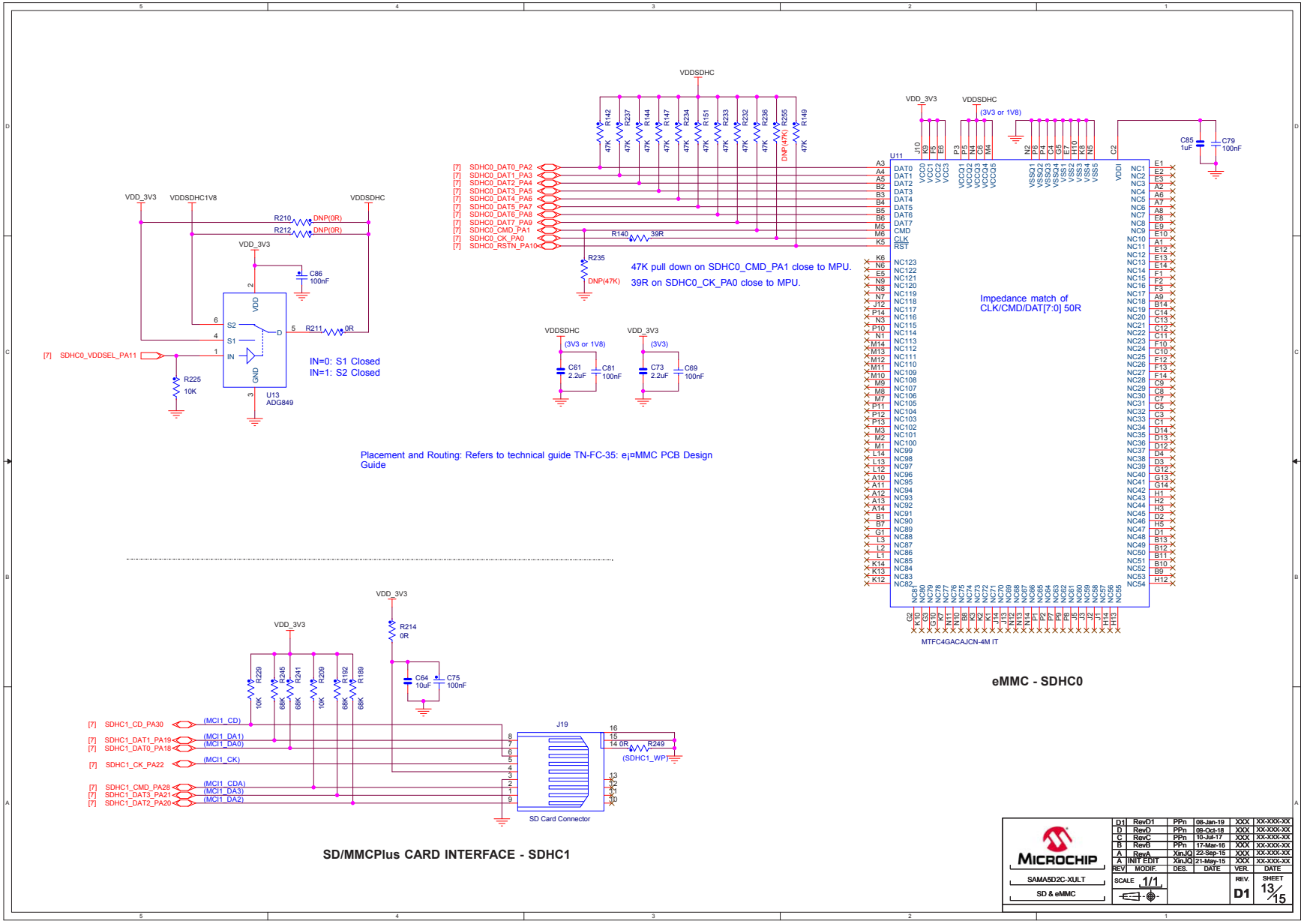


Figure 7-13. EDBG

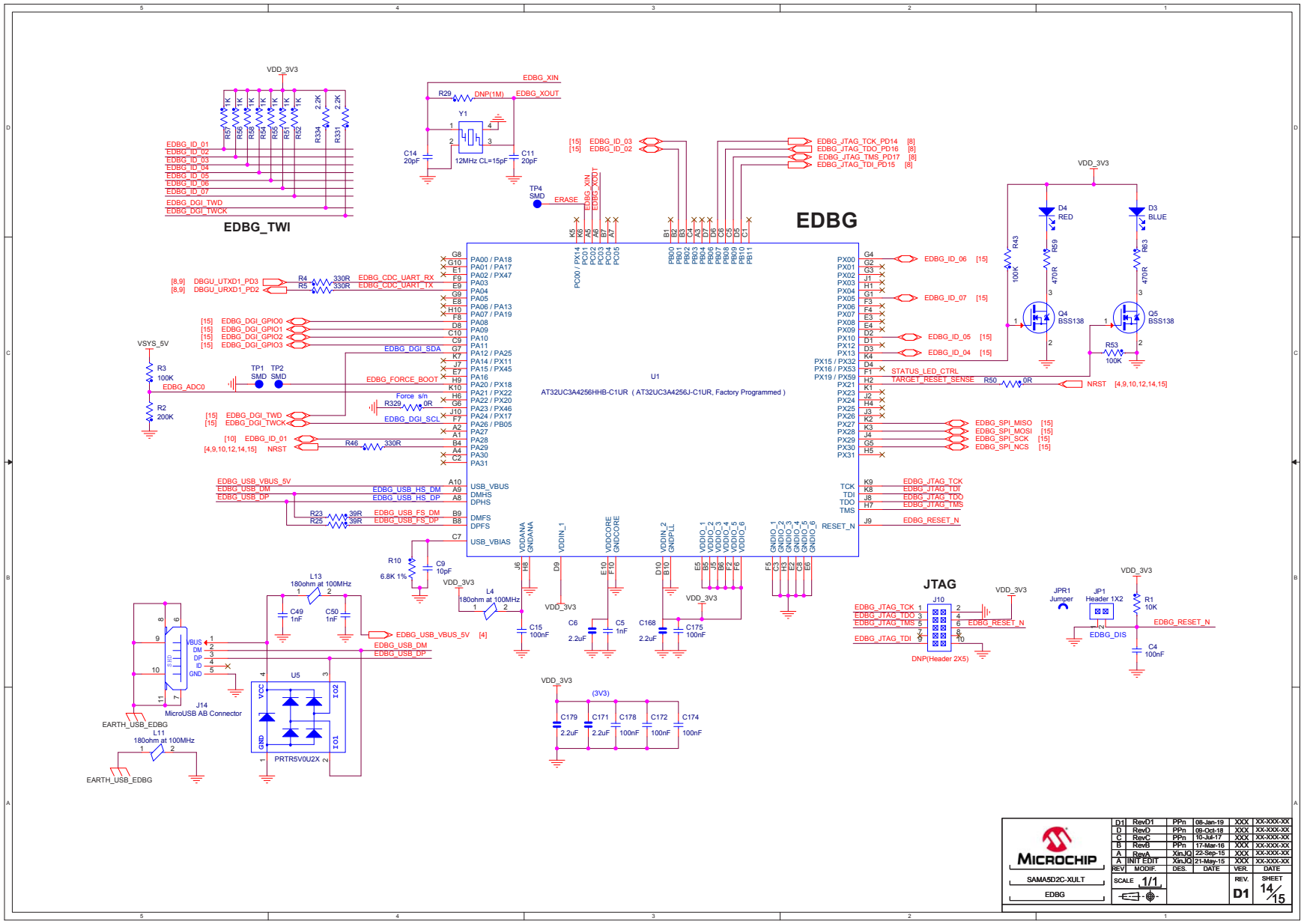
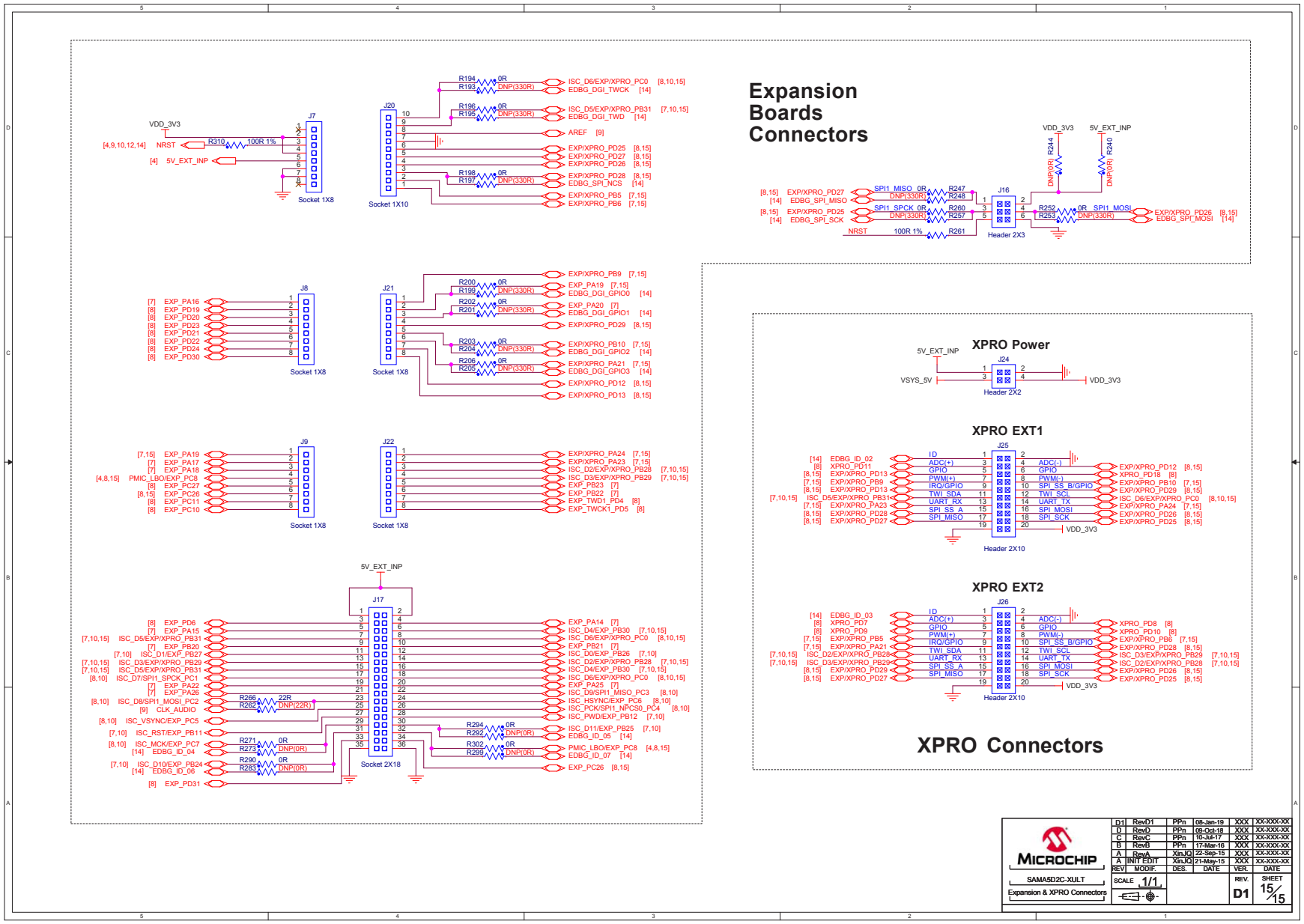


Figure 7-14. Expansion and XPRO Connectors



8. Errata

8.1 NRST

Issue: Pullup R6 is connected to VDD_3V3

Workaround: Connect pullup R6 to VDDBU.

8.2 nLBO

Issue: No pullup on nLBO

Workaround: Add pullup 10K to nLBO output.

8.3 R63

Issue: Incorrect R63 resistance in schematic "EDBG"

Workaround: Correct the resistance to 47R.

8.4 R100/R105

Issue: The values of resistors R100/R105 (mounted as a resistive divider on VDD_5V_IN) are swapped. This results in:

- a leakage current path is created from VDD_5V_IN to VDDDU through the ACP pin, and
- the ACP pin is biased around 4V instead of 0.88V, therefore the voltage detection between ACP and CAN does not work

Workaround: Swap R100 and R105.

9. Revision History

Table 9-1. Rev. E – 08/2020

Changes
Updated PD12 and PD13 in XPRO EXT1 Connector J25 Signal Descriptions and J21 Connector Signals.

Table 9-2. Rev. D – 05/2019

Changes
Updated 7. Board Schematics: all schematics regenerated.

Table 9-3. Rev. C – 10/2018

Changes
Document title modified to *SAMA5D2C XULT User's Guide* (was *SAMA5D2 (Rev. C) Xplained Ultra Evaluation Kit User's Guide*)
Updated Figure 6-10.
Changed eMMC reference in section eMMC.
All schematics regenerated.
Added R100/R105 in section Errata.

Table 9-4. Rev. B – 12/2017

Changes
Updated SAMA5D27 – PIOA and PIOB.
Removed Declaration of Conformity.

Table 9-5. Rev. A – 10/2017

Changes
First issue.

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