USB7002

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB7002. These checklist items should be followed when utilizing the USB7002 in a new design. A summary of these items is provided in Section 10.0, "Hardware Checklist Summary," on page 31. Detailed information on these subjects can be found in the corresponding section:

- Section 2.0, "General Considerations"
- Section 3.0, "Power and Bypass Capacitance"
- Section 4.0, "USB Signals"
- Section 5.0, "USB Connectors"
- Section 6.0, "Clock Circuit"
- Section 7.0, "Power and Startup"
- Section 8.0, "External SPI Memory"
- Section 9.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.2 Ground

- The ground pins, **GND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

2.3 USB-IF Compliant USB Connectors

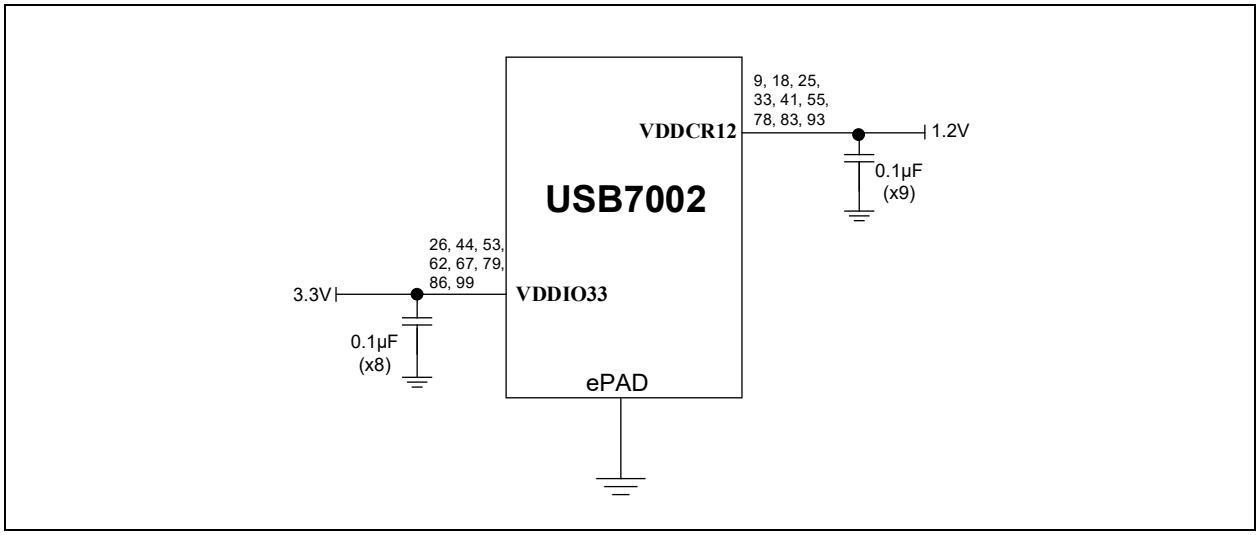
USB-IF certified USB Connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

3.0 POWER AND BYPASS CAPACITANCE

- The analog supplies (**VDD33**) are located on pins 26, 44, 53, 62, 67, 79, 86, and 99, and require a connection to a regulated 3.3V power plane.
- Each **VDD33** pin should include a 0.1 µF capacitor to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The analog supplies (**VDD12**) are located on pins 9, 18, 25, 33, 41, 55, 78, 83, and 93, and require a connection to a regulated 1.2V power plane.
- Each **VDD12** pin should include a 0.1 µF capacitor to decouple the device. The capacitor size should be SMD_0603 or smaller.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



4.0 USB SIGNALS

4.1 Upstream Port USB Signals

- **USB2UP_DP** (pin 89): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP[1] pin of a USB connector.
- **USB2UP_DM** (pin 90): This pin is the negative (–) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM[1] pin of a USB connector.
- **USB3UP_TXDPA** (pin 91): This pin is the positive (+) signal of the upstream USB3.1 'Side A' transmitter (TX) differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX+ (or TX–)[2] pin of the USB connector.
- **USB3UP_TXDMA** (pin 92): This pin is the negative (–) signal of the upstream USB3.1 'Side A' TX differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX– (or TX+)[2] pin of the USB connector.
- **USB3UP_RXDPA** (pin 94): This pin is the positive (+) signal of the upstream USB3.1 'Side A' receiver (RX) differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the RX+ (or RX–)[2] pin of the USB connector.
- **USB3UP_RXDMA** (pin 95): This pin is the negative (–) signal of the upstream USB3.1 'Side A' RX differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the RX– (or RX+)[2] pin of the USB connector.
- **USB3UP_TXDPB** (pin 81): This pin is the positive (+) signal of the upstream USB3.1 'Side B' TX differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX+ (or TX–)[2] pin of the USB connector.
- **USB3UP_TXDMB** (pin 82): This pin is the negative (–) signal of the upstream USB3.1 'Side B' TX differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX– (or TX+)[2] pin of the USB connector.
- **USB3UP_RXDPB** (pin 84): This pin is the positive (+) signal of the upstream USB3.1 'Side B' RX differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the RX+ (or RX–)[2] pin of the USB connector.

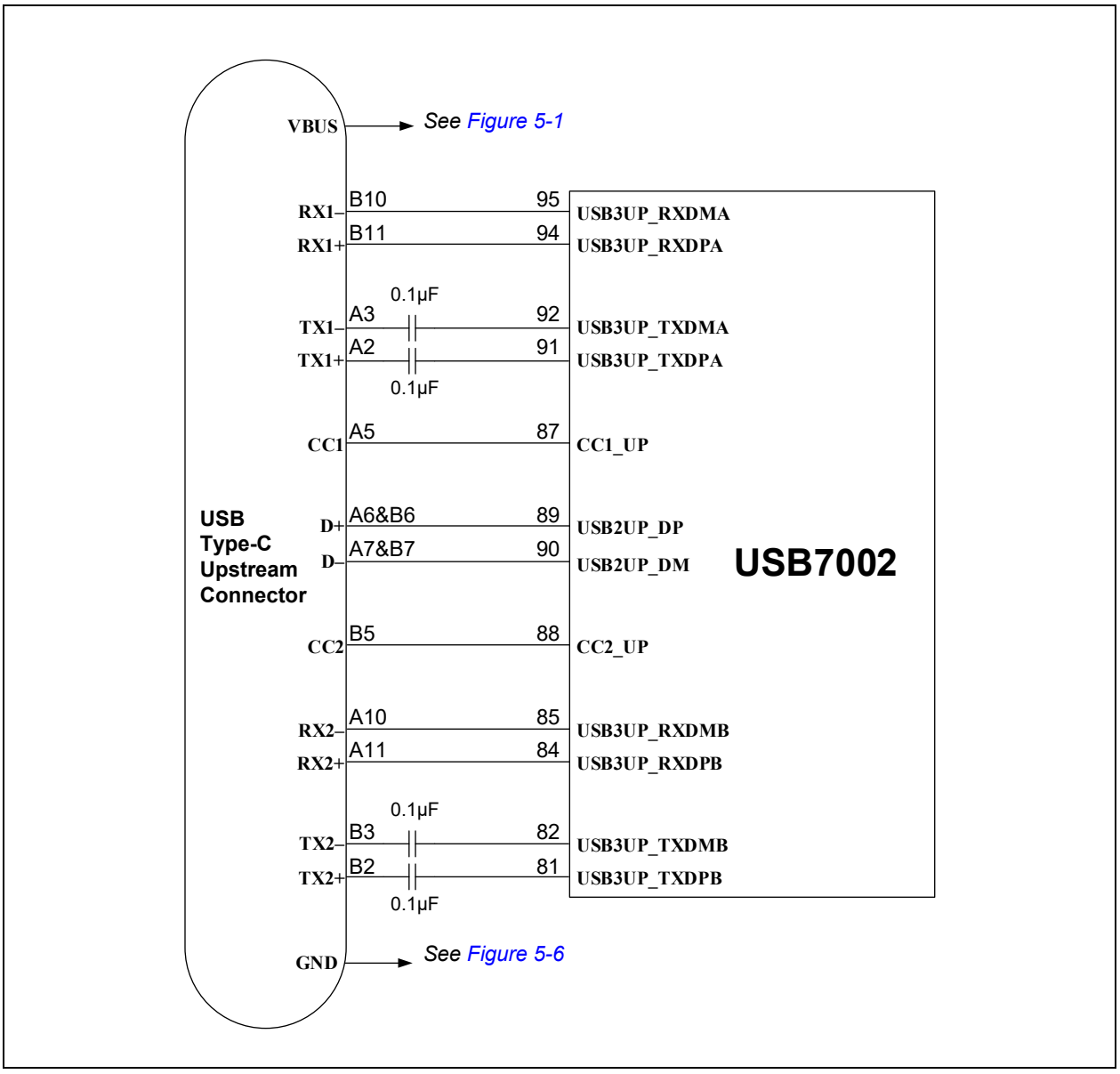
- **USB3UP_RXDMB** (pin 85): This pin is the negative (–) signal of the upstream USB3.1 'Side B' receiver (RX) differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the RX– (or RX+)[2] pin of the USB connector.
- **CC1_UP** (pin 87): This pin is used to detect a USB Type-C connection and insertion orientation. This should connect directly to the CC1 pin of the USB Type-C connector.
- **CC2_UP** (pin 88): This pin is used to detect a USB Type-C connection and insertion orientation. This should connect directly to the CC2 pin of the USB Type-C connector.

Note 1: The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via One-Time Programmable (OTP) or SMBus/I^{2}C configuration registers.

2: A standard feature of USB3.1 is automatic polarity detection and correction. There is no negative impact if the positive and negative pins of the TX lines are swapped, or if the positive and negative pins of the RX lines are swapped.

For the standard Type-C port connection details, refer to Figure 4-1.

FIGURE 4-1: UPSTREAM PORT TYPE-C USB CONNECTIONS

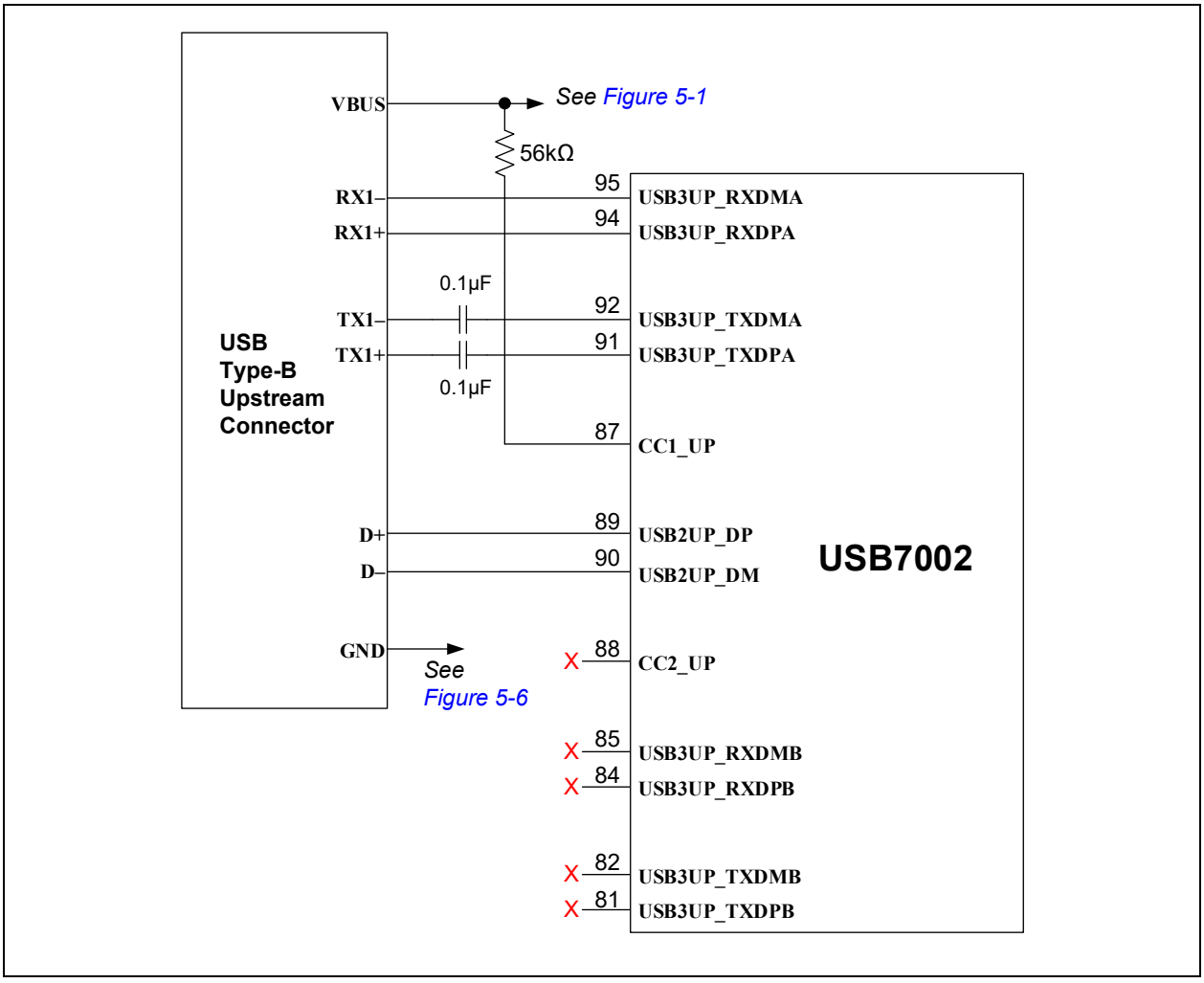


When connecting the upstream port to a legacy Type-B connector, some pin connections change:

- All of the 'Side B' transmitter and receiver pins are floated.
- The **CC1_UP** pin should be connected directly to VBUS through a 56 kΩ pull-up resistor.
- The **CC2_UP** pin should be left floating.

For an example on how to connect the upstream port to a legacy Type-B port, refer to Figure 4-2.

FIGURE 4-2: UPSTREAM PORT TYPE-B USB CONNECTIONS

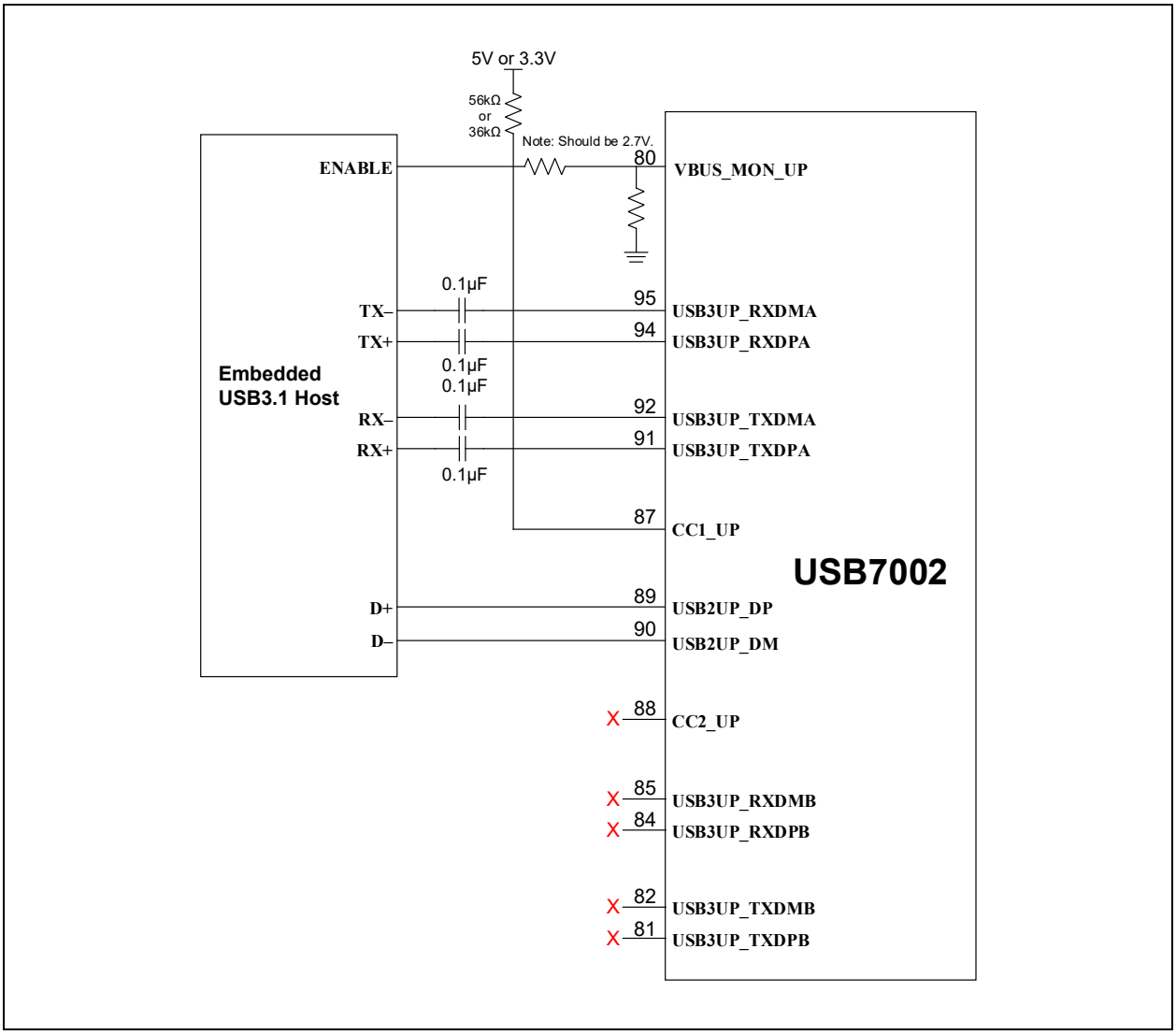


When connecting the upstream port to an embedded USB3.1 host, some pin connections change:

- All of the 'Side B' transmitter and receiver pins should be left floating.
- The **CC1_UP** pin should be connected directly to a 5V power supply through a 56 kΩ pull-up resistor, or a 3.3V power supply through a 36 kΩ pull-up resistor.
- The **CC2_UP** pin should be left floating.
- The **VBUS_MON_UP** pin may be connected to an Enable output from the host processor which is divided down to a nominal 2.7V voltage when enabled. Alternatively, this can be tied directly to a 3.3V power rail through a resistor divider network to create a nominal 2.7V voltage, but a host control is recommended, whether it be through the **VBUS_MON_UP** pin or the **RESET_N** pin.

For an example on how to connect the upstream port to an embedded USB3.1 host, refer to Figure 4-3.

FIGURE 4-3: UPSTREAM PORT EMBEDDED HOST USB CONNECTIONS



4.2 Downstream Ports 1 and 2 USB Signals

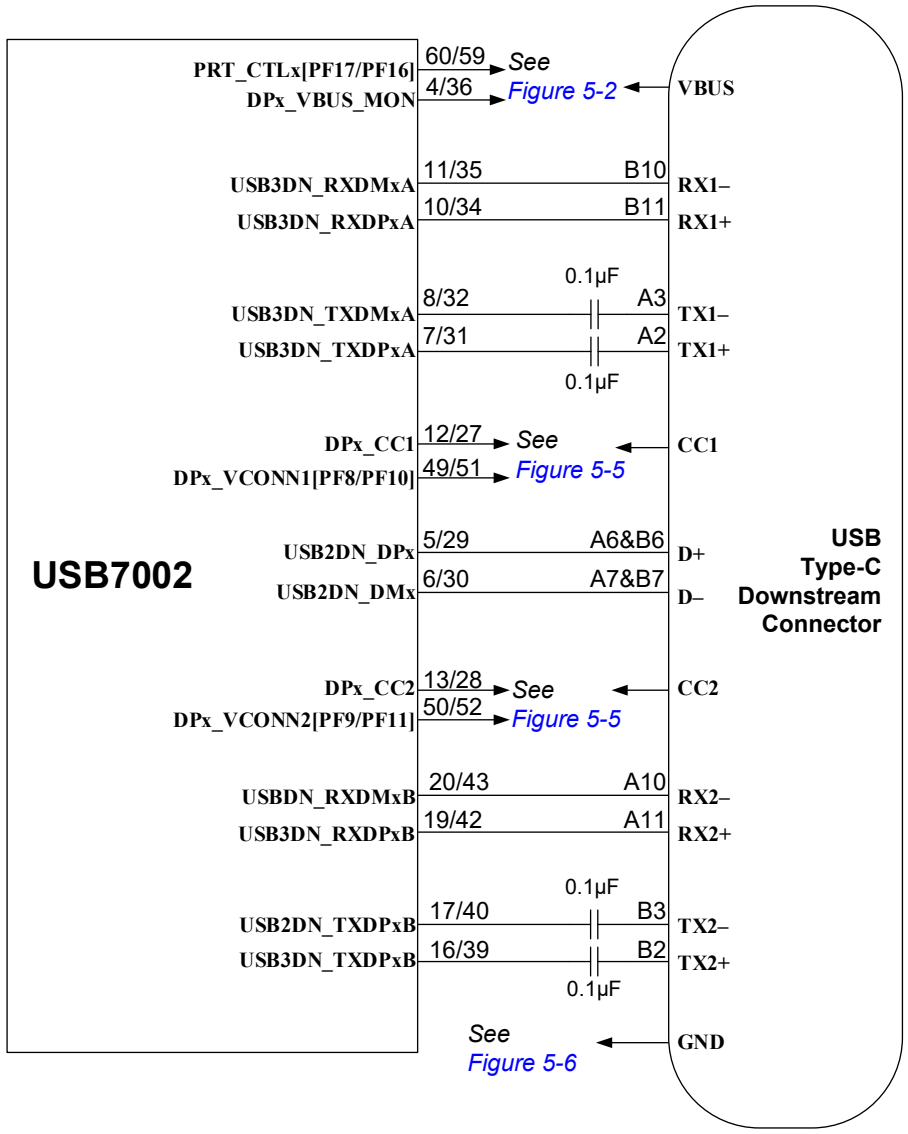
- **USB2DN_DP1/USB2DN_DP2** (pin 5/29): This pin is the positive (+) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP[1] pin of a USB connector.
- **USB2DN_DM1/USB2DN_DM2** (pin 6/30): This pin is the negative (–) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM[1] pin of a USB connector.
- **USB3DN_TXDP1A/USB3DN_TXDP2A** (pin 7/31): This pin is the positive (+) signal of the downstream port USB3.1 'Side A' transmitter (TX) differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX+ (or TX–)[2] pin of the USB connector.
- **USB3DN_TXDM1A/USB3DN_TXDP2A** (pin 8/32): This pin is the negative (–) signal of the downstream port USB3.1 'Side A' TX differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX– (or TX+)[2] pin of the USB connector.
- **USB3DN_RXDP1A/USB3DN_RXDP2A** (pin 10/34): This pin is the positive (+) signal of the downstream port USB3.1 'Side A' receiver (RX) differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the RX+ (or RX–)[2] pin of the USB connector.
- **USB3DN_RXDM1A/USB3DN_RXDM2A** (pin 11/35): This pin is the negative (–) signal of the downstream port USB3.1 'Side A' RX differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the RX– (or RX+)[2] pin of the USB connector.
- **USB3DN_TXDP1B/USB3DN_TXDP2B** (pin 16/39): This pin is the positive (+) signal of the downstream port USB3.1 'Side B' TX differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX+ (or TX–)[2] pin of the USB connector.
- **USB3DN_TXDM1B/USB3DN_TXDM2B** (pin 17/40): This pin is the negative (–) signal of the downstream port USB3.1 'Side B' TX differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX– (or TX+)[2] pin of the USB connector.
- **USB3DN_RXDP1B/USB3DN_RXDP2B** (pin 19/42): This pin is the positive (+) signal of the downstream port USB3.1 'Side B' RX differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the RX+ (or RX–)[2] pin of the USB connector.
- **USB3DN_RXDM1B/USB3DN_RXDN2B** (pin 20/43): This pin is the negative (–) signal of the downstream port USB3.1 'Side B' RX differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the RX– (or RX+)[2] pin of the USB connector.
- **DP1_CC1/DP2_CC1** (pin 12/27): This pin is used to detect a USB Type-C connection and insertion orientation. This should connect directly to the CC1 pin of the USB Type-C connector.
- **DP1_CC2/DP2_CC2** (pin 13/28): This pin is used to detect a USB Type-C connection and insertion orientation. This should connect directly to the CC2 pin of the USB Type-C connector.

Note 1: The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via OTP or SMBus/I^{2}C configuration registers.

2: A standard feature of USB3.1 is automatic polarity detection and correction. There is no negative impact if the positive and negative pins of the TX lines are swapped, or if the positive and negative pins of the RX lines are swapped.

For the standard Type-C port connection details, refer to Figure 4-4.

FIGURE 4-4: DOWNSTREAM PORT 1 AND 2 TYPE-C USB CONNECTIONS

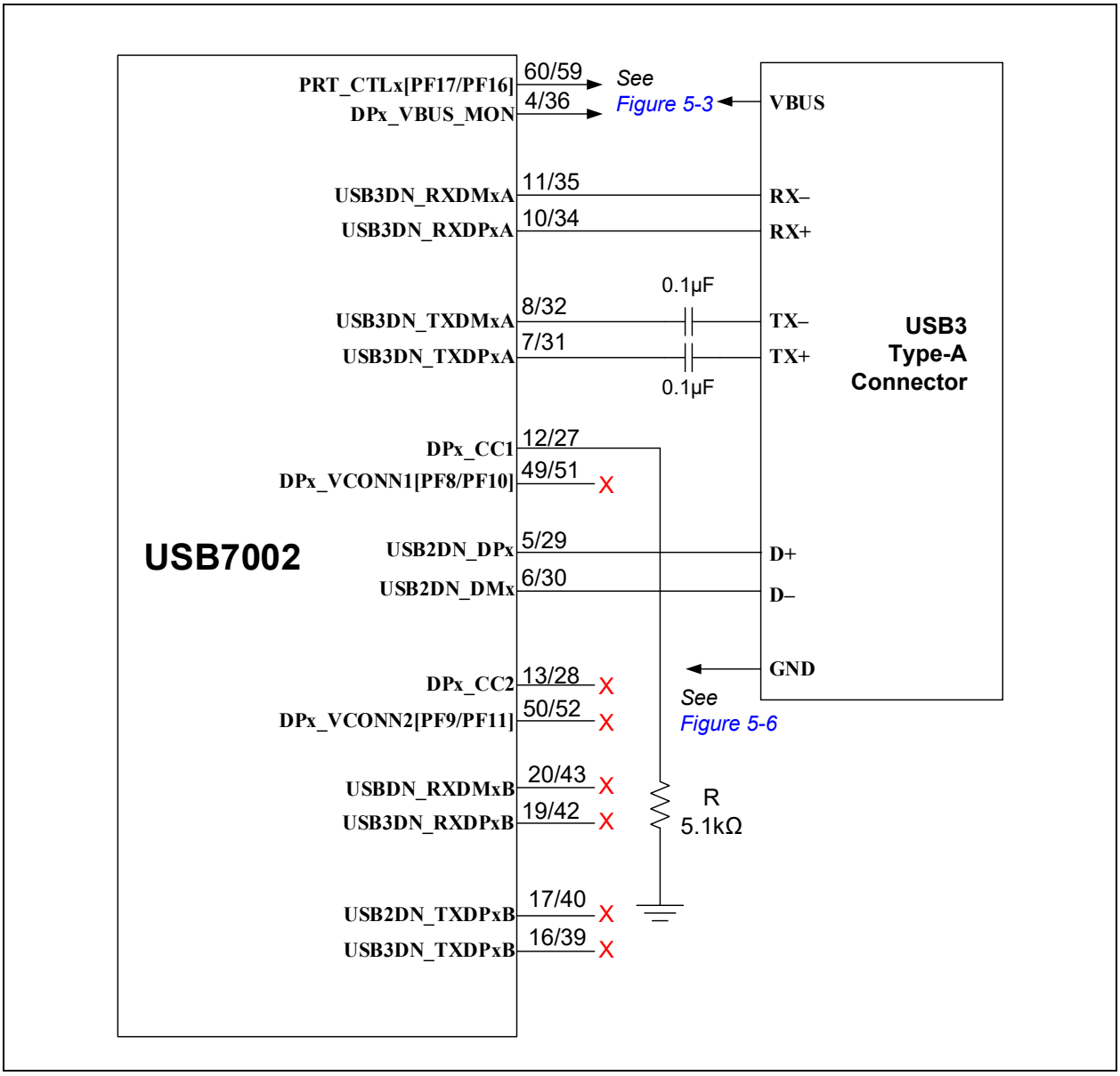


When connecting the upstream port to a legacy Type-B connector, some pin connections change:

- All of the 'Side B' TX and RX pins should be left floating.
- The **DPx_CC1** pin should be connected directly to GND through a 5.1 kΩ pull-up resistor.
- The **DPx_CC2** pin should be left floating.
- **DPx_VCONN1** and **DPx_VCONN2** pins should be left floating.

For an example on how to connect downstream port 1, port 2, or both to a legacy Type-B port, refer to Figure 4-5.

FIGURE 4-5: DOWNSTREAM PORT 1 AND 2 TYPE-A USB CONNECTIONS

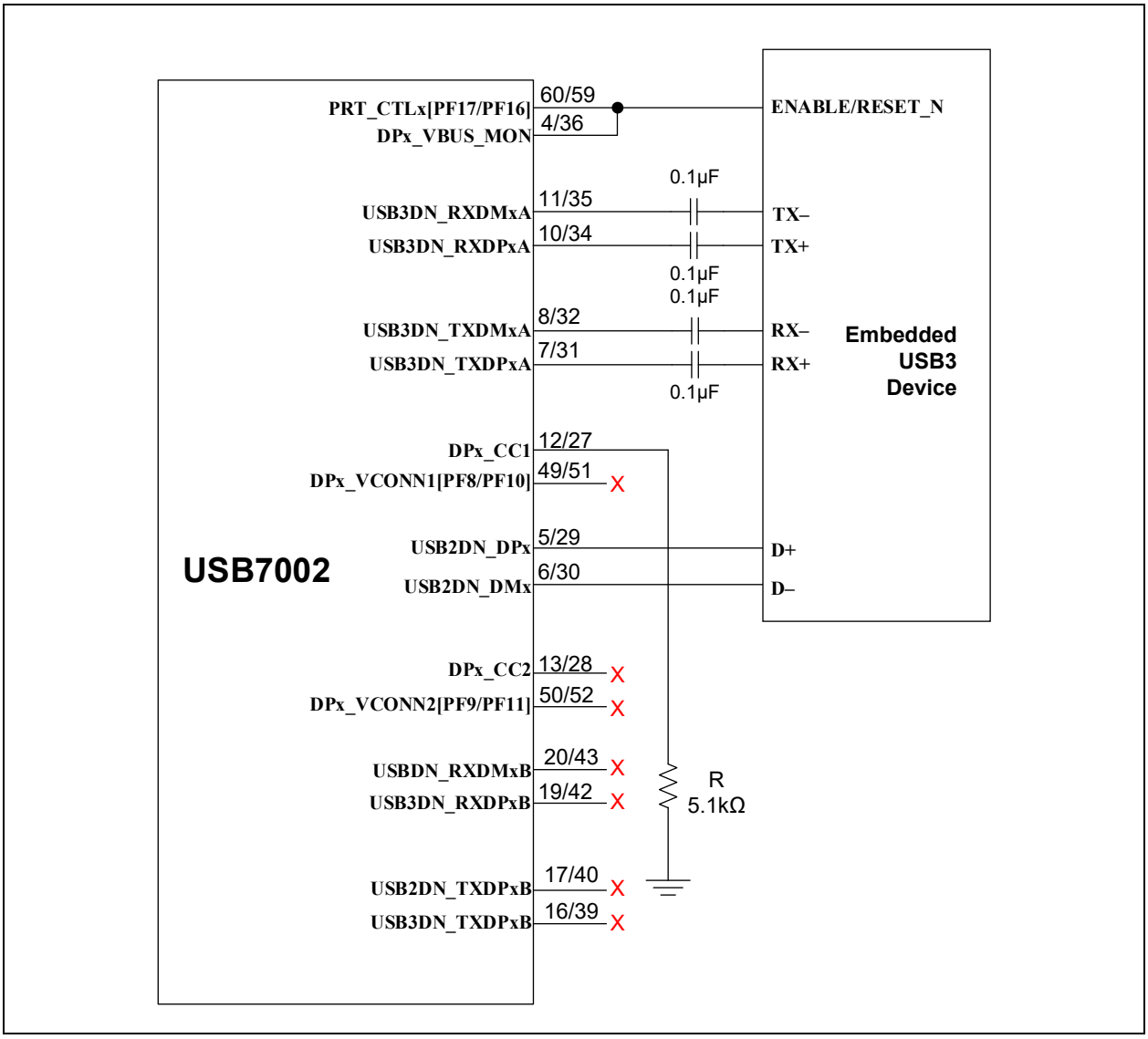


When connecting the upstream port to an embedded USB3.1 device, some pin connections change:

- All of the ‘Side B’ transmitter and receiver pins should be left floating.
- The **DPx_CC1** pin should be connected directly to GND through a 5.1 kΩ pull-up resistor.
- The **DPx_CC2** pin should be left floating.
- **DPx_VCONN1** and **DPx_VCONN2** pins should be left floating.
- **PRT_CTLx** and **DPx_VBUS_MON** can be shorted together and connected directly to the Enable signal of the USB3.1 device, assuming a 3.3V logic level is required by the device. This gives the USB host the ability to reset the device through standard USB protocol.

For an example on how to connect downstream port 1, port 2, or both to an embedded USB3.1 device, refer to Figure 4-6.

FIGURE 4-6: DOWNSTREAM PORT 1 AND 2 EMBEDDED DEVICE USB CONNECTIONS



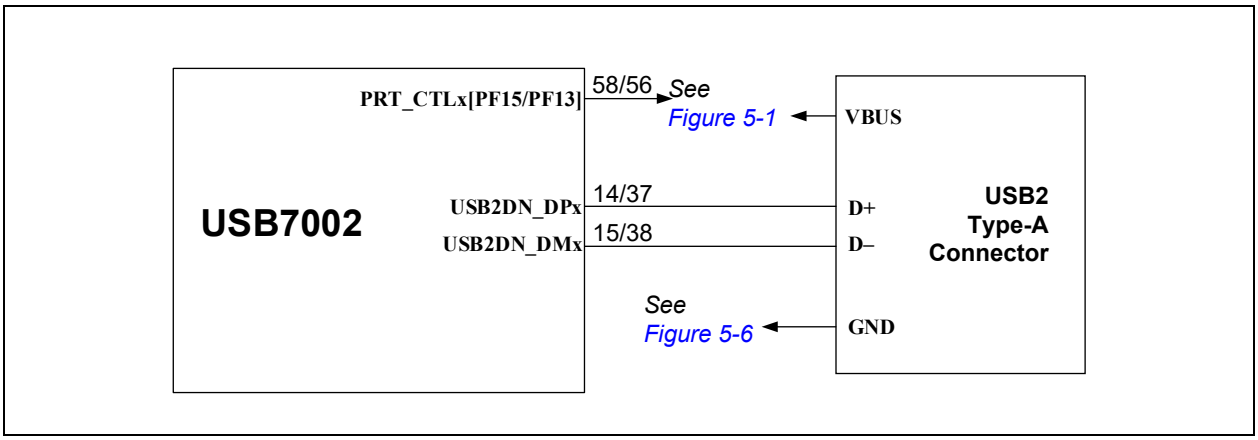
4.3 Downstream Ports 3 and 4 USB Signals

- **USB2DN_DP3/USB2DN_DP4** (pin 14/37): This pin is the positive (+) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP[1] pin of a USB connector.
- **USB2DN_DM3/USB2DN_DM4** (pin 15/38): This pin is the negative (–) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM[1] pin of a USB connector.

Note 1: The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via OTP or SMBus/I^{2}C configuration registers.

For an example on how to connect downstream ports 3 and 4 to USB2.0 connector, refer to Figure 4-7.

FIGURE 4-7: DOWNSTREAM PORT 3 AND 4 TYPE-A USB CONNECTIONS



4.4 Disabling Downstream Ports

Disable downstream ports if unused.

If a downstream port of the USB7002 is unused, it should be disabled. This can be achieved through hub configuration (I^{2}C or OTP), or through a port disable strap option.

If using the port disable strap option, the USB_DP2 and USB_DM2 signals should be pulled high to 3.3V. This connection can be made directly to the 3.3V power net, or through a pull-up resistor. All other signals related to the associated port may be floated.

4.5 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These generally are grouped into three categories:

- TVS protection diodes
  - ESD protection for IEC-61000-4-2 system-level tests
- Application-targeted protection ICs or galvanic isolation devices
  - DC overvoltage protection for short-to-battery protection
- Common-mode chokes
  - For EMI reduction

The USB7002 can be used in conjunction with these types of devices, but these devices may have negative effect on USB signal integrity. Thus, it is important to select components accordingly and follow implementation guidelines from the device manufacturer. The following general guidelines for implementing these devices may also be followed:

- Select only devices that are designed specifically for high-speed applications. Per the USB2.0 Specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry. In a USB3.1 Gen 1 system, ESD protection should add no more than 0.5 pF capacitance to the differential pairs.

- Place these devices as close as possible to the USB connector.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- Always ensure a very low impedance path to a large ground plane. The effectiveness of TVS devices depends heavily on effective grounding.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

4.5.1 ADDITIONAL PROTECTION OPTIONS FOR USB3 PINS

In addition to TVS diodes, some or all of the following may be implemented:

- Use decoupling capacitors on both the TX and RX differential pairs. Decoupling capacitors on the RX pairs are not required for operation, but add some additional ESD immunity at low cost.
- Use decoupling capacitors with high voltage ratings. 0.1 µF capacitors at 0402 sizes are widely available.
- A very small resistor of 0.3-0.5Ω may be placed in series with the decoupling capacitor (placed physically between the TVS diode and the decoupling capacitor) to help steer more of the ESD energy through the TVS diode. A resistor network (2-resistor/4-contact) in 0402 or 0201 size can be placed with very little impact to the differential routing of the signals.

Note: Microchip PHYBoost, VariSense™, and High-Speed Disconnect Threshold adjustment configuration options are available for compensating the negative effects of these devices. These features can help to overcome marginal failures. It is simplest to determine the appropriate setting using lab experiments, such as USB eye diagram tests, on physical hardware.

5.0 USB CONNECTORS

5.1 Upstream Port VBUS and VBUS_DET

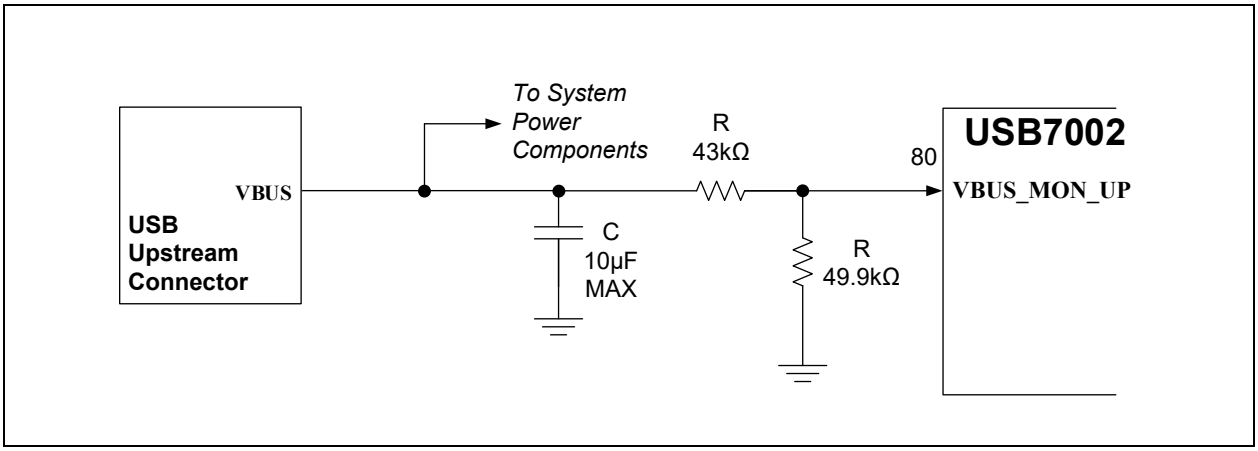
The upstream port VBUS line must have no more than 10 µF of total capacitance connected.

The USB7002 uses the **VBUS_MON_UP** pin to detect the presence of a USB host. The USB host can also toggle the state of VBUS at any time to force a soft reset and reconnection of the USB7002.

It is permissible to tie **VBUS_MON_UP** directly to a 2.7V voltage (3.3V divided down to 2.7V through a resistor divider network). However, this is not recommended as the ability to force a reset of the hub from the USB host VBUS control is lost.

The recommended implementation is shown in Figure 5-1.

FIGURE 5-1: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS



5.2 VBUS and PRT_CTLx Connections of Downstream Ports 1 and 2

The **PRT_CTLx** pin is a hybrid input/output (I/O) pin that has the following states:

- *PORT OFF*: **PRT_CTLx** is an output and drives low. The **PRT_CTLx** pin only transitions to the PORT ON state through a specific command from the USB host.
- *PORT ON*: **PRT_CTLx** is an input with a weak internal pull-up enabled. The input buffer monitors overcurrent events, which are indicated by the port power controller by pulling the **PRT_CTLx** line low. Once an overcurrent event is detected, the **PRT_CTLx** automatically moves to the PORT OFF state until the USB host can be notified of the overcurrent event.

When connecting the **PRT_CTLx** pin to a port power controller, the signal should be connected to both the Enable and the fault indicator pins of the port power controller. Do not place an external pull-up resistor on the line.

Note: The overcurrent detect debounce parameters are configurable and may be adjusted if required to operate properly with the selected port power controller.

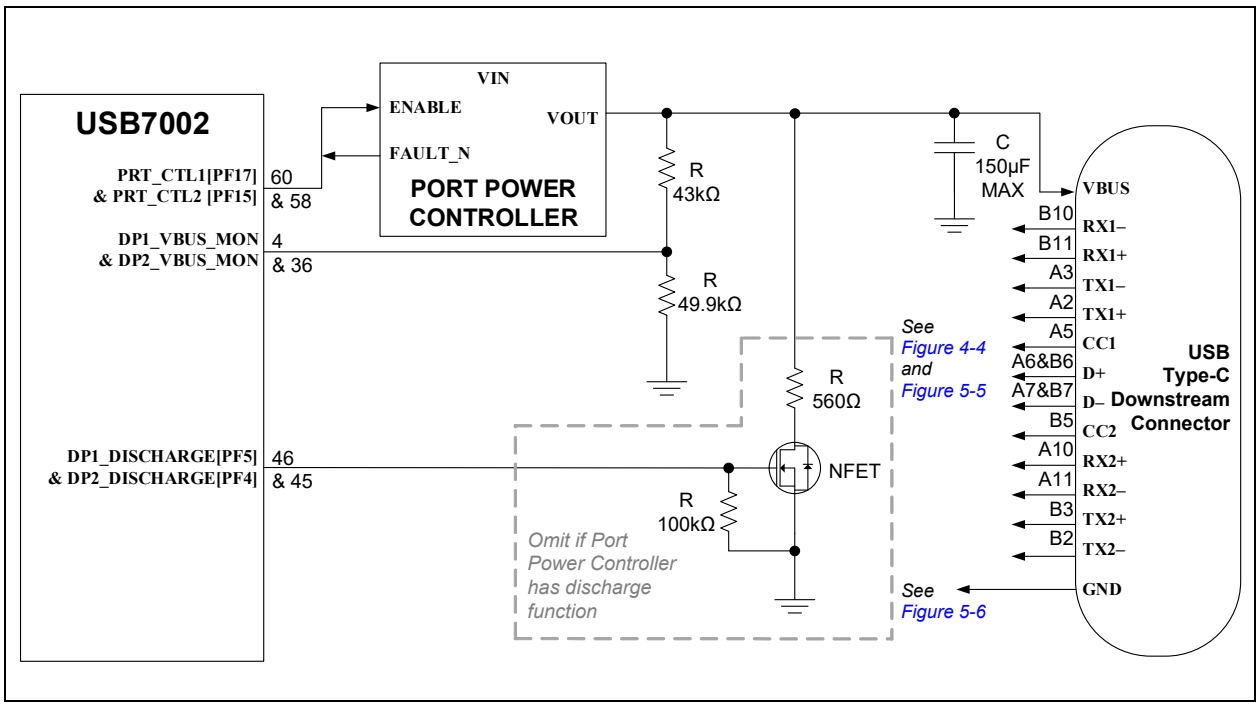
The **DPx_VBUS_MON** pin is an input with a preconfigured set of comparator banks. These comparator banks are used to monitor the voltage on the **VBUS** pin to ensure that the voltage is within the correct range while in the VBUS ON and OFF states (‘vSafe5V’ and ‘vSafe0V’, respectively). The recommended connection to VBUS is through a resistor divider of 43 kΩ over 49.9 kΩ. This pin must be connected per this guidance and may not be left floating or unused.

The **DPx_DISCHARGE** pin is an output that asserts whenever power to VBUS is transitioning from ON to OFF (‘vSafe5V’ to ‘vSafe0V’). This pin can be connected to a transistor that should turn on and short VBUS to GND when this signal asserts to 3.3V. A series resistor in the 400-700Ω range is recommended to limit the current through the transistor and to add discharge slew rate controllability. When discharging the VBUS pin, the voltage must reach the vSafe0V voltage window within the discharge time as defined in the USB Type-C Specification (see the latest revision for the most up-to-date timing and voltage requirements).

Some port power controllers have an automatic discharge function when they are shut off. In that case, the **DPx_DISCHARGE** pin may be left floating.

A typical Type-C implementation is shown in Figure 5-2.

FIGURE 5-2: DOWNSTREAM PORT 1 AND 2 VBUS AND PRT_CTL CONNECTIONS FOR TYPE-C PORT

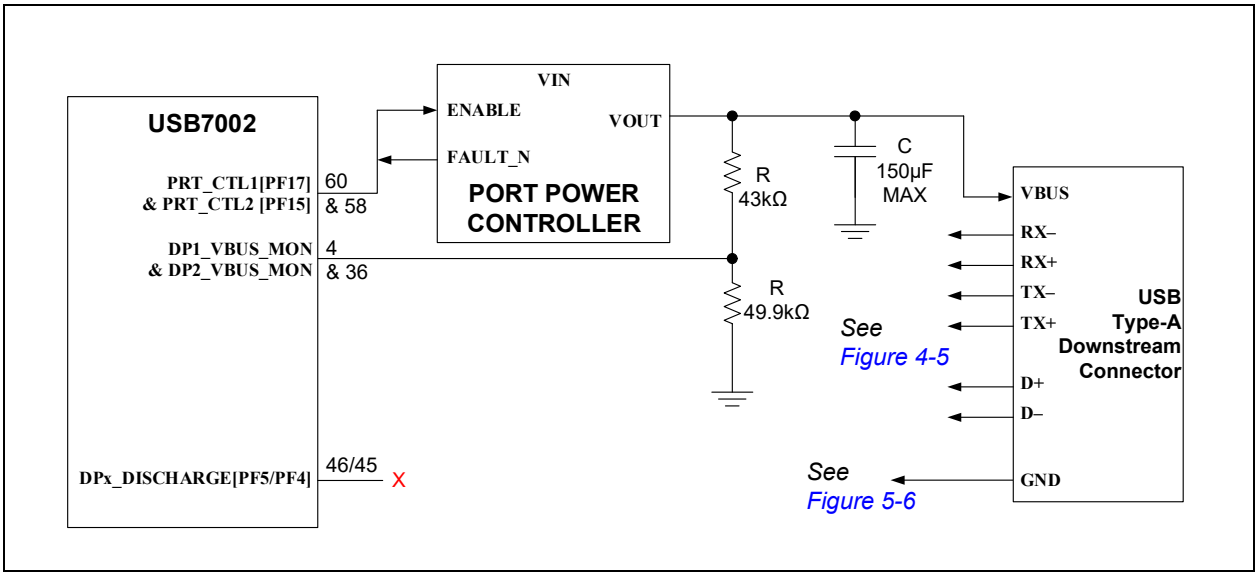


Note: The implementation as shown in Figure 5-2 assumes that the port power controller has an active-high Enable input, and an active-low, open drain style fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

When connecting downstream ports 1 and 2 to a standard Type-A port, the **DPx_VBUS_MON** pin must still be connected in the same manner, but **DPx_DISCHARGE** may be left disconnected, as a standard Type-A port is an 'always on' port that does not require fast discharging.

A typical Type-A implementation is shown in Figure 5-3.

FIGURE 5-3: DOWNSTREAM PORT 1 AND 2 VBUS AND PRT_CTLX CONNECTIONS FOR TYPE-A PORT



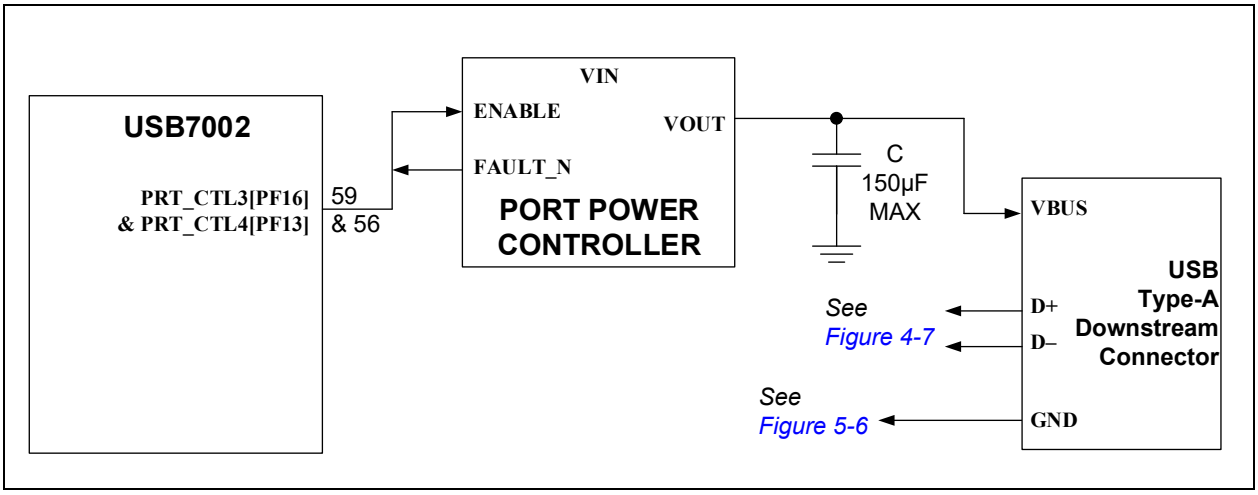
Note: The implementation as shown in Figure 5-2 assumes that the port power controller has an active-high Enable input, and an active-low, open drain style fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

5.3 VBUS and PRT_CTLx Connections of Downstream Ports 3 and 4

Downstream ports 3 and 4 are basic USB2.0-only ports, and they do not include **DPx_VBUS_MON** and **DPx_DISCHARGE** pins.

A typical downstream port 3 and 4 Type-A implementation is shown in Figure 5-4.

FIGURE 5-4: DOWNSTREAM PORT 3 AND 4 VBUS AND PRT_CTLX CONNECTIONS



Note: The implementation as shown in Figure 5-4 assumes that the port power controller has an active-high Enable input, and an active-low, open drain style fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

5.4 CC1 and CC2 Connections of Downstream Ports 1 and 2

If connecting downstream port 1, downstream port 2, or both to a Type-A port, see Figure 4-5.

If connecting downstream port 1, downstream port 2, or both to an embedded USB device, see Figure 4-6.

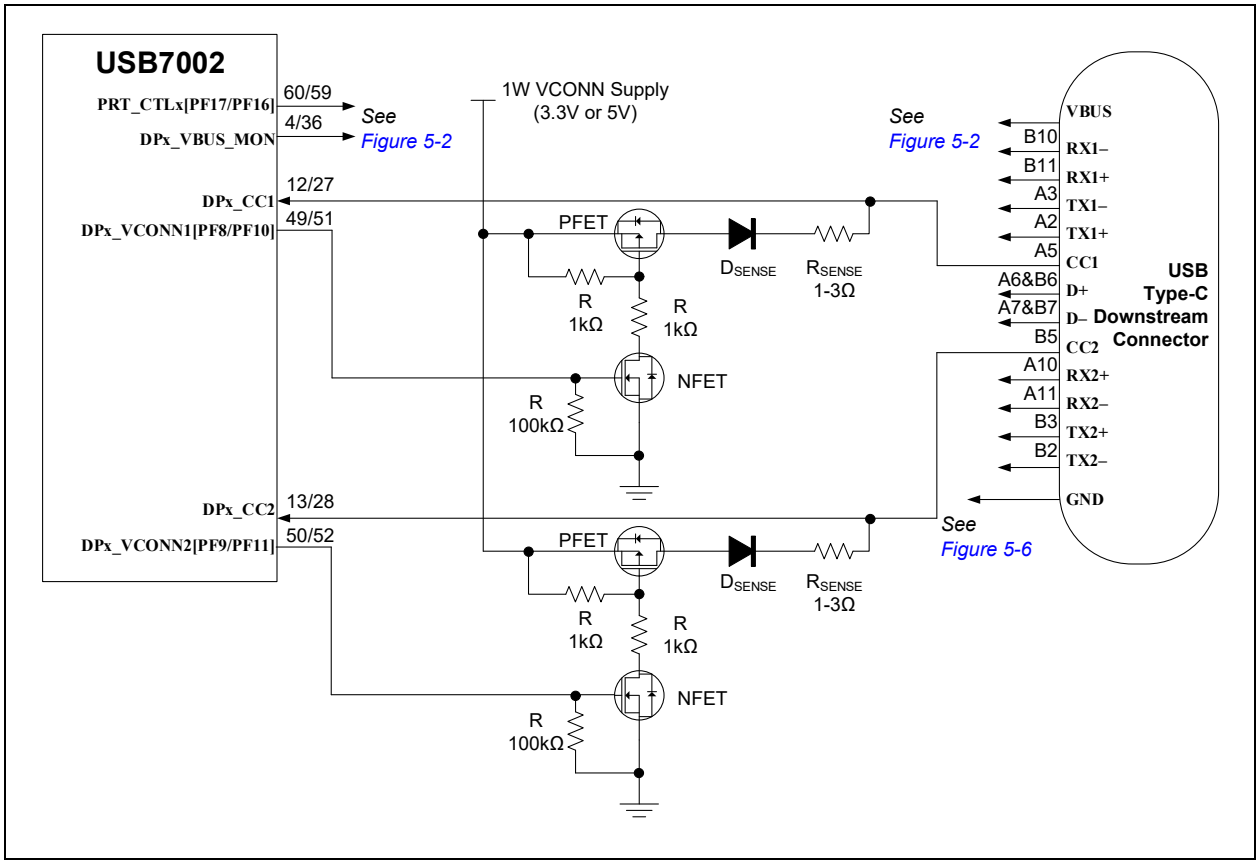
DPx_CC1 and **DPx_CC2** of downstream ports 1 and 2 of USB7002 are designed to connect directly to the respective CC1 and CC2 pins of the Type-C connector.

DPx_VCONN1 and **DPx_VCONN2** of downstream ports 1 and 2 of USB7002 are active high control signals that assert when the VCONN should be supplied to an active or electronically marked cable or to a VCONN powered accessory. The VCONN supply for a standard Type-C application must be capable of supplying 1W of VCONN power to each Type-C downstream port. For the VCONN power supply, 5V is recommended though lower voltages are also supported. The recommended arrangement is an NFET to invert the polarity of the control signal, and a PFET pass transistor for the VCONN voltage.

VCONN overcurrent is sensed by voltage drop on the **CCx** pin. A diode and a low impedance series resistor may be necessary to ensure this voltage drop is achieved when VCONN current draw exceeds the desired overcurrent threshold. The diode and resistor characteristics should be tuned by the system designer to match the exact desired overcurrent setting.

A typical implementation is shown in Figure 5-5.

FIGURE 5-5: DOWNSTREAM PORTS 1 AND 2 CC1 AND CC2 CONNECTIONS



Note: The implementation as shown in Figure 5-5 assumes that the Type-C controller has an active-high Enable input, and the port power controller have an active-low, open drain style fault indicator. External polarity inversion through buffers or FETs may be required if the Type-C controller, port power controller, or both have different I/O characteristics.

5.5 GND and EARTH Recommendations

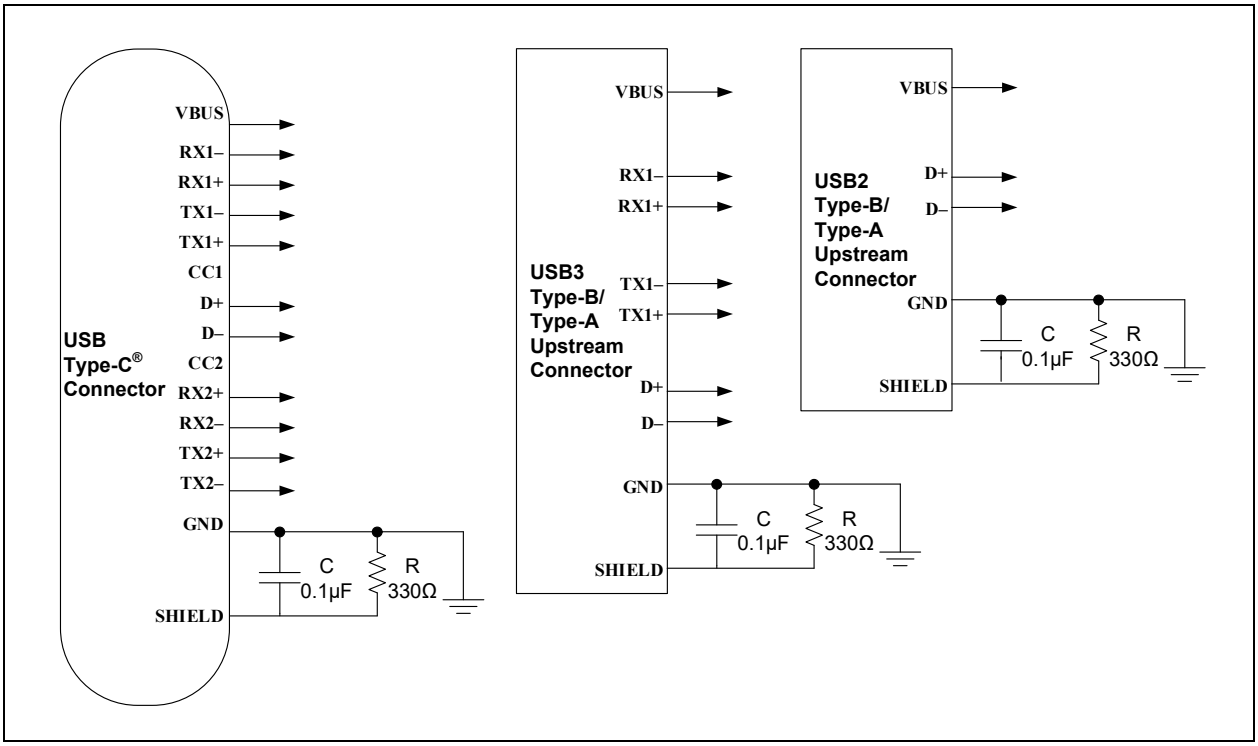
The **GND** pins of the USB connector must be connected to the PCB with a low impedance path directly to a large GND plane.

The **EARTH** pins of the USB connector may be connected in one of two ways:

- (*Recommended*) Connect to GND through a resistor and a capacitor in parallel. A resistor-capacitor (RC) filter can help to decouple and minimize EMI between a PCB and a USB cable.
- Connect directly to the GND plane.

The recommended implementation is shown in Figure 5-6.

FIGURE 5-6: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS



6.0 CLOCK CIRCUIT

6.1 Crystal and External Clock Connection

A 25.000 MHz (±50 ppm) reference clock is the source for the USB interface and for all other functions of the device. For exact specifications and tolerances, refer to the latest revision of the *USB7002 Data Sheet*.

- **XTALI** (pin 98) is the clock circuit input for the USB7002. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XTALO** (pin 97) is the clock circuit output for the USB7002. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- The crystal loading capacitor values are system-dependent, which are based on the total C_L spec of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly used formula for calculating the appropriate physical C_1 and C_2 capacitor values is:

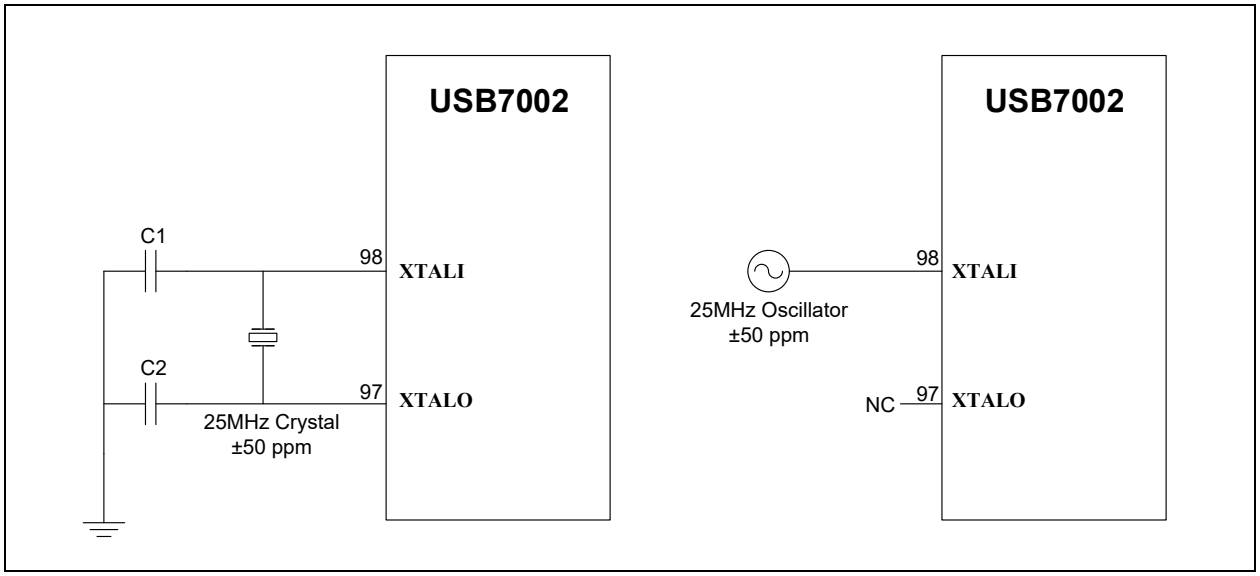
  $C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$

Where, C_L is the spec from the crystal data sheet, $C_{X1} = C_{stray} + C_1$, $C_{X2} = C_{stray} + C_2$.

Note: C_{stray} is the stray or parasitic capacitance due to PCB layout. It can be assumed to be very small, in the 1-2 pF range, and then verified by physical experiments in the lab if PCB simulation tools are not available.

- Alternatively, a 25.000 MHz, 3.3V clock oscillator may be used to provide the clock source for the USB7002. When using a single-ended clock source, **XTALO** (pin 97) should be left floating as a No Connect (NC).

FIGURE 6-1: CRYSTAL AND OSCILLATOR CONNECTIONS



7.0 POWER AND STARTUP

7.1 RBIAS Resistor

The **RBIAS** pin on the USB7002 must connect to ground through a 12 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the internal circuitry. This should be placed as close as possible to the IC pin, and be given a dedicated, low-impedance path to a ground plane.

7.2 Board Power Supplies

7.2.1 POWER RISE TIME

The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *USB7002 Data Sheet*.

If a monotonic or fast power rail rise cannot be assured, then the RESET_N signal should be controlled by a reset supervisor and only released when the power rail has reached a stable level.

7.2.2 CURRENT CAPABILITY

It is important to size the 5V and 3.3V power rails appropriately. The 5V power supply must be capable of supplying 500 mA (if BC1.2 is not enabled), 1.5A (if BC1.2 is enabled), or up to 3.0A (if the maximum Type-C current is enabled) to the USB downstream port VBUS without dropping below the minimum voltage permissible in the USB Specification.

The 3.3V and 1.2V power supply must be able to supply enough power to the USB hub IC. It is recommended that the 3.3V and 1.2V power rails be sized such that they are able to supply maximum power consumption specification as displayed in the *USB7002 Data Sheet.*

7.3 Reset Circuit

RESET_N (pin 28) is an active-low reset input. This signal resets all logic and registers within the USB7002. A hardware reset (RESET_N assertion) is not required following power-up. Refer to the latest copy of the *USB7002 Data Sheet* for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the USB7002 when reset is triggered by the power supply.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

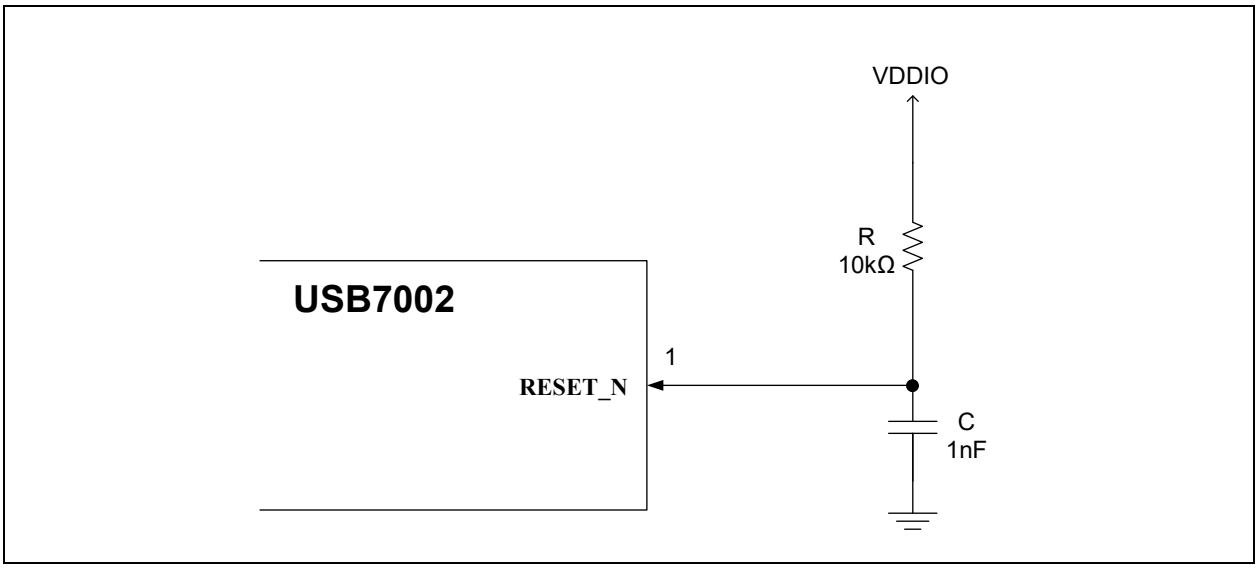
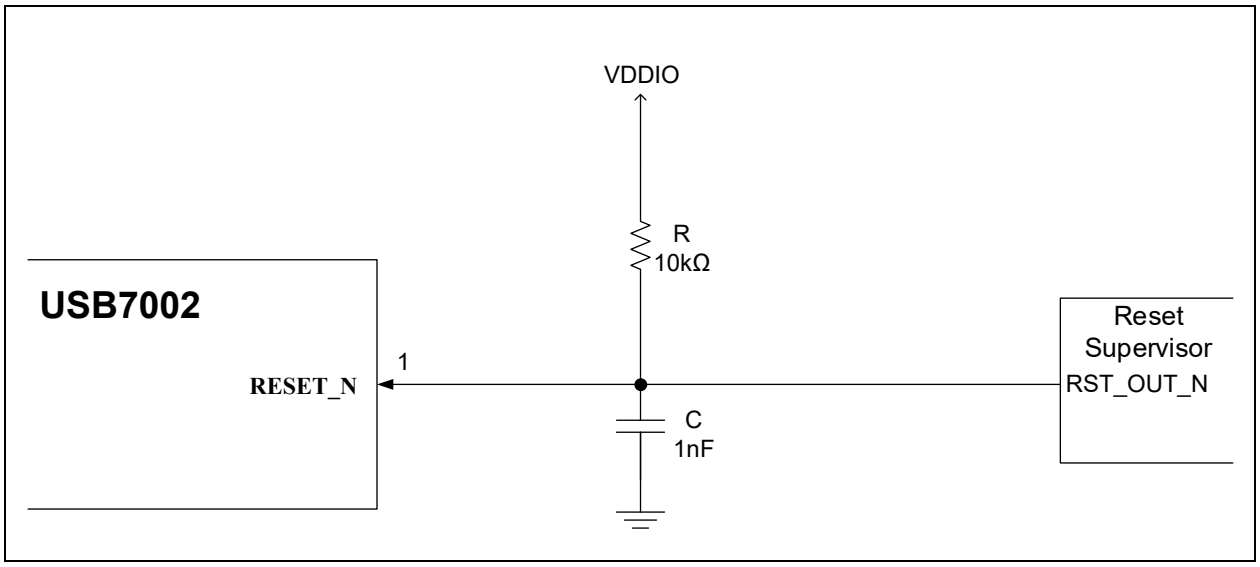


Figure 7-2 details the recommended reset circuit for applications where reset is driven by an external CPU/MCU. The reset out pin (RST_OUT_N) from the CPU/MCU provides the warm reset after power-up.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT



8.0 EXTERNAL SPI MEMORY

8.1 SPI Operation Summary

By default, the USB7002 executes firmware from an internal read only memory (ROM). The USB7002 supports optional firmware execution from an external SPI Flash device. An SPI Flash is only required if a custom firmware is required for the application.

The SPI interface can operate at 60 MHz or 30 MHz, and can operate in Dual mode or Quad mode.

The firmware image can be executed in one of two ways:

- *Execute in place*: The firmware is continuously executed directly from the SPI Flash, and the interface is constantly active.
- *Execute in internal SRAM*: The firmware is loaded into the hub's internal SRAM and executed internally. This may only be supported if the firmware image is smaller than the hub's SRAM size.

Note: All firmware images are developed, compiled, tested, and provided by Microchip. The SPI interface speed is an OTP-configurable option and only speeds that were specifically tested with the firmware image should be selected. The execution method is configured with the firmware image itself and cannot be changed via configuration.

8.2 Compatible SPI Flash Devices

Microchip recommends SST-brand SPI Flash devices. Microchip has verified compatibility of the following list of SPI Flash devices:

- SST26VF016B
- SST26VF032B
- SST26VF064B
- SST25VF064C
- AT25SF041
- AT26DF081

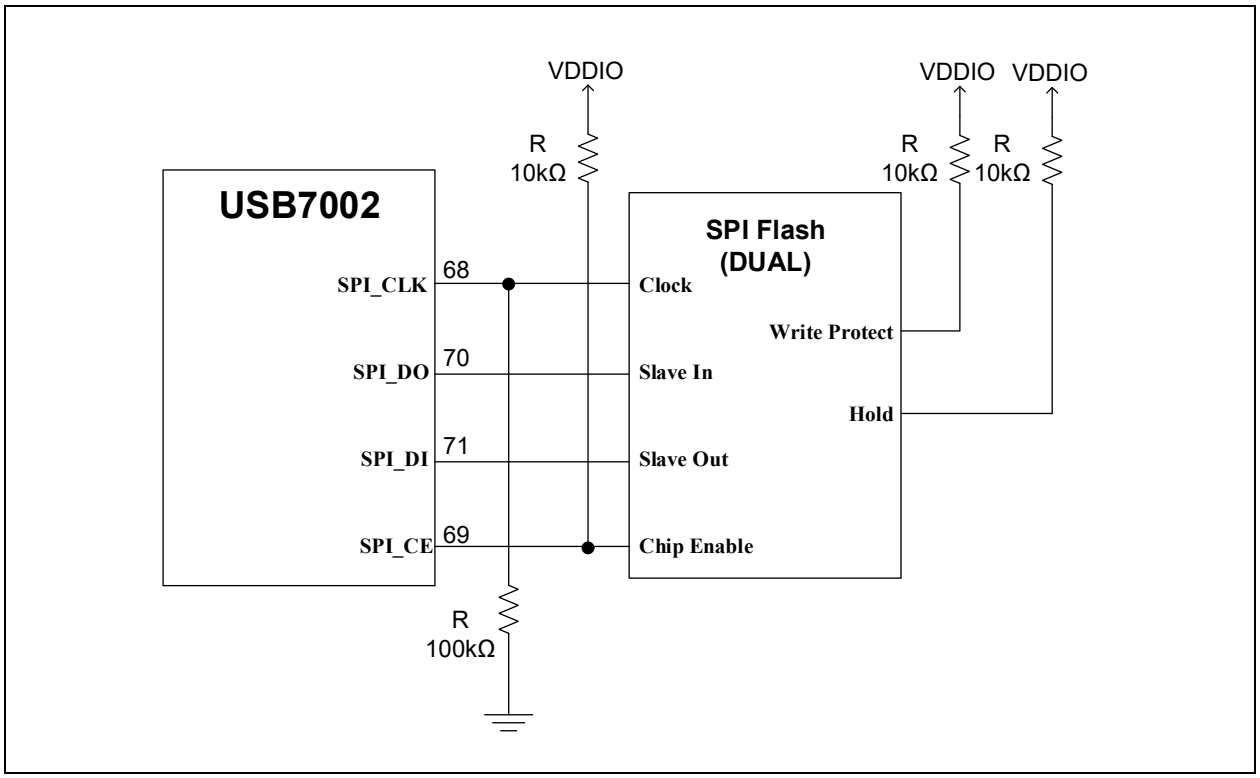
Other SPI Flash devices may be used, provided that they meet the following minimum requirements:

- Operation at 30 MHz or 60 MHz
- Mode 0 or mode 3
- Memory of 256 kB or larger
- Utilization of the same OpCode commands as with the above list of compatible devices
- Dual mode or Quad mode operation

8.3 SPI Connection Diagrams

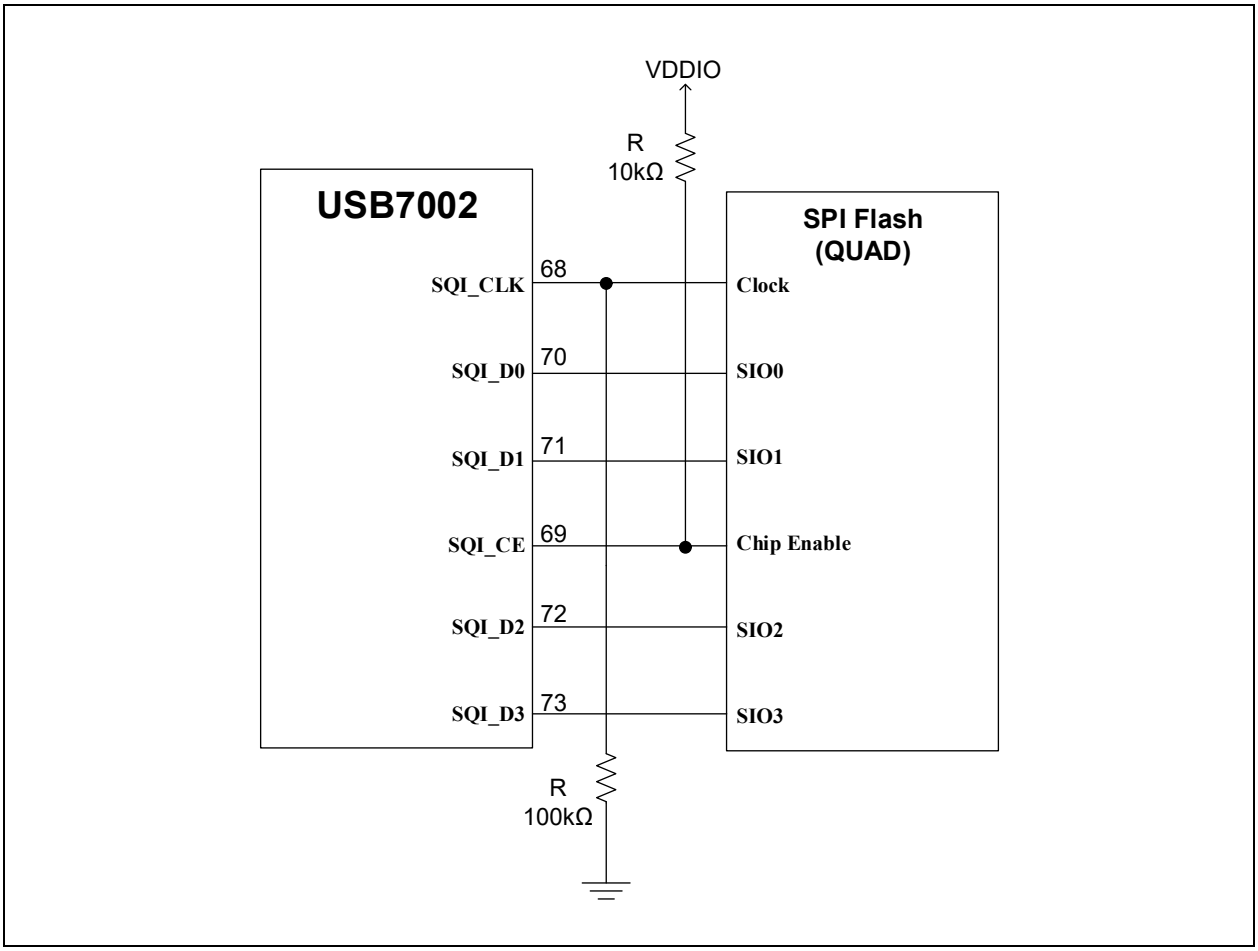
If a Dual SPI Flash device is used, the recommended schematic connections are shown in Figure 8-1.

FIGURE 8-1: DUAL SPI FLASH CONNECTIONS



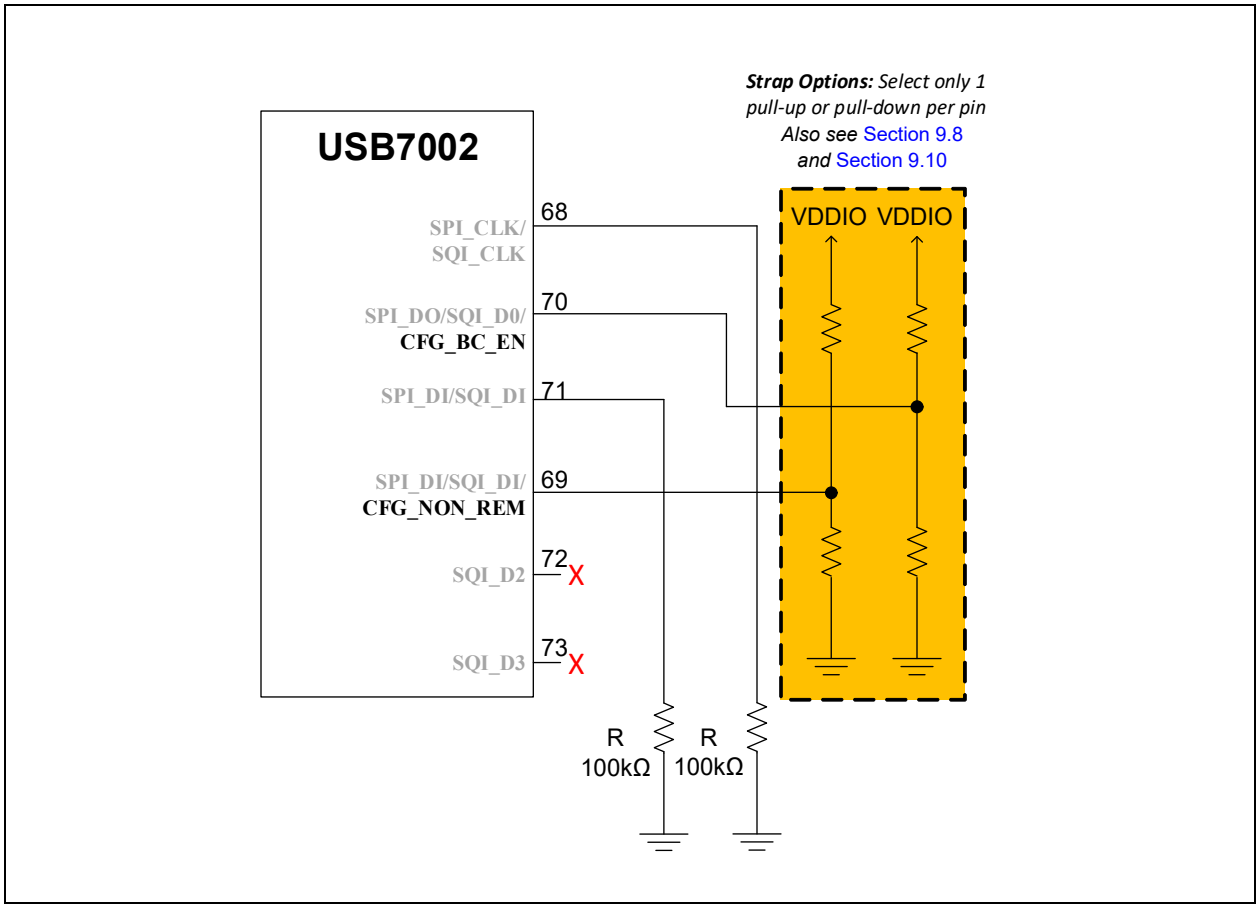
If a Quad SPI Flash device is used, the recommended schematic connections are shown in Figure 8-2.

FIGURE 8-2: QUAD SPI FLASH CONNECTIONS



If an SPI Flash device is not used, the recommended schematic connections are shown in Figure 8-3. Some of the SPI pins become configuration straps when an SPI Flash is not connected. A configuration strap option must be selected, and the pins cannot be floated.

FIGURE 8-3: RECOMMENDED CONNECTIONS IF SPI FLASH IS NOT USED



9.0 MISCELLANEOUS

9.1 Test Pins

USB7002 includes five test pins that are not intended for use within an end system. These pins should be handled as follows:

- **TESTEN** (pin 24): This pin should be pulled to GND either directly or through a resistor.
- **TEST1/TEST2/TEST3** (pins 63/64/65): **TEST1** should be pulled up to 3.3V through a resistor. **TEST2** and **TEST3** may alternatively be pulled up to 3.3V or pulled down to ground through a resistor.
- **ATEST** (pin 96): This pin should be tied to GND either directly or through a resistor. This pin may alternatively be left floating.

9.2 GPIOs

The four GPIO pins included on USB7002 may be controlled from the USB host or from an embedded SoC/MCU. These GPIOs can be used without any additional configuration. By default, all of the GPIOs are configured as inputs. If a default output power-on state is required, the default pin output state can be configured in the hub's OTP memory or through the I^2C/SMBus slave interface during the configuration stage (SOC_CFG). These pins are described in Table 9-1.

TABLE 9-1: AVAILABLE GPIOS

Pin	PF Pin	Name	Configuration Requirements
47	PF6	GPIO70	Configuration 1, 2, and 4
48	PF7	GPIO71	Configuration 1 and 4
54	PF12	GPIO76	All Configurations
57	PF14	GPIO78	Configuration 1 and 4
77	PF28	GPIO92	All Configurations
74	PF29	GPIO93	All Configurations
2	PF30	GPIO94	Configuration 1, 3, and 4
3	PF31	GPIO95	Configuration 1, 3, and 4

Instructions for operating these pins, including register definitions, are described in full in *AN2750 - USB-to-GPIO Bridging with Microchip USB70xx Hubs*.

Ensure that the voltages applied to these pins are within the electrical specifications for the pins, and that any external loading is within the drive strength capabilities as described in the *USB7002 Data Sheet*.

Note: Additional GPIOs may be made available for use under certain conditions or with custom firmware development. Please consult your Microchip support representative or submit a request to the Microchip online support system to discuss options.

9.3 I^2C/SMBus Connections

There are two I^2C/SMBus interfaces available on USB7002. These are described in Table 9-2.

TABLE 9-2: I^2C/SMBUS PINS

Pin	PF Pin	Name	Role	Configuration Requirements
61	PF18	MSTR_I2C_CLK	USB to I^2C master clock	Configuration 1
66	PF19	MSTR_I2C_DATA	USB to I^2C master data	Configuration 1
75	PF26	SLV_I2C_CLK	I^2C slave data	Configuration 1
76	PF27	SLV_I2C_DATA	I^2C slave clock	Configuration 1
2	PF30	MSTR_I2C_CLK	USB to I^2C master clock	Configuration 2
3	PF31	MSTR_I2C_DATA	USB to I^2C master data	Configuration 2

9.3.1 SLAVE INTERFACE

The USB7002 may be configured by an embedded SoC/MCU during both the start-up and runtime stages. Pull-up resistors must be detected by the hub at start-up in order for the I²C/SMBus interface to become active. The interface command specification and configuration register set is described in full in *AN2810 - Configuration of USB7002/USB705x*.

Typically, a pull-up resistor value of 1-10 kΩ is sufficient, depending on the interface speed and total capacitance on the I²C tree.

A pull-up voltage of 1.8V-3.3V is supported.

Note: If I²C/SMBus pull-up resistors are detected by the USB7002 at start-up, the hub waits indefinitely to be configured by the attached I²C/SMBus master. For early prototyping, it may be necessary to physically remove the pull-up resistors until the I²C/SMBus master is fully operational and can properly configure the hub at start-up.

9.3.2 MASTER INTERFACE

The USB7002 has an I²C/SMBus master interface that can bridge USB commands to I²C/SMBus. Instructions for operating the I²C/SMBus master interface are contained in *AN2754 - USB-to-I2C Bridging with USB7002, USB7050, USB7051, and USB7052 Hubs*.

Typically, a pull-up resistor of 1-10 kΩ is sufficient, depending on the configured interface speed and total capacitance on I²C tree.

A pull-up voltage of 1.8-3.3V is supported.

Ensure that all I²C/SMBus slave devices connected to the bus have unique addresses assigned.

Ensure that the USB7002 and all I²C/SMBus slave devices connected to the bus can support the target bus speed.

9.4 I²S™ Connections

There is one USB-to-I²S interface available on USB7002. The interface is enabled when Configuration 2 is selected through the **CFG_STRAP** pin.

A compatible I²S codec is required. By default, the I²S interface is configured to be connected to an ADAU1961.

Refer to Table 9-3 to ensure that the selected codec is compatible with the options available on USB7002.

TABLE 9-3: I²S™ CODEC COMPATIBILITY GUIDE

Parameter	Supported Values
Sampling Frequency (fs)	8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz
MCLK Frequency	1*fs to 1024*fs Since LRCLK is derived from MCLK source, the MCLK signal should be an even integer multiple of fs.
Audio Sample Size	16-bit, 24-bit, 32-bit
I²S Audio Format	I²S mode, Left Justified mode, Right Justified mode
I²C Master Control Interface Frequency	100 kHz or 400 kHz
Audio Channels	Mono or Stereo
Interface Enable/Disable Options	Three options: • Audio OUT and Audio IN mode • Audio OUT Only mode (Speaker Interface) • Audio IN Only mode (Mic Interface)
Audio Jack Insertion Detection	Two options: • Audio Jack Insertion Detection Enabled (through HID interface) • Audio Jack Insertion Detection Disabled

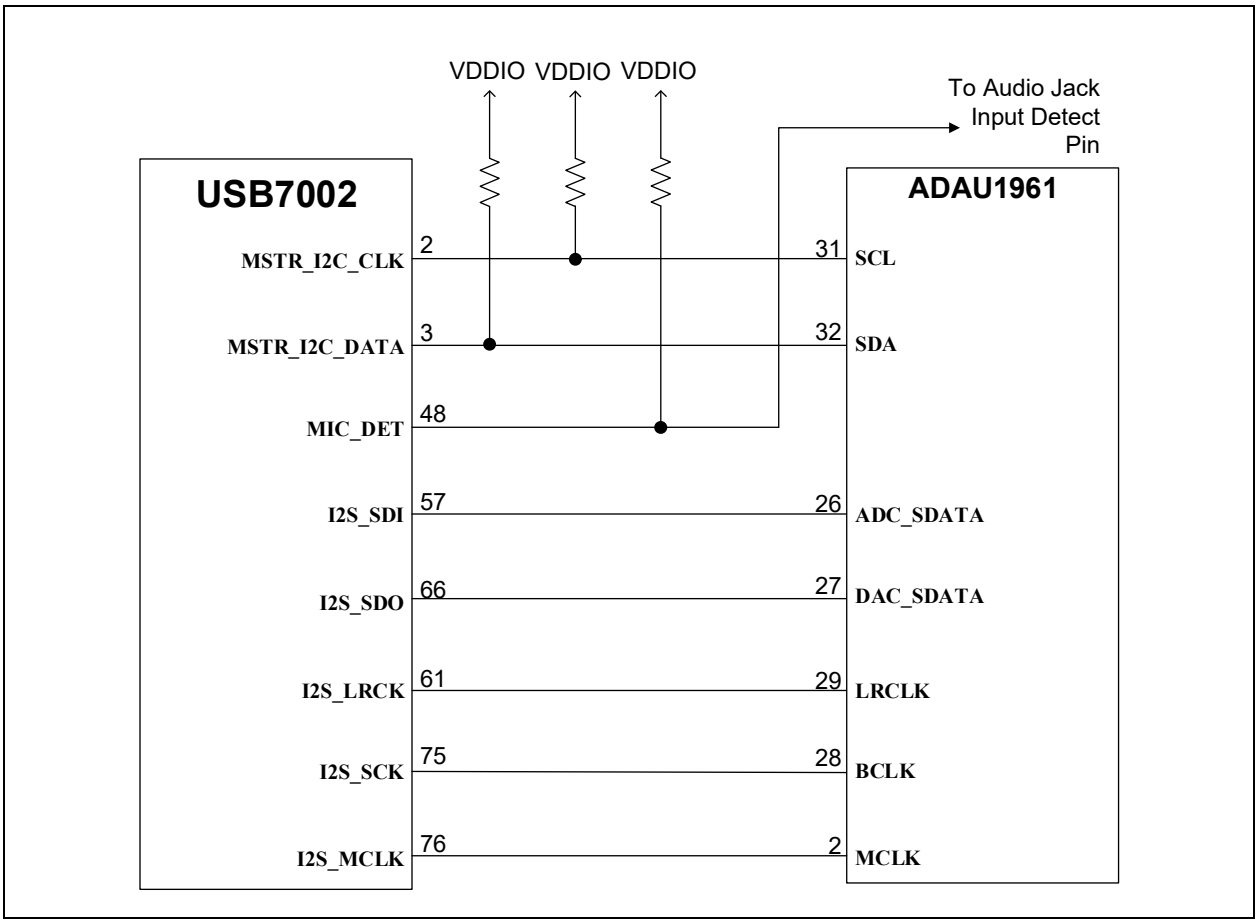
The I²S pins are described in Table 9-4.

TABLE 9-4: I²S™ PINS

Pin	PF Pin	Name	Role	Configuration Requirements
48	PF7	MIC_DET	Optional - Microphone Detection Pin	Configuration 2
57	PF14	I2S_SDI	I²S Serial Data In	Configuration 2
61	PF18	I2S_LRCK	I²S Left Right Clock	Configuration 2
66	PF19	I2S_SDO	I²S Serial Data Out	Configuration 2
75	PF26	I2S_SCK	I²S Continuous Serial Clock	Configuration 2
76	PF27	I2S_MCLK	I²S Master Clock	Configuration 2

If connecting to an ADAU1961, the I²S signals should be connected as shown in Figure 9-1. If using a different codec, consult the design guidelines provided by the manufacturer of the selected codec for implementation guidelines.

FIGURE 9-1: ADAU1961 I²S™ CODEC CONNECTIONS



9.5 UART Connections

There is one USB-to-UART interface available on USB7002.

The interface is enabled when Configuration 2 is selected through the **CFG_STRAP** pin. The pins are described in Table 9-5.

These signals may be attached directly to an embedded UART device, or connected to an RS232 connector. If routing the UART signals to an RS232 connector, a UART transceiver is recommended.

TABLE 9-5: UART PINS

Pin	PF Pin	Name	Role	Configuration Requirements
47	PF6	UART_RX	UART Receiver	Configuration 3
48	PF7	UART_TX	UART Transmitter	Configuration 3
57	PF14	UART_nCTS	Optional UART	Configuration 3
61	PF18	UART_nDCD	Optional UART	Configuration 3
66	PF19	UART_nRTS	Optional UART	Configuration 3
75	PF26	UART_nDSR	Optional UART	Configuration 3
76	PF27	UART_nDTR	Optional UART	Configuration 3

9.6 Multi-Host Endpoint Reflector

The Multi-Host Endpoint Reflector requires no additional schematic or PCB-level circuitry to operate.

9.7 FlexConnect

The FlexConnect feature allows the USB2 host role, USB3 host role, or both host roles to be reassigned to any of the downstream ports in the hub. This feature is highly implementation-specific and usually has numerous hardware design ramifications. If the FlexConnect feature is required in any specific application, it is recommended to reach out to a Microchip support representative early on in the design cycle to discuss the option available.

9.8 Non-Removable Port Settings

In a typical USB7002 application, downstream port 1 is routed to a user-accessible USB connector. Thus, the downstream port should be configured as a removable port.

The USB7002 has a configuration strap option, **CFG_NON_REM**, which can be used to set the default configuration for port 1. This is located on pin 69. The strap setting is sampled one time at start-up. A configuration strap option must be selected unless the hub firmware is being executed from an external SPI Flash device. These are described in Table 9-6.

TABLE 9-6: CFG_NON_REM

Setting	Effect
200 kΩ pull-down to GND	All ports are removable. (Recommended for most USB7002 applications)
200 kΩ pull-up to 3.3V	Port 1 is non-removable; only a valid selection if port 1 is connected directly to an embedded USB device.
10 kΩ pull-down to GND	Ports 1 and 2 are non-removable; only a valid selection if ports 1 and 2 are connected directly to embedded USB devices.
10 kΩ pull-up to 3.3V	Ports 1, 2, and 3 are non-removable; only a valid selection if ports 1, 2, and 3 are connected directly to embedded USB devices.
10Ω pull-down to GND	Ports 1, 2, 3, and 4 are non-removable; only a valid selection if ports 1, 2, 3, and 4 are connected directly to embedded USB devices.

The following guidelines can be used to determine which setting to use:

- If the port is routed to a user-accessible USB connector, it is *removable*.
- If the port is routed to a permanently attached and embedded USB device on the same PCB, or non user-accessible wiring or cable harness, it is *non-removable*.

Note: The removable or non-removable device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors, which the USB host may use to understand if a port is a user-accessible port or if the device is a permanently attached device. Under standard operating conditions, the USB host may or may not modify its operation based upon this information. Certain USB compliance tests are impacted by this setting, so designs that must undergo USB compliance testing and certification must ensure the configuration settings are correct.

9.9 Self-Powered/Bus-Powered Settings

In a typical USB7002 application, the hub should be configured as Self-Powered, which is the default configuration setting.

The following guidelines can be used to determine which setting to use:

- If the entire system (hub included) is powered completely from the upstream USB connector's VBUS pin and the system is designed to operate using standard USB cabling and any standard USB host, then the hub system is *bus-powered*.
- If the entire system (hub included) is always powered by a separate power connector, then the hub system is *self-powered*.
- If the hub included is part of a larger embedded system with fixed cabling and a fixed USB host, then the hub system is most likely *self-powered* (even if all of the power is derived from the upstream USB connector's VBUS pin).

Note: The self-powered or bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors that the USB host will use to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub and all of its downstream ports must continue to operate within that 500 mA budget. A USB host will typically limit the downstream ports of a self-powered hub to 100 mA. Any device that connects to a self-powered hub, which declares it needs more than 100 mA will be prevented from operating by the USB host.

9.10 Battery Charging Settings

The USB7002 hub includes built-in Dedicated Charging Port (DCP), Charging Downstream Port (CDP), and vendor-specific (SE1) battery charging support.

The USB7002 has a configuration strap option, **CFG_BC_EN**, which can be used to set the default configuration for port 1. This is located on pin 70. The strap setting is sampled one time at start-up. A configuration strap option must be selected unless the hub firmware is being executed from an external SPI Flash device. The configuration strap options are described in Table 9-7.

TABLE 9-7: CFG_BC_EN

Setting	Effect	Additional Notes
200 kΩ pull-down to GND	Port 1 BC disabled	Battery Charging is not enabled. Select this option if configuration will be done in hub OTP, via I^2C/SMBus, or by external firmware in SPI Flash. If SE1 charging is required, this strap option should be selected and SE1 must be enabled in hub OTP, via I^2C/SMBus, or by external firmware in SPI Flash.
200 kΩ pull-up to 3.3V	Port 1 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream port 1 operates in DCP mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream port 1 operates in CDP mode.
10 kΩ pull-down to GND	Port 1 and 2 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream ports 1 and 2 operate in DCP mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream ports 1 and 2 operate in CDP mode.
10 kΩ pull-up to 3.3V	Port 1, 2, and 3 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream ports 1, 2, and 3 operate in DCP mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream ports 1, 2, and 3 operate in CDP mode.
10Ω pull-down to GND	Port 1, 2, 3, and 4 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream ports 1, 2, 3, and 4 operate in DCP mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream ports 1, 2, 3, and 4 operate in CDP mode.

Note: The vendor-specific SE1 charging mode uses the USB data lines to communicate charging capability. Hence, SE1 can only be active when no USB host is present. Additional vendor-specific charging modes exist for charging at elevated current levels when an active data connection is also present. This is handled by a vendor-specific USB protocol between the USB host and the device. The USB7002 supports these vendor-specific protocol exchanges. These vendor-specific command specifications must be obtained from the respective device vendors.

10.0 HARDWARE CHECKLIST SUMMARY

TABLE 10-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.2, "Ground"	Verify that the grounds are tied together.		
	Section 2.3, "USB-IF Compliant USB Connectors"	Verify that USB-IF-compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power and Bypass Capacitance"	Section 3.0, "Power and Bypass Capacitance"	Ensure **VDD33** is in the range 3.0V to 3.6V, and a 0.1 µF capacitor is on each pin. Ensure **VDD12** is in the range 1.08V to 1.32V, and a 0.1 µF capacitor is on each pin.		
Section 4.0, "USB Signals"	Section 4.1, "Upstream Port USB Signals"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines, and do not cross the USB3 TX and RX differential pairs. If connected to a Type-C port, pay special attention to the “Side A” and “Side B” connections and ensure the routing is not crossed between the two.		
	Section 4.2, "Downstream Ports 1 and 2 USB Signals"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines, and do not cross the USB3 TX and RX differential pairs. If connected to a Type-C port, pay special attention to the “Side A” and “Side B” connections and ensure the routing is not crossed between the two.		
	Section 4.3, "Downstream Ports 3 and 4 USB Signals"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines.		
Section 4.0, "USB Signals"	Section 4.4, "Disabling Downstream Ports"	If any of the USB ports are unused, ensure they are properly disabled via pin strap. If pin strapping is not used, other methods may be used such as I^2C/SMBus configuration or OTP configuration.		
	Section 4.5, "USB Protection"	Verify that ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance of the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB2 trace. Protection devices on USB3 traces should not add more than 0.5 pF on each line.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 5.0, "USB Connectors"	Section 5.1, "Upstream Port VBUS and VBUS_DET"	Verify that the upstream port VBUS has no more than 10 µF capacitance and that the VBUS signal is properly divided down to a 3.3V signal and connected to the **VBUS_DET** pin of the hub.		
	Section 5.2, "VBUS and PRT_CTLx Connections of Downstream Ports 1 and 2"	Verify that **PRT_CTL1** and **PRT_CTL2** are properly connected to both the Enable pin of the downstream port power controller and the fault indicator output of the port power controller. Ensure the port power controller current capability is sized appropriately (500 mA, 900 mA, 1.5A, or 3A) and that the overcurrent threshold is set appropriately.		
	Section 5.3, "VBUS and PRT_CTLx Connections of Downstream Ports 3 and 4"	Verify that **PRT_CTL3** and **PRT_CTL4** are properly connected to both the Enable pin of the downstream port power controller and the fault indicator output of the port power controller. Ensure the port power controller current capability is sized appropriately (500 mA, 900 mA, or 1.5A) and that the over-current threshold is set appropriately.		
	Section 5.4, "CC1 and CC2 Connections of Downstream Ports 1 and 2"	If downstream port 1, downstream port 2, or both are standard Type-C ports, verify that **DP1_CC1** and **DP1_CC2** are properly connected to the Type-C port CC1 and CC2 pins. The VCONN supplies must also be designed such that 1W of VCONN power can be delivered to the **CC1** or **CC2** pin when enabled by the **DP1_VCONN1**, **DP1_VCONN2**, **DP2_VCONN1**, and **DP2_VCONN2** active-high Enable signals.		
	Section 5.5, "GND and EARTH Recommendations"	Verify that the USB connector is properly connected to PCB ground on both the **GND** pins and the **SHIELD** pins. It is recommended that an RC filter be placed in between the **SHIELD** pins and PCB ground.		
Section 6.0, "Clock Circuit"	Section 6.1, "Crystal and External Clock Connection"	Confirm the crystal or clock is 25.000 MHz (±50 ppm). If a single-ended clock is used, ensure it is connected to **XTALI** while leaving **XTALO** floating. If a crystal is used, ensure the loading capacitors are appropriately sized for the crystal loading requirement.		
Section 7.0, "Power and Startup"	Section 7.1, "RBIAS Resistor"	Confirm that a 12.0 kΩ 1% resistor is connected between the **RBIAS** pin and the PCB ground.		
	Section 7.2, "Board Power Supplies"	Verify that the board power supplies deliver 3.0-3.6V, and 1.08-1.32V to the hub power rails, and that the power-on rise time meets the requirement of the hub as defined in the data sheet. If the rise time requirement cannot be met, ensure that the **RESET_N** line is held low until the power regulators reach a steady state.		
	Section 7.3, "Reset Circuit"	Ensure that the RESET_N signal has an external pull-up resistor, or is otherwise properly controlled by an external SoC, MCU, or Reset supervisor device.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 8.0, "External SPI Memory"	Section 8.1, "SPI Operation Summary"	Determine if a custom SPI firmware image is required and which mode of operation the selected SPI Flash device must support.		
	Section 8.2, "Compatible SPI Flash Devices"	Ensure the selected SPI Flash device is compatible with the hub.		
	Section 8.3, "SPI Connection Diagrams"	Verify that the SPI Flash is connected according to the diagrams in Figure 8-1 or Figure 8-2. Follow Figure 8-3 if no SPI Flash is connected in the design.		
Section 9.0, "Miscellaneous"	Section 9.1, "Test Pins"	Verify that **TESTEN** is pulled to GND, **TEST1** is pulled to 3.3V, **TEST2** and **TEST3** are either pulled up to 3.3V or to GND, and **ATEST** is pulled to GND or floating.		
	Section 9.2, "GPIOs"	Verify that any GPIO pins that will be used as GPIOs within the application are connected properly, and never exceed the voltage maximums/minimums, or overload the current source/sink maximums as defined in the hub data sheet.		
	Section 9.3, "I2C/SMBus Connections"	If the USB to I^2C/SMBus slave interface is implemented, ensure that appropriate pull-up resistors are connected and that the connections to the I^2C/SMBus master are correct. Note that the pull-up resistors are detected on the I^2C/SMBus slave interface, the USB hub will not enumerate to a USB host until it receives the special “Attach” command from the I^2C/SMBus master.		
	Section 9.4, "I2S™ Connections"	If using the USB-to-I^2S bridge feature, ensure that Configuration 2 is selected via the **CFG_STRAP** pin, and ensure that the pin connections to the I^2S codec are correct. If using any codec other that the ADAU1961, ensure that it is compatible by referencing the compatibility guide in Table 9-4.		
	Section 9.5, "UART Connections"	If using the USB to UART bridge feature, ensure that Configuration 3 is selected via the **CFG_STRAP** pin, and ensure that the pin connections to the UART device or transceiver are correct.		
	Section 9.7, "FlexConnect"	If using the FlexConnect feature, contact Microchip support for design and implementation assistance.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 9.0, "Miscellaneous"	Section 9.8, "Non-Removable Port Settings"	Verify that the CFG_NON_REM configuration strap is set per application requirements. Most USB7002 applications should set this strap to the 'Port 1 Removable' setting.		
	Section 9.9, "Self-Powered/Bus-Powered Settings"	Verify the application requirements for Self-Powered or Bus-Powered operation. If Self-Powered operation is required, then no additional configuration or circuitry is required. If Bus-Powered operation is required, then the hub must be configured via OTP or I^2C/SMBus.		
	Section 9.10, "Battery Charging Settings"	Verify that the CFG_BC_EN configuration strap is set per application requirements. Most USB7002 applications should set this strap to the 'Port 1 BC Enable' setting.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002820C (02-02-22)	Figure 4-3	Updated the figure. Corrected pin number for VBUS_MON_UP and added two resistors.
DS00002820B (05-25-21)	Section 4.1, "Upstream Port USB Signals"	Corrected the information about how to connect VBUS_MON_UP when connecting to an embedded processor output or when tying to a fixed voltage.
	Figure 4-3	Fixed VBUS_MON_UP implementation in the figure to properly show resistor divider.
	Figure 4-7	Fixed incorrect figure title (now labeled as Downstream Port 3 and 4 Type-A USB Connections)
	Section 5.1, "Upstream Port VBUS and VBUS_DET"	Corrected the information about how to connect VBUS_MON_UP when tying to a fixed voltage.
	Figure 5-1	Fixed resistor divider in the figure. Simplified the USB connector symbol.
	Figure 5-2, Figure 5-3, and Figure 5-4	Fixed incorrect pin assignments for PF13, PF15, PF16, and PF17.
	Section 6.1, "Crystal and External Clock Connection"	Corrected pin number references for XTALI and XTALO (now pins 98 and 97, respectively).
	Figure 7-1 and Figure 7-2	Changed the recommended capacitor value to 1 nF.
	Section 9.1, "Test Pins"	Added this new section describing how all test pins should be connected.
	Table 10-1	Added an entry for Section 9.1, "Test Pins".
	All	Made very minor text formatting changes throughout.
DS00002820A (10-26-18)	Initial release	

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