
Libero® SoC PolarFire® Design Flow

Introduction

This application note describes how to implement the basic PolarFire® Field Programmable Gate Array (FPGA) designs using the Libero® System-on-Chip (SoC) PolarFire design tool. Each section introduces new features on top of the previous section. After completing this demo, you will be familiar with the following steps.

- [1.1. Step 1—Creating a Libero SoC PolarFire Project](#)
- [1.2. Step 2—Creating Your Design](#)
- [1.3. Step 3—Creating HDL](#)
- [1.4. Step 4—Creating SmartDesign](#)
- [1.5. HDL Testbench](#)
- [1.6. SmartDesign Testbench](#)
- [1.7. Step 5—Synthesis and Pin Assignment](#)
- [1.8. Step 6—Programming the Device](#)
- [1.9. Step 7—Running the Design](#)
- [1.10. Step 8—Design Iterations in the Libero SoC PolarFire](#)

Prerequisites

The following table lists the prerequisites for the demo.

Table 1. Prerequisites for the Demo

System Requirements	Description
Software requirements	Libero SoC PolarFire v2021.2
Hardware requirements	PolarFire Evaluation Kit (MPF300-EVAL-KIT)
Source files	Not required. The design is created from scratch

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1. Running the demo

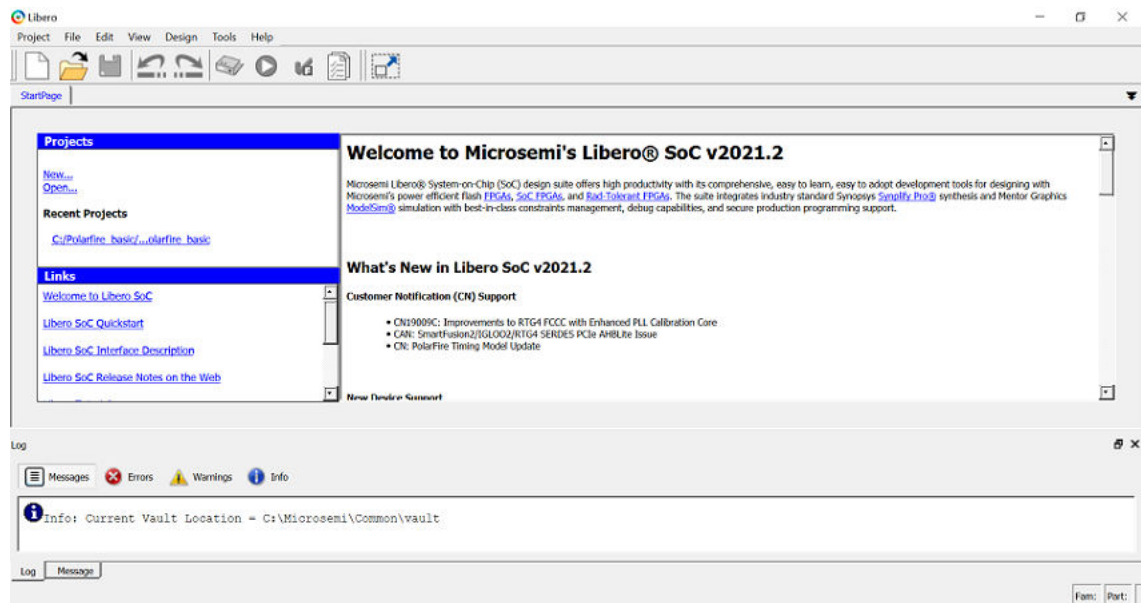
The following sections describe the step-by-step procedure to run this demo. See the [Liberio® SoC Design Flow User Guide](#) for detailed description of each step of Liberio design flow.

1.1 Step 1—Creating a Liberio SoC PolarFire Project

To create a Liberio SoC project, perform the following steps.

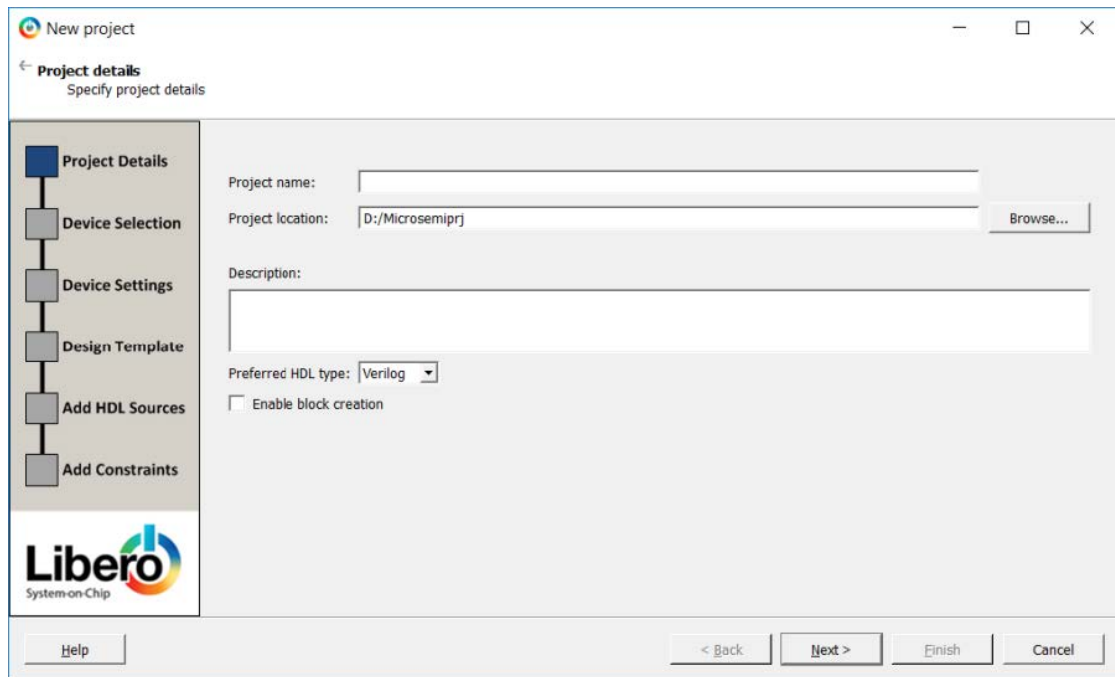
1. Click **Start > Programs > Microsemi Liberio SoC PolarFire v2021.2 > Liberio SoC PolarFire v2021.2**, or click the shortcut on your desktop. The following figure shows the Liberio SoC PolarFire Project Manager window.

Figure 1-1. Liberio SoC PolarFire Project Manager



2. To create a new project, on the **Start Page** tab, click **New** (shown in the preceding figure), from the Liberio Soc menu, click **Project > New Project** . The **New Project** window is displayed.

Figure 1-2. New Project Window



- In the **Project Details** page of the **New Project** dialog box, enter the following information and then click **Next**.

- Project name: PolarFire_basic

- Project location:

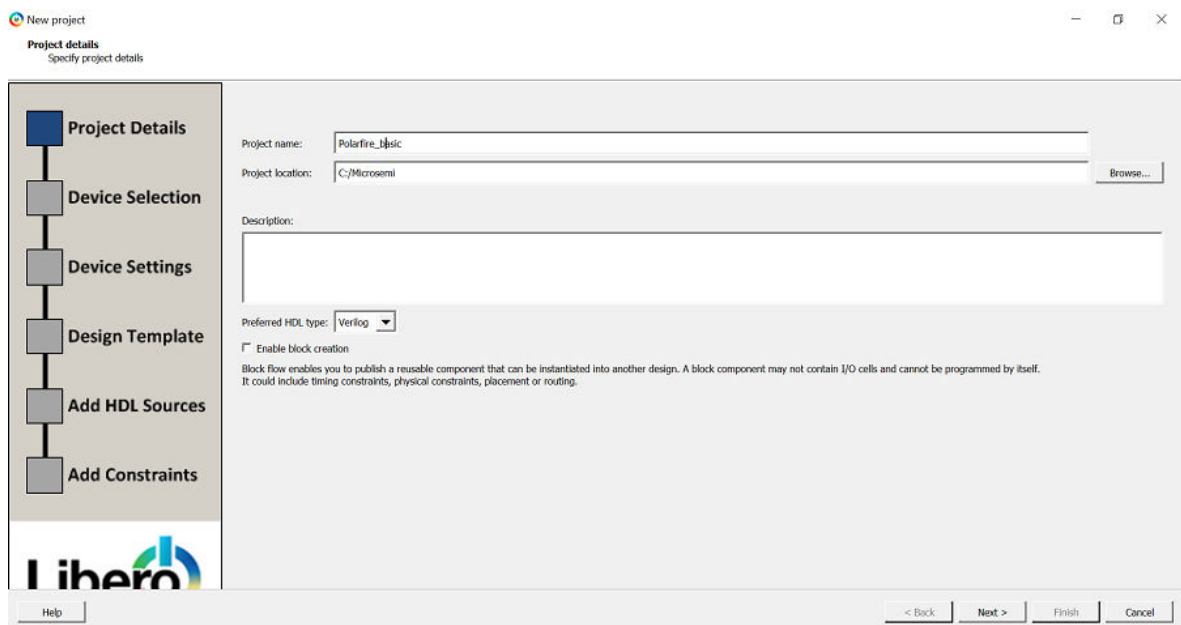
<C: or D:>/Microsemiprj

(or the path to where the files are extracted).

- Preferred HDL type: Select either VHDL or Verilog based on the HDL preferences.

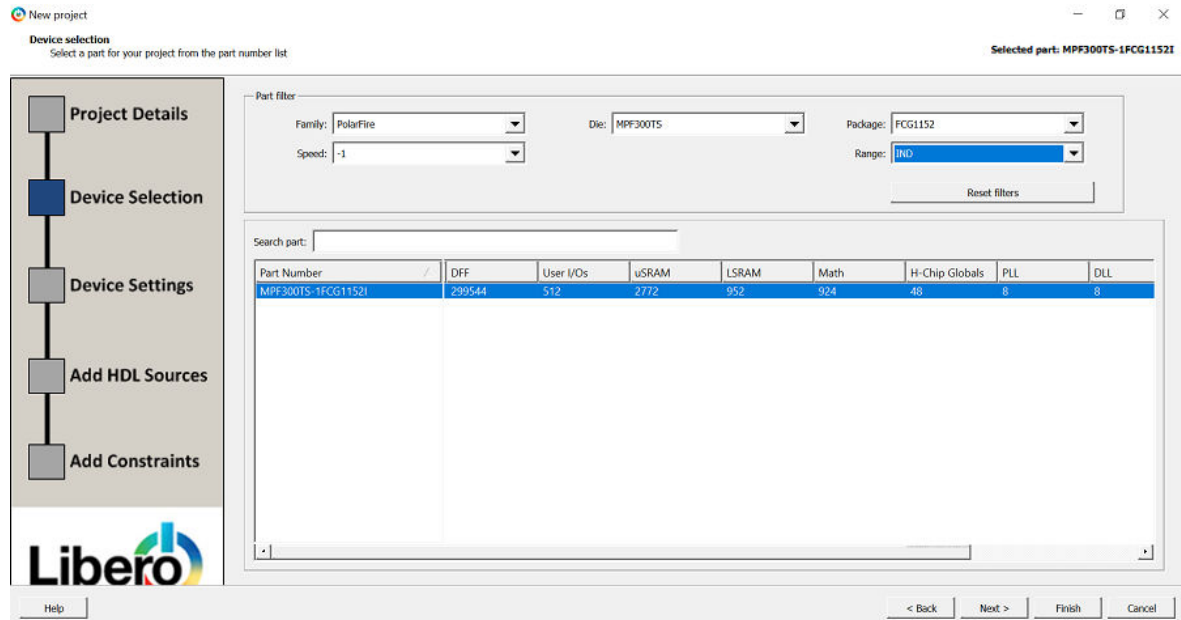
Note: Project name is case sensitive for Verilog design.

Figure 1-3. Project Details



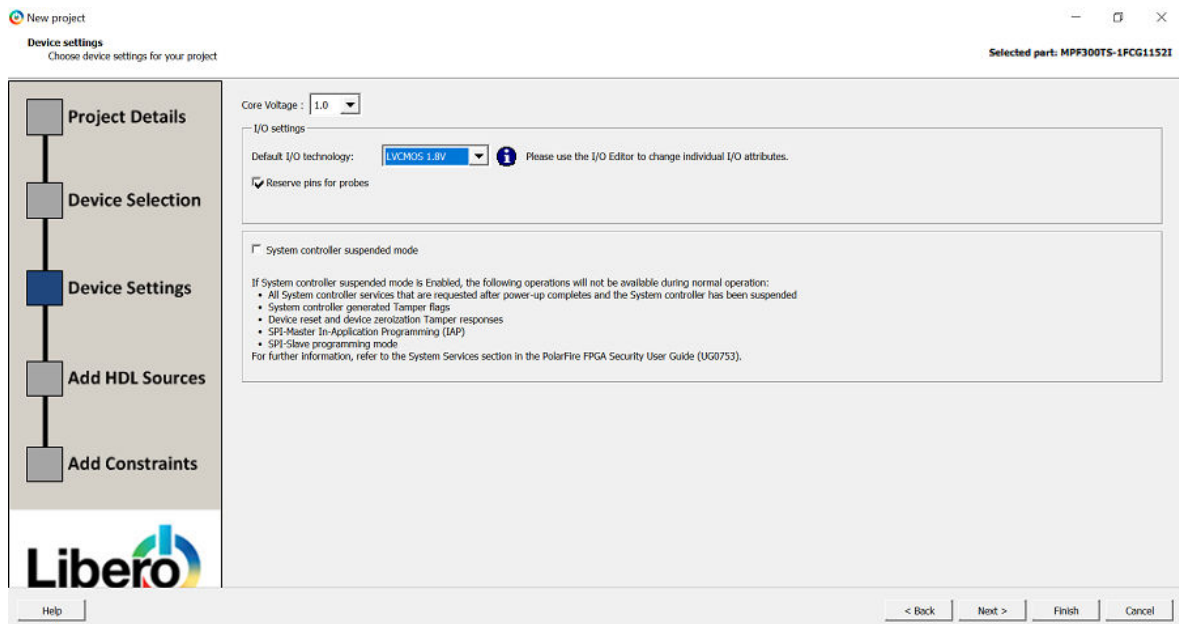
- In the **Device Selection** page of the **New Project** dialog box, enter the following details, and then click **Next**.
 - Family: PolarFire
 - Die: MPF300TS
 - Package: FCG1152
 - Speed: -1
 - Range: IND

Figure 1-4. Device Selection



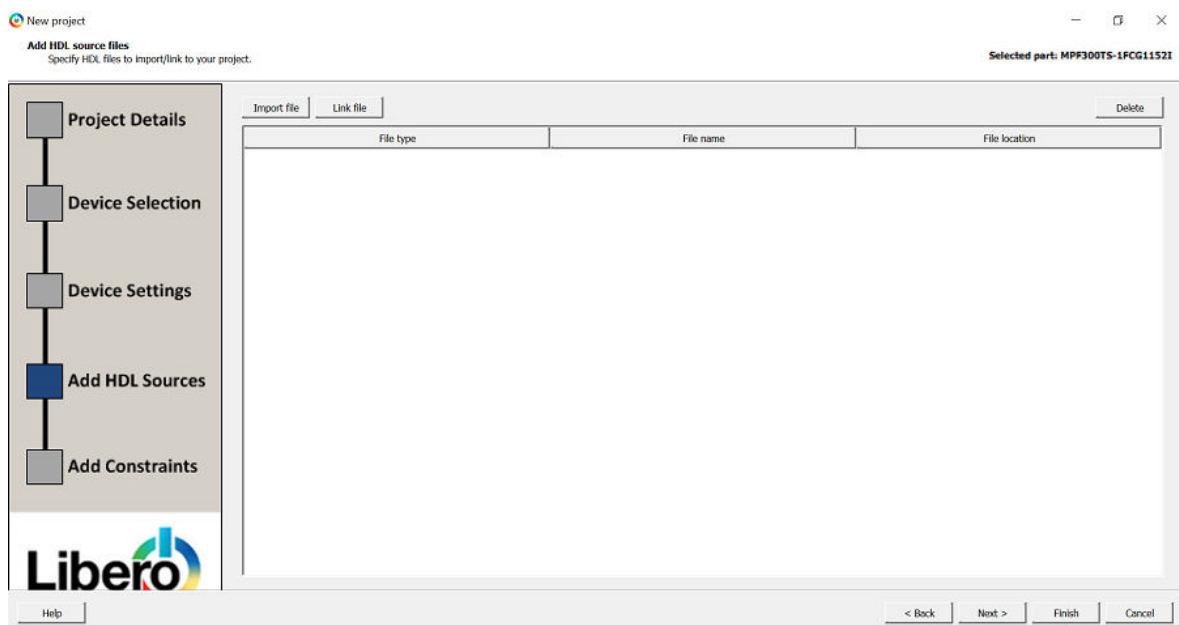
- In the **Device settings** page of the **New Project** dialog box, enter the following details, and then click **Finish**.
 - Core Voltage: 1.0 (default)
 - I/O settings
 - Default I/O technology: LVCMOS 1.8V
 - Reserve pins for probes: Checked (default)
 - System controller suspended mode: Un-checked (default)

Figure 1-5. Device Settings



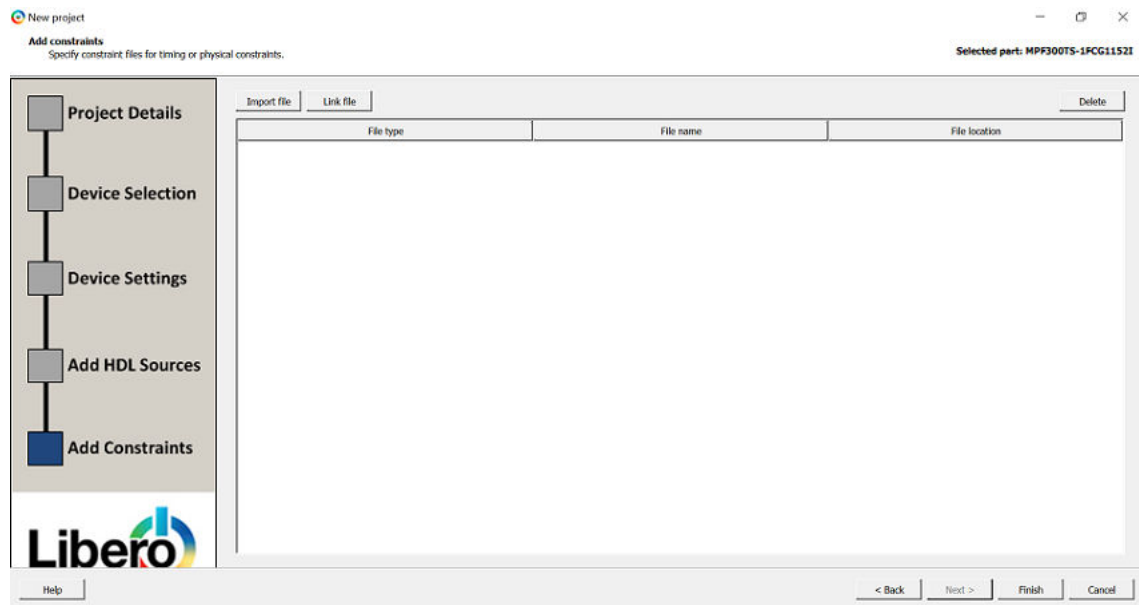
- This is the page where you can add the existing HDL design source files to your Libero SoC project. The HDL source files can be imported or linked to the Libero SoC project.

Figure 1-6. HDL Import



- In this page, you can add the timing constraints and physical constraints files to the Libero SoC project by importing or linking.

Figure 1-7. Constraints Import

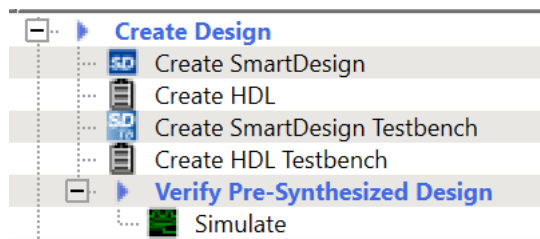


1.2 Step 2—Creating Your Design

To create a design, perform the following step.

The **Design Flow** window is used to manage design creation flow. This window has multiple tabs. You can switch between these tabs by clicking the tabs at the bottom, as shown in the following figure.

Figure 1-8. Design Creation

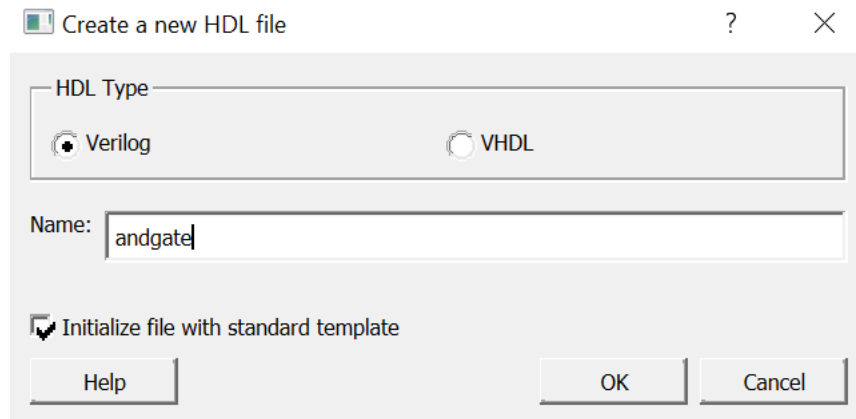


1.3 Step 3—Creating HDL

To create a design in HDL, perform the following steps.

1. Double click **Create HDL** in the **Design Flow** window . The **Create a new HDL file** dialog box is displayed.

Figure 1-9. Creating HDL



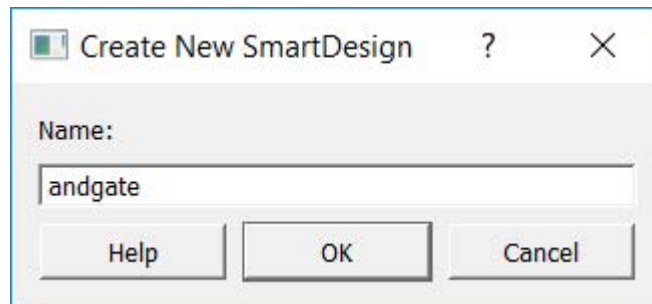
2. Under **HDL Type** section, select an option as shown in the previous figure. Select whether to **Initialize file with standard template** to populate the file with default headers and footers.
3. Enter a name and click **OK**.
Note: Do not enter a file extension because Libero SoC adds one for you, which is by default.
4. Click **Save**.

1.4 Step 4—Creating SmartDesign

To create a design in SmartDesign, perform the following steps.

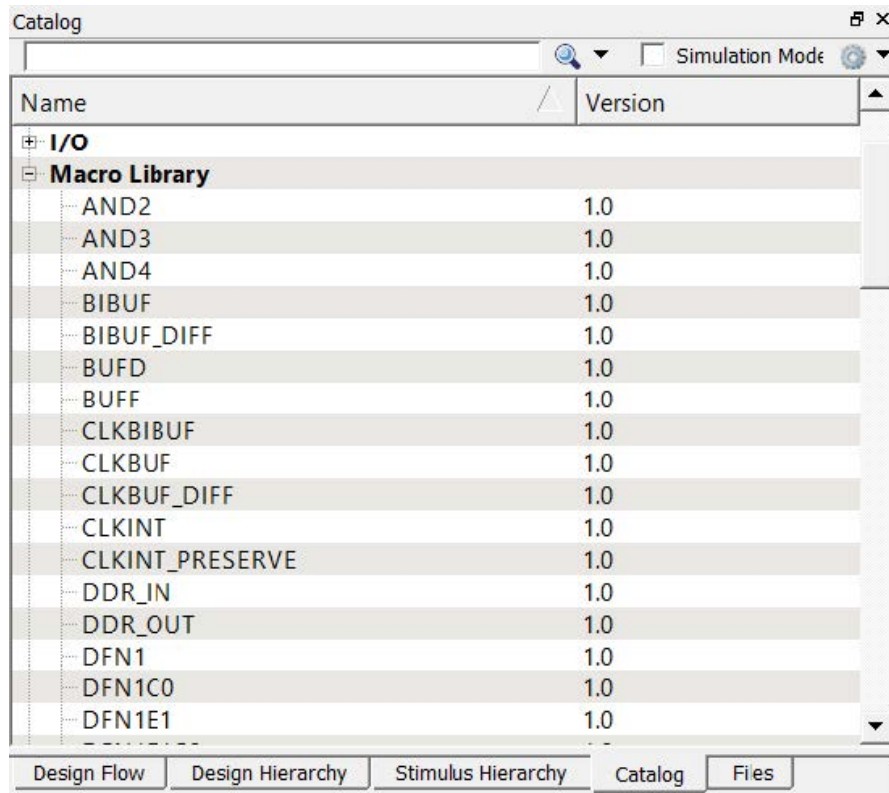
1. In the **Design Flow** window, double click **Create SmartDesign** and name your design as andgate, and then click **OK**. The **SmartDesign Canvas** is displayed.

Figure 1-10. Creating New SmartDesign



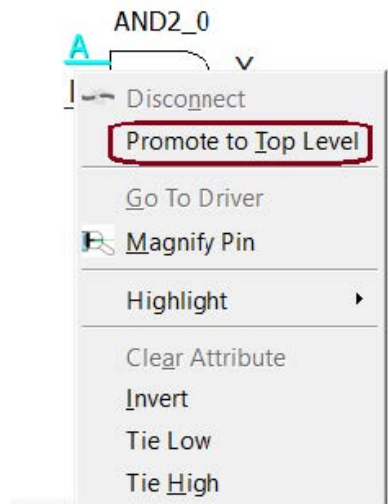
2. In the **Design Flow** window, click the **Catalog** tab, in the **Design Flow** window and then expand the **Macro Library** section, as shown in the following figure.

Figure 1-11. Catalog Tab



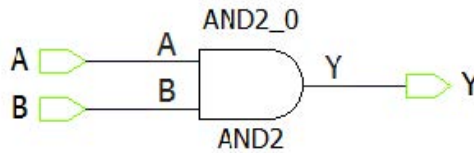
- From the **Catalog**, drag **AND2** gate onto the blank **SmartDesign Canvas** on the right.
- Select **A** and then right click to bring up the menu. From the menu, select **Promote to Top Level**, as shown in the following figure. This creates an external connection on the device that is connected to a switch. Repeat the same steps for B and Y.

Figure 1-12. AND2 Gate



- When you have completed this step, you should have the view shown in the following figure.

Figure 1-13. AND2 Connection



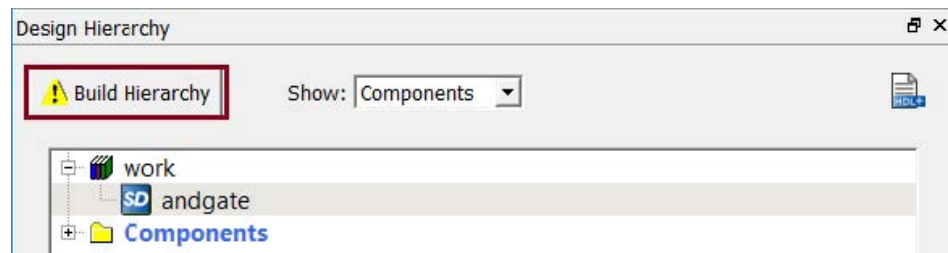
6. Click the **Generate Component** button on the top of the canvas to generate the design. The andgate was successfully generated message is displayed in the **Libero SoC Log** tab, as shown in the following figure.

Figure 1-14. Successful Message in Libero SoC Log Tab



7. Select the **Design Hierarchy** window, set andgate as root, and then click **Build Hierarchy** as shown in the following figure.

Figure 1-15. Design Hierarchy



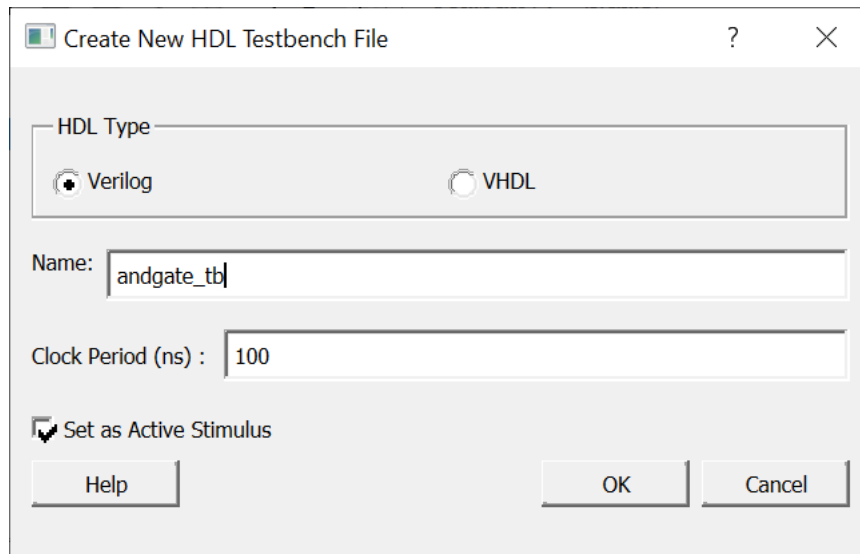
andgate is displayed in the bold font under the **Design Hierarchy** tab, indicating that it is the root level.

1.5 HDL Testbench

To create HDL Testbench, perform the following steps.

1. In the Design Hierarchy, right click **SmartDesign**, and then select **Create Testbench > HDL**. Provide a name for the testbench. The HDL testbench instantiates the selected SmartDesign into the component automatically.

Figure 1-16. HDL Testbench



2. To create a new testbench file, under **Create Design**, double click **Create HDL Testbench** to display the **Create New HDL Testbench** dialog box. The dialog box allows you to create a new testbench file, with the option to include standard testbench content and your design data.

Figure 1-17. Creating New HDL Testbench File

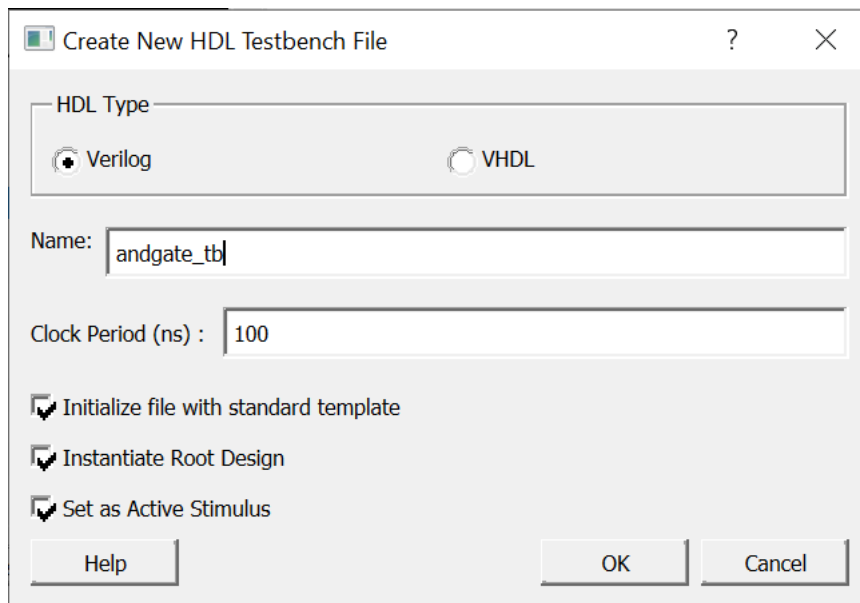


Figure 1-18. HDL Testbench File

```

`timescale 1ns/100ps

]module sample_tb;

parameter SYSCLK_PERIOD = 100;// 10MHZ

reg A,B;
wire y;

]//reg SYSCLK;
]////////////////////////////////////.
]// Instantiate Unit Under Test: andgate
]////////////////////////////////////.
]andgate andgate_0 (
    // Inputs
    .A(A),
    .B(B),
    // Outputs
    .Y(y)
    // Inouts
);

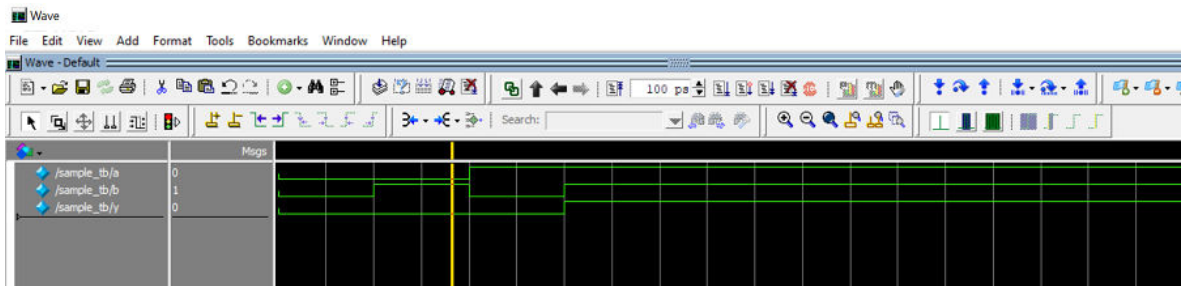
initial
]begin
    A=0; B=0;
    #100;
    A=0; B=1;
    #100;
    A=1; B=0;
    #100;
    A=1; B=1;
    #100;
end

endmodule

```

- To perform pre-synthesis simulation, go to **Stimulus Hierarchy**. Right click testbench and run **Simulate Pre-synthesis Design**. For more information, see section 4.10 in [Libero® SoC Design Flow User Guide for the all families](#).

Figure 1-19. Pre-Synthesis SIM

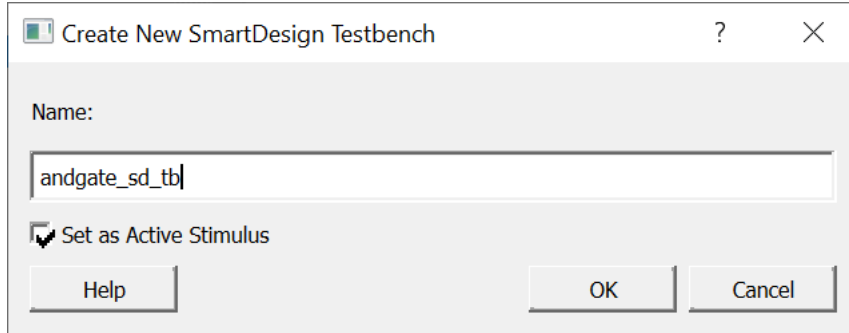


1.6 SmartDesign Testbench

SmartDesign Testbench component can be used as both top-level and lower-level testbench component.

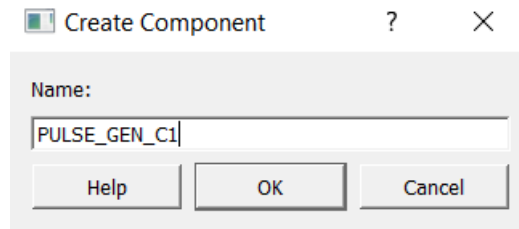
1. In the Design Flow window, double click **Create SmartDesign Testbench**. The **Create New SmartDesign Testbench** dialog box is displayed.

Figure 1-20. SmartDesign Testbench



2. Enter a unique component name.
3. Select **Set as Active Stimulus** to make this SmartDesign Testbench your active stimulus.
4. Click **OK**. The component is displayed under the **Stimulus Hierarchy** tab of the Design Explorer.
5. To perform simulation, need to add pulse generator. Go to **Catalog** tab, then select the **Simulation** option and double click pulse generator under **Clock & Management** section.

Figure 1-21. Creating Pulse Generator Component



6. In Pulse Generator configurator, set the parameters in such way that all the input combinations are generated. Repeat 5 and 6 steps to create another pulse generator.

Figure 1-22. Configuring Pulse Generator

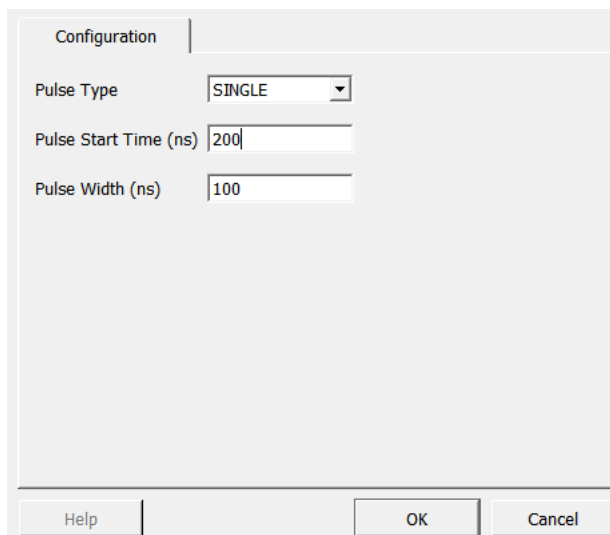
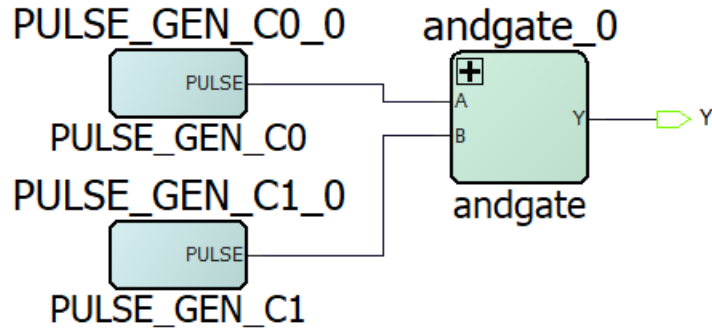


Figure 1-23. SmartDesign Testbench Canvas



To perform pre-synthesis simulation, go to **Stimulus Hierarchy**, double click **Build Hierarchy**, **save** and then right click **SmartDesign testbench** and run **Simulate Pre-synthesis Design**.

Figure 1-24. Adding Simulation

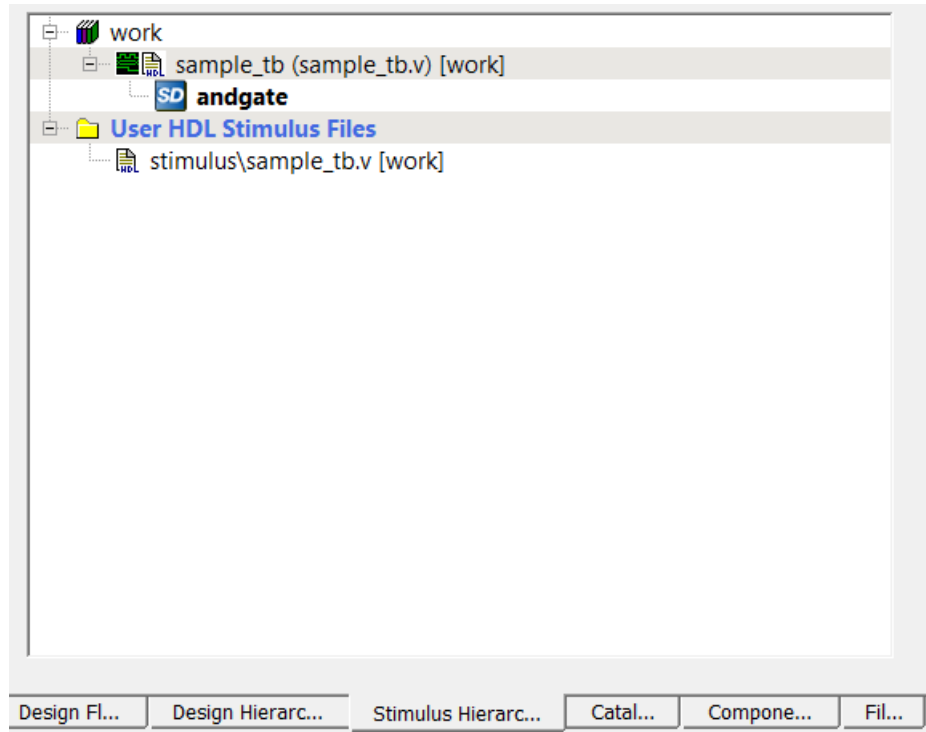
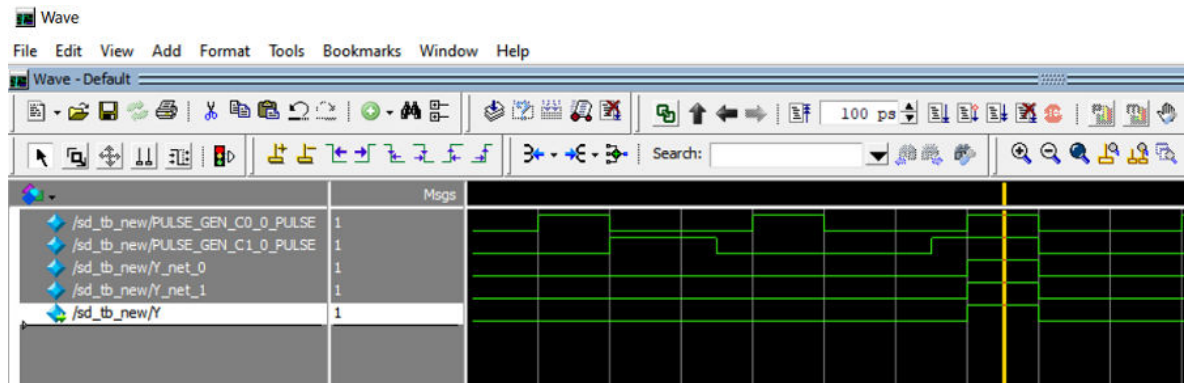


Figure 1-25. SmartDesign Pre-Synthesis SIM

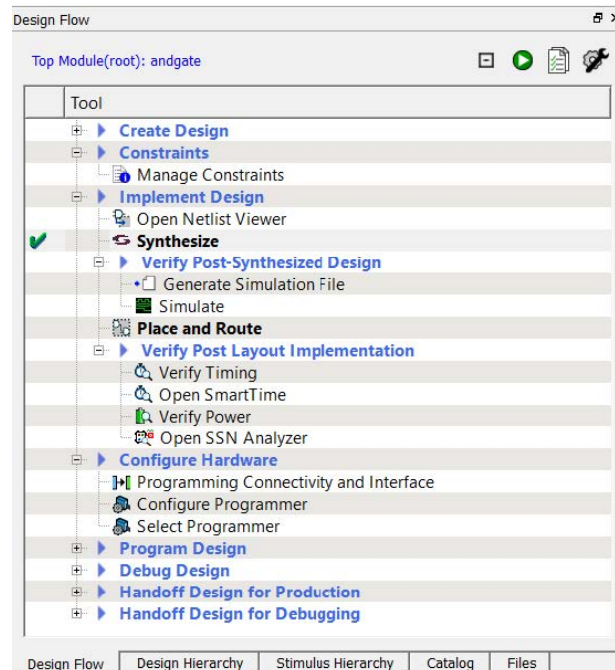


1.7 Step 5—Synthesis and Pin Assignment

To perform synthesis and assign pin, perform the following steps.

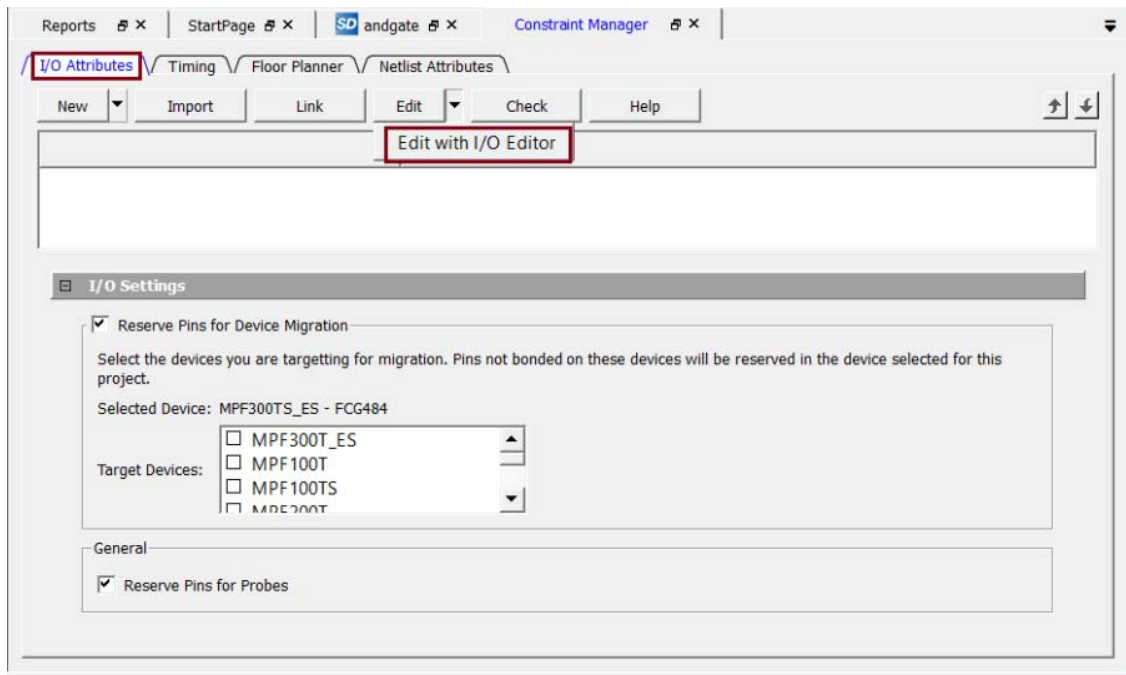
1. In the **Design Flow** window, under **Implement Design**, double click **Synthesize**, as shown in the following figure, to synthesize the design with Synplify Pro. Synplify Pro adds I/O pads to the design. A green check mark appears in the **Design Flow** window to indicate synthesis was successful.

Figure 1-26. Synthesize in Design Flow



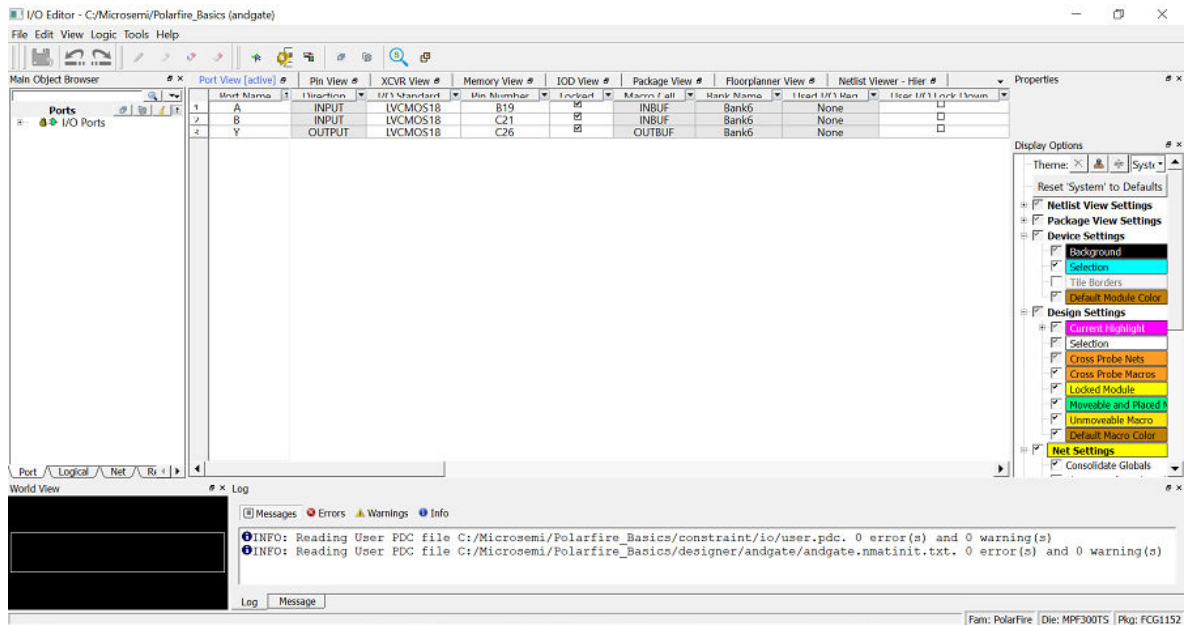
2. In the **Design Flow** window, double click **Manage Constraints** to open the **Libero SoC Constraints Manager**.

Figure 1-27. Libero SoC Constraints Manager



3. Confirm that the **I/O Attributes** tab is selected. From the list on the **Edit** button, select **Edit with I/O Editor** (highlighted in the preceding figure) to open the **I/O Editor**.
4. Select the **Port View** tab of the **I/O Editor**, as shown in the following figure.

Figure 1-28. I/O Editor



5. Use this window to set the **I/O Standard** and **Pin Number**. Confirm that LVCMOS18 is the I/O standard for each pin, as shown in the following figure.
6. In the **Pin Number** column, click **Unassigned** to reveal available I/O pins. Make the following assignments. You can either type the pin number in the field or use the list to select the pin.
 - A—B19
 - B—C21
 - Y—C26

- Ensure the connections match the following screenshot, then select **File > Commit**, and close the window by clicking **File > Exit**.

Figure 1-29. I/O Standard and Pin Number Assignments

Port Name	Direction	I/O Standard	Pin Number	Locked	Macro Call	Bank Name	Use I/O Mem	Use I/O Lock Down
A	INPUT	LVC MOS18	B19	<input checked="" type="checkbox"/>	INBUF	Bank6	None	<input type="checkbox"/>
B	INPUT	LVC MOS18	C21	<input checked="" type="checkbox"/>	INBUF	Bank6	None	<input type="checkbox"/>
Y	OUTPUT	LVC MOS18	C26	<input checked="" type="checkbox"/>	OUTBUF	Bank6	None	<input type="checkbox"/>

- To add timing constraints (if required for your design), see [Timing Constraints Editor User Guide for Libero SoC v2021.2 for all the families](#).

Push-Button Switches

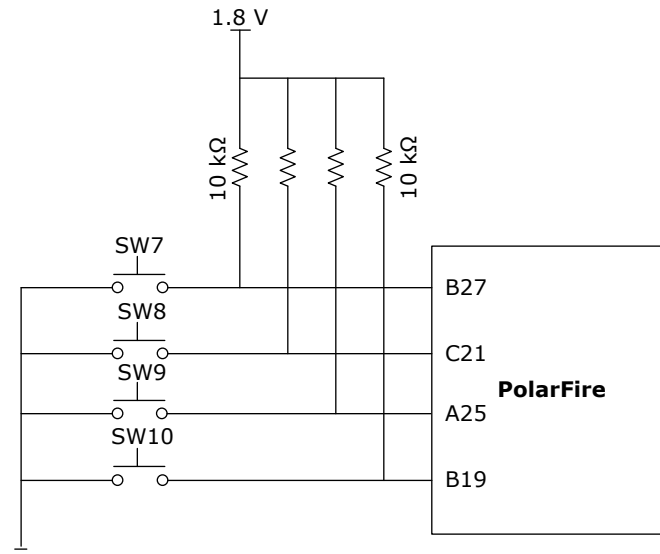
The PolarFire evaluation board comes with four debug push button switches connected to the PolarFire FPGA. The following table lists the on-board push button switches.

Table 1-1. PolarFire Evaluation Kit - Push-Button Switches

PolarFire® Evaluation Board Pin	PolarFire FPGA Pin Number	PolarFire FPGA Pin Name	Bank
SW10	B19	HSIO46PB6	Bank - 6
SW9	C21	HSIO49PB6	Bank - 6
SW8	A25	HSIO68PB6/DQS/CCC_SE_PLL1_OUT0	Bank - 6
SW7	B27	HSIO69NB6	Bank - 6

The following figure shows push button and pin connections.

Figure 1-30. Push-Button and Pin Connections



User LEDs

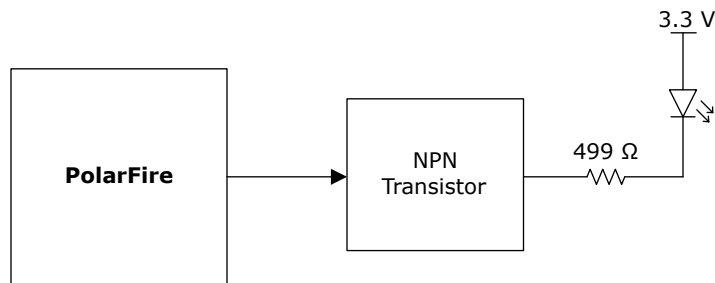
The board provides user access to eight active-high LEDs that are connected to the PolarFire device for debugging applications. The following table lists the on-board user LEDs.

Table 1-2. PolarFire Evaluation Kit - User LEDs

PolarFire® Evaluation Board Pin	PolarFire FPGA Pin Number	Number PolarFire Pin Name	Bank
LED7	D25	HSIO70PB6/CCC_SE_PLL1_OUT1	Bank - 6
LED6	C26	HSIO70NB6	Bank - 6
LED5	B26	HSIO71NB6	Bank - 6
LED4	F22	HSIO64NB6	Bank - 6
LED11	H21	HSIO36NB6	Bank - 6
LED10	H22	HSIO60NB6	Bank - 6
LED9	F23	HSIO62PB6/DQS/CCC_SE_PLL0_OUT0	Bank - 6
LED8	C27	HSIO71PB6/CCC_SE_CLKIN_S_15	Bank - 6

The following figure shows how the LEDs are connected to the PolarFire FPGA. When the PolarFire output goes high (logic 1), the LED turns on. When the output goes low (logic 0), the LED turns off.

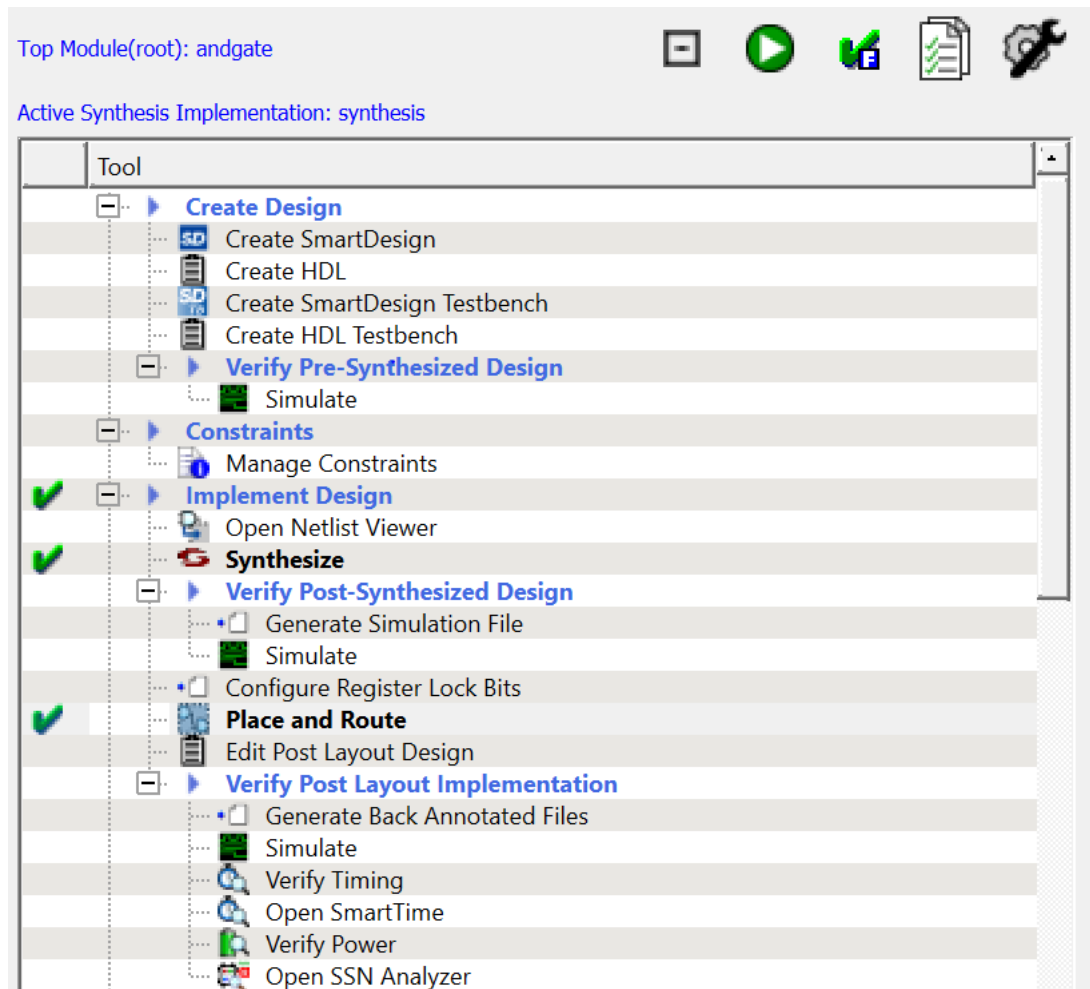
Figure 1-31. PolarFire Evaluation Kit User Defined LEDs



Note: For more information, see the [PolarFire Evaluation Board Schematic](#) document provided separately.

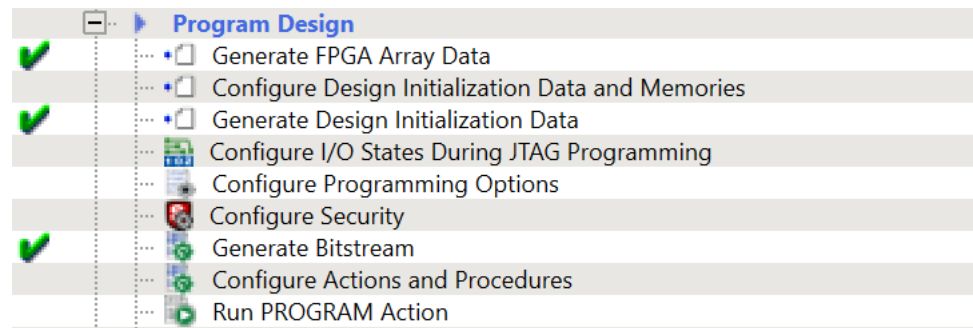
- To perform place and route, under **Implement Design** in the **Design Flow** window, double click **Place and Route**.

Figure 1-32. Place and Route



Note: Double click **Verify Timing** to perform timing analysis for sequential circuits and to analyze the generated timing report. If there are any timing violations in design, then see [SmartTime Static Timing Analysis \(STA\) for Libero SoC v2021.2 for all the families](#).

Figure 1-33. Programming Design Flow Image



Generate FPGA Array Data

Generate FPGA Array Data tool generates database files used in the following downstream tools:

- *.map files used for programming
 - RAM structural information used in Configure Design Initialization and Memories tools
- To generate FPGA array data, double click **Generate FPGA Array Data**. Ensure to complete Place and route step.

Generate Design Initialization Data

This tool is used to generate initialization data of the design, if there are any initialization clients of Fabric RAMs.

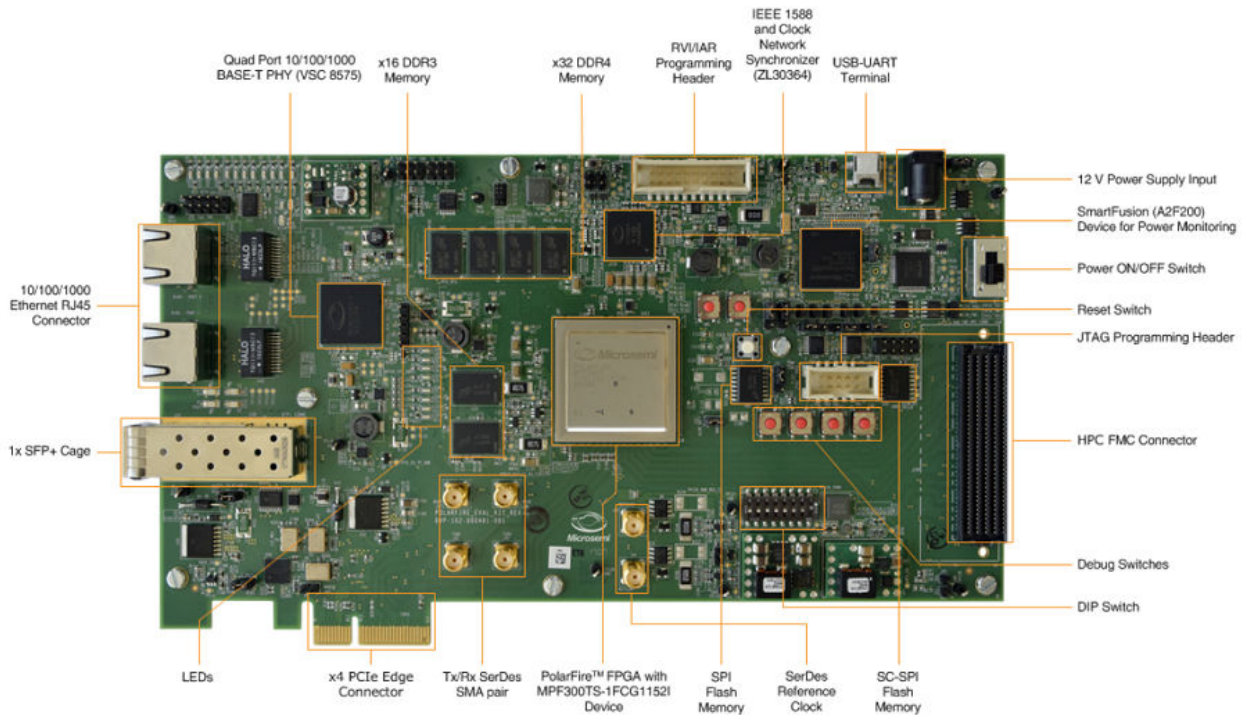
Generate Bitstream

This tool incorporates the fabric design, sNVM configuration, eNVM configuration (if configured), and custom security settings (if configured) to generate the bit stream file. Before you generate the bit stream, configure the bit stream. Otherwise, default settings with all available features included are used. To display the Configure Bit stream dialog box, expand **Program Design**, right click **Generate Bitstream**, and then select **Configure Options** to select the components you want to program.

1.8 Step 6—Programming the Device

The following steps describe how to run the FlashPro in batch mode to program the PolarFire MPG300 on the PolarFire evaluation board, as shown in the following figure.

Figure 1-34. PolarFire Evaluation Kit Board



1. Prior to programming (and powering up) the PolarFire evaluation board, confirm that the jumpers are positioned as listed in the following table.

Table 1-3. Jumper Settings

Jumper	Description	Pin	Default Setting
J18, J19, J20, J21, J22	Jumpers to select the PolarFire JTAG or A2F JTAG	Close pin 1 and 2 for programming the power sequence and monitoring chip through the FTDI. Close pin 2 and 3 for programming the PolarFire® FPGA through FTDI. You must always retain the default jumper setting.	Open Closed

.....continued

Jumper	Description	Pin	Default Setting
J46	Jumper to select switch-side MUX inputs of A or B to the line side	Close pin 1 and 2 (Input A to the line side) for routing the on-board 122.88 MHz differential clock oscillator output to the line side. Close pin 1 and 2 (Input B to the line side) for routing the on-board 125 MHz differential clock oscillator output to the line side.	Open Closed
J28	Jumper to select the external JTAG or the onboard FlashPro5 for programming the PolarFire device	Close pin 1 and 2 for programming through the on-board FlashPro5.	Closed
J26	Jumper to select the FTDI SPI or SC_SPI header	Close pin 1 and 2 for programming through the SC_SPI Header.	Open
J27	Jumper to select between FTDI SPI or External SPI Flash to program the device	Close pin 1 and 2 for programming through the External SPI Flash.	Open
J23	Jumper to define the SPI interface mode	Close pin 1 and 2 to define the SPI Slave mode.	Open
J4	Jumper to select the SW3 input or the ENABLE_FT4232 signal from the FT4232H chip	Close pin 1 and 2 for manual power switching using SW3. Close pin 2 and 3 for remote power switching using the GPIO capability of the FT4232 chip.	Closed Open
J12	Jumper to select the PolarFire VCCIO voltage (VCCIO_HPC_VA DJ) to 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V	Close pin 1 and 2 for 3.3V. Close pin 3 and 4 for 2.5V. Close pin 5 and 6 for 1.8V. Close pin 7 and 8 for 1.5V. Close pin 9 and 10 for 1.2V.	Open Closed Open Open Open
J43	Jumper to select the VDD voltage	Close pin 1 and 2 for 1.05V	Open

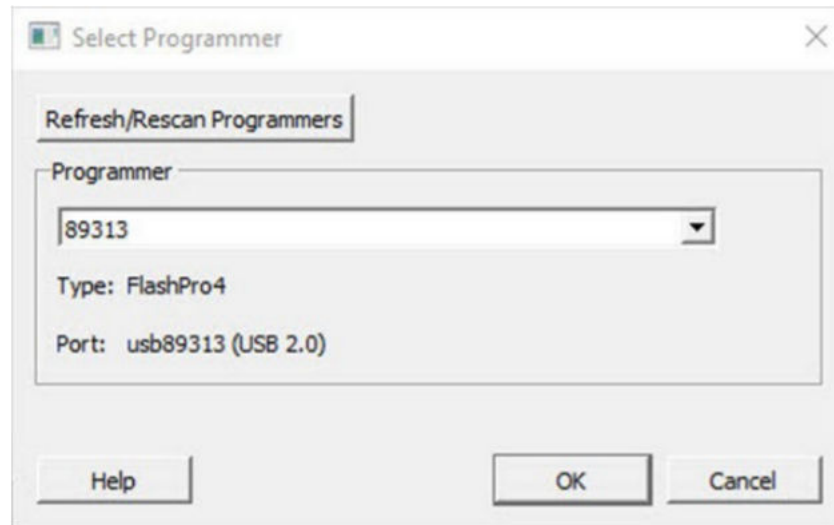
2. Connect 12V power supply brick to the J2 connector.
3. Connect a USB cable between the J1 mini USB connector and the host PC.
4. Slide the main power switch SW1 to ON.
5. Install the FlashPro4 drivers if prompted. The drivers are located in the

```
<Libero SoC PolarFire v2021.2 Installation Directory>\drivers
```

folder.

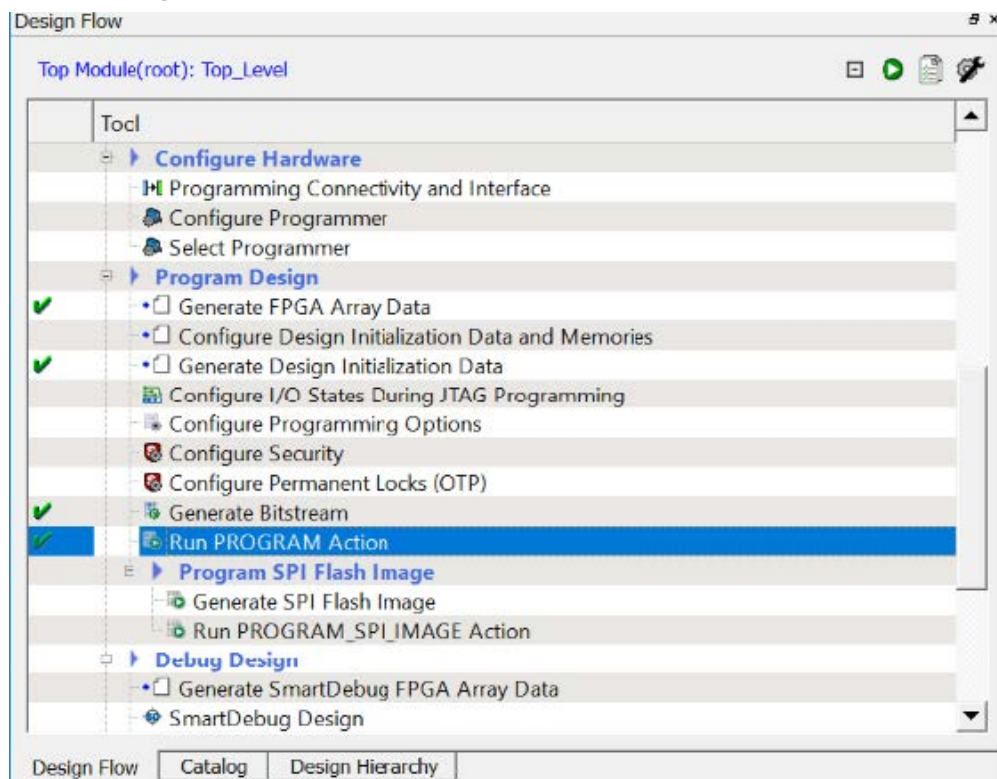
6. To program the design, a programmer must be selected. For that, expand the Configure Hardware, double-click **Select Programmer**. From the list, select the programmer you want to use. If no programmers are connected, connect a programmer without closing the dialog box, and then click **Refresh/Rescan Programmers** to display the connected programmer from the list.

Figure 1-35. Select Programmer Dialog Box



7. In the **Design Flow** window, expand **Program Design**. Right click **Run PROGRAM Action** and select **Run** to generate the programming file and begin programming.

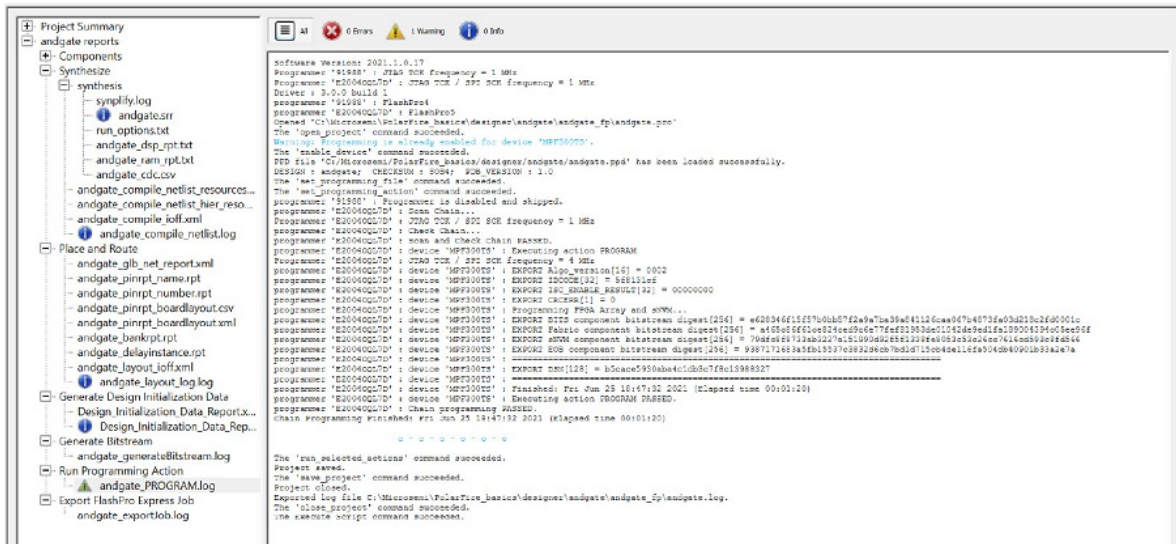
Figure 1-36. Run Program Action



8. FlashPro runs in batch mode and programs the device. Programming messages are visible in the **Libero SoC log** window (programmer number differs).
Note: Do not interrupt the programming sequence.
9. The following message is displayed in the **Reports** view under **Run PROGRAM Action**, when the device is programmed successfully (programmer number differs).

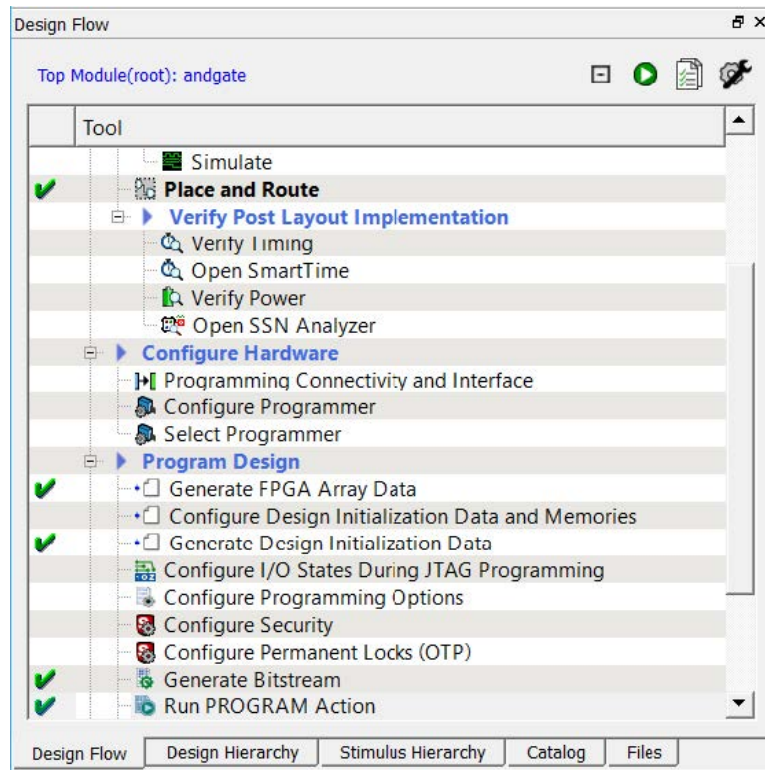
```
programmer 'E2001JZK2X': device 'MPF300T_ES': Executing action PROGRAM PASSED.
programmer 'E2004OQL7D': device 'MPF300TS': Executing action PROGRAM PASSED.
```

Figure 1-37. Reports Tab



A green tick mark appears next to **Program Design and Run PROGRAM Action** in the **Design Flow** window to indicate successful programming as shown in the following figure.

Figure 1-38. Design Flow Green Tick Marks



- To save your completed project, from the Libero menu, click **Project > Save**.
Note: Do not close the window.

To debug your design in real time, use SmartDebug tool. For more information about SmartDebug tool, see [SmartDesign v2021.2 User Guide for all the families](#).

1.9 Step 7—Running the Design

This is a very simple design designed to show an AND gate. The following steps are performed to run the design.

1. Observe LED1 with switch 5 and switch 6 released—it illuminates.
2. Press switch 5 and observe the behavior of LED1—it turns OFF.
3. Press switch 6 and observe the behavior of LED1—it turns OFF.
4. Press both switches to turn OFF LED1.

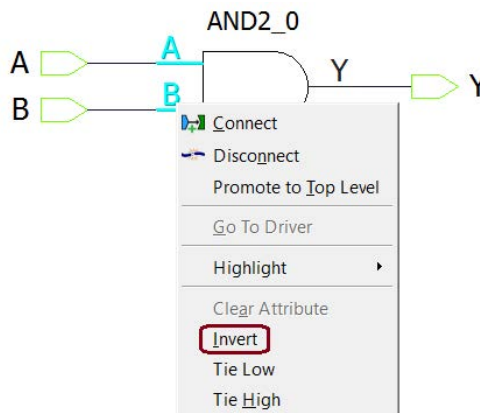
For an AND gate, you might expect the LED to illuminate when both switches are pressed, but in this application, releasing the switch generates a logic one, which illuminates the LED. To correct this, you must invert the inputs to the AND gate. For more information, see Figure 16 Switches Interface in [UG0747: PolarFire FPGA Evaluation Kit User Guide](#).

1.10 Step 8—Design Iterations in the Libero SoC PolarFire

To design iteration in the Libero SoC PolarFire v2021.2, perform the following steps.

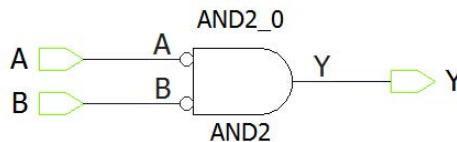
1. Reopen the **SmartDesign** Canvas again, look for the andgate tab.
2. Hold the **Ctrl** key and select input ports **A** and **B** of AND2_0, then right click to bring up the menu. Select **Invert** to invert the signals, as shown in the following figure. This is built into the SmartDesign capabilities to invert or tie off any I/O.

Figure 1-39. Design Iterations



The ports are inverted.

Figure 1-40. Ports Inversion



3. Generate the Component . It resets the rest of the compilation functions, but keeps your I/O constraints.
4. In the **Design flow** window, right click **Run PROGRAM Action** , then select **Update and Run** to run all the steps in between and reprogram the device in one click.
5. Check if the **Warning** dialog box about running in non-timing-driven mode is displayed behind your active window.
6. Observe the correct behavior on the board by pressing both switches simultaneously to illuminate LED1. This step completes the tutorial of the Libero SoC PolarFire v2021.2 design flow.

2. References

The following documents are referred for this demo.

- [UG0758: PolarFire FPGA Design Flow User Guide](#)
- [UG0779: SmartDesign User Guide for PolarFire](#)
- [UG0750: PolarFire FPGA I/O Editor User Guide](#)
- [PolarFire FPGA Tcl Commands Reference Guide](#)
- [UG0776: PolarFire FPGA Design Constraints User Guide](#)
- [UG0769: Timing Constraints Editor User Guide for PolarFire](#)
- [UG0738: Netlist Viewer Interface User Guide for PolarFire](#)
- [UG0821: PolarFire FPGA Chip Planner User Guide](#)
- [SmartPower User Guide for Libero SoC PolarFire](#)
- [UG0773: PolarFire FPGA SmartDebug User Guide](#)

3. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	04/2022	<p>The following is the list of changes in revision A of the document:</p> <ul style="list-style-type: none"> • The document was migrated to the Microchip template. • The document number was updated to DS00004528A from 50200844.
3.0	—	<p>The following is a summary of the changes in revision 3.0 of this document.</p> <ul style="list-style-type: none"> • Updated the document for Libero SoC v2021.2. • Updated section 1.1. Step 1—Creating a Libero SoC PolarFire Project • Updated section 1.2. Step 2—Creating Your Design • Added section 1.3. Step 3—Creating HDL • Added section 1.4. Step 4—Creating SmartDesign • Added section 1.5. HDL Testbench • Added section 1.6. SmartDesign Testbench • Updated section 1.7. Step 5—Synthesis and Pin Assignment • Updated section 1.8. Step 6—Programming the Device
2.0	—	<p>The following is a summary of the changes in revision 2.0 of this document.</p> <ul style="list-style-type: none"> • Updated section 1.1. Step 1—Creating a Libero SoC PolarFire Project • Updated section 1.7. Step 5—Synthesis and Pin Assignment
1.0	09/2018	Initial Revision.

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