



Flash Microcontrollers

Application Note

Migrating from Philips P89LPC913 to Atmel AT89LP214

1. Introduction

The Atmel® AT89LP214 can replace the Philips® P89LPC913 directly in an existing application provided that the following software differences are taken into consideration.

2. Pin Mapping

[Table 2-1](#) shows how the pins of P89LPC913 map to the pins of AT89LP214. While alternate functions such as the SPI or UART pins are in identical locations, their respective assigned port pins are different (e.g. pin 1 is MOSI in both devices but it is P2.2 in P89LPC913 and P1.5 in AT89LP214.)

Table 2-1. Pin Mapping Comparison

Pin	P89LPC913		AT89LP214	
1	P2.2	MOSI	P1.5	MOSI
2	P2.5	SPICLK	P1.7	SCK
3	P1.5	$\overline{\text{RST}}$	P1.3	$\overline{\text{RST}}$
4	VSS		GND	
5	P0.6	KBI6	P1.2	GPI2
6	P1.1	RXD	P3.0	RXD
7	P3.1	XTAL1	P3.2	XTAL1
8	P3.0	XTAL2/CLKOUT	P3.3	XTAL2/CLKOUT
9	P1.0	TXD	P3.1	TXD
10	VDD		VDD	
11	P0.5	KBI5/CMPREF(-)	P1.0	GPI0/AIN0(+)
12	P0.4	KBI4/CIN1A(+)	P1.1	GPI1/AIN1(-)
13	P0.2	KBI2	P1.4	GPI4
14	P2.3	MISO	P1.6	MISO



3. Port Configuration

The 12 I/O pins of P89LPC913 span four ports whereas the pins of the AT89LP214 span only two ports. The 8 port configuration registers in P89LPC913 are mapped into only 4 registers in AT89LP214.

Table 3-1. Px.y Pin Configuration

P89LPC913		AT89LP214		I/O Mode
PxM1	PxM2	PxM0	PxM1	
0	0	0	0	Quasi-bidirectional
0	1	0	1	Push-pull Output
1	0	1	0	Input-only
1	1	1	1	Open-drain

SFRs controlling port direction in the P89LPC913:

P0M1	84H
P0M2	85H
P1M1	91H
P1M2	92H
P2M1	A4H
P2M2	A5H
P3M1	B1H
P3M2	B2H

The functions above are mapped together into the following SFRs in the AT89LP214:

P1M0	C2H
P1M1	C3H
P3M0	C6H
P3M1	C7H

For example:

- To configure AT89LP214 P3.0 (RXD) which corresponds to P89LPC913 P1.1 (RXD), use the following SFR bits:
 - P3M0.0 (C6H) instead of P1M1.1 (91H)
 - P3M1.0 (C7H) instead of P1M2.1 (92H)
- To configure AT89LP214 P1.7 (SCK) which corresponds to P89LPC913 P2.5 (SPI-CLK), use the following SFR bits:
 - P1M0.7 (C2H) instead of P2M1.5 (A4H)
 - P1M1.7 (C3H) instead of P2M2.5 (A5H)

4. SPI Migration

4.1 SPI SFR Mapping

1. P89LPC913 SPCTL.7 (SSIG) maps into AT89LP214 SPSR.2 (SSIG).
2. P89LPC913 SPI Interrupt has exclusive vector 004BH whereas AT89LP214 SPI Interrupt shares vector 0023H with UART.

The P89LPC913 SPI Interrupt is enabled by IEN1.3 (ESPI) at E8H. The AT89LP214 SPI Interrupt is enabled by SPCR.7 (SPIE) in conjunction with IE.4 (ES) at A8H.

The P89LPC913 SPI Interrupt priority is controlled by IP1.4 (PSPI) at F8H and IP1H.4 (PSPIH) at F7H. The AT89LP214 SPI Interrupt priority is controlled by IP.4 (PS) at B8H and IPH.4 (PSH) at B7H.

3. P89LPC913 supports clock ratios of 4, 16, 64, and 128 for SCK. AT89LP214 supports clock ratios of 4, 8, 32, and 64 for SCK.
4. The SPIF and WCOL flags are cleared in P89LPC913 by writing 1s to them. The flags are cleared in AT89LP214 by first reading SPSR and then reading or writing SPDR.

P89LPC913		AT89LP214	
SPSTAT	E1H	SPSR	E8H
SPCTL	E2H	SPCR	E9H
SPDAT	E3H	SPDR	EAH

5. UART Migration

1. The clock rate for Mode 0 is 1/16 in P89LPC913, but 1/2 in AT89LP214.
2. Modes 1, 2, and 3 operate identically.
3. AT89LP214 does not include a separate baud rate generator and therefore must use Timer 1 for Modes 1 or 3. Note that Timer 1 in AT89LP214 counts at twice the rate of Timer 1 in P89LPC913. To achieve the same timing, TPS (CLKREG[7-4], address 8FH) should be set to 0001.
4. AT89LP214 does not support enhanced UART features of P89LPC913 such as Break Detect, Overrun Error, Double Buffering, or separate TI/RI interrupts.

6. Watchdog Migration

The WDT in AT89LP214 always runs on the system clock and can only generate a reset.

Table 6-1. Watchdog Overflow Period (in clock cycles)

P89LPC913	$(2^{(5+PRE)} * (WDL+1)) + 1$
AT89LP214	$2^{(14+PS)} * (TPS+1)$

Table 6-2. Watchdog SFR Mapping

P89LPC913		AT89LP214	
WDCON	A7H	WDTCN	A7H
WFEEED1	C2H	WDTRST	A6H
WFEEED2	C3H	WDTRST	A6H
WDL	C1H		

The current status of the WDT is found in the following registers:

P89LPC913	WDCON.2 (WDRUN)
AT89LP214	WDTCN.0 (WDTEN)

P89LPC913 Feed Sequence:

```
CLR    EA                ; disable interrupt
MOV    WFEEED1,#0A5H    ; start watchdog feed part 1
MOV    WFEEED2,#05AH    ; start watchdog feed part 2
SETB   EA                ; enable interrupt
```

AT89LP214 Feed Sequence:

```
CLR    EA                ; disable interrupt
MOV    WDTRST,#01EH     ; start watchdog feed part 1
MOV    WDTRST,#0E1H     ; start watchdog feed part 2
SETB   EA                ; enable interrupt
```

7. Analog Comparator Migration

7.1 Comparator SFR Mapping

1. The AT89LP214 supports only comparator 1 without internal reference.
2. The comparator inputs in the AT89LP214 have reversed polarity from P89LPC913 (+/- are swapped) such that the comparator output will be complemented for the same input condition.
3. P89LPC913 comparator Interrupt has vector 0043H whereas AT89LP214 comparator Interrupt has vector 0033H.

The P89LPC913 comparator Interrupt is enabled by IEN1.2 (EC) at E8H. The AT89LP214 comparator Interrupt is enabled by IE.6 (EC) at A8H.

The P89LPC913 comparator Interrupt priority is controlled by IP1.3 (PC) at F8H and IP1H.3 (PCH) at F7H. The AT89LP214 comparator Interrupt priority is always fixed at the lowest priority.

4. The comparator is enabled by CMP1.5 in P89LPC913 but by ACSR.3 in AT89LP214.
5. The comparator interrupt flag is located at CMP1.0 in P89LPC913 bit at ACSR.4 in AT89LP214.
6. The comparator output is read from CMP1.1 in P89LPC913 but from P3.6 in AT89LP214.

P89LPC913		AT89LP214	
CMP1	ACH	ACSR	97H

8. Keypad Interrupt Migration

The General-purpose Interrupt (GPI) block in AT89LP214 cannot replicate the pattern matching function of the P89LPC913 Keypad Interrupt. However, the GPI can implement the original KBI functionality for low level pin detection (KBPATN = FFH and PATN_SEL=0).

This can be achieved by moving the mask value to GPIEN (9CH) instead of KBMASK (86H). All other register can remain at their default values.

8.1 Keypad SFR Mapping

1. P89LPC913 Keypad Interrupt has vector 003BH whereas AT89LP214 GPI Interrupt has vector 002BH.

The P89LPC913 Keypad Interrupt is enabled by IEN1.1 (EKBI) at E8H. The AT89LP214 GPI Interrupt is enabled by IE.5 (EGP) at A8H.

The P89LPC913 Keypad Interrupt priority is controlled by IP1.1 (PKBI) at F8H and IP1H.1 (PKBIH) at F7H. The AT89LP214 SPI Interrupt priority is controlled by IP.5 (PGP) at B8H and IPH.5 (PGPH) at B7H.

2. The P89LPC913 has a single interrupt flag located at KBCON.0 (94H). The AT89LP214 has one flag for each pin located in GPIF (9DH).

P89LPC913		AT89LP214	
KBCON	94H	GPIF	9DH
KBMASK	86H	GPIEN	9CH
KBPATN	93H	GPLS	9BH
		GPMOD	9AH

9. Timer Migration

By default the timers in AT89LP214 count at twice the rate of the timers in P89LPC913. To achieve the same timing, TPS (CLKREG[7-4], address 8FH) should be set to 0001.

9.1 Clock-Out

In the P89LPC913, the clock-out feature is enabled by the ENCLK bit at TRIM.6 (96H). In the AT89LP214 clock-out is enabled by bit COE in CLKREG.0 (8FH).

9.2 Software Reset

In the P89LPC913, a software reset is generated by setting the SRST bit at AUXR1.3 (A2H). In the AT89LP214, a software reset is generated by writing the sequence 5AH/A5H to WDTRST (A6H).

```
CLR    EA                ; disable interrupt
MOV    WDTRST, #05AH     ; start software part 1
MOV    WDTRST, #0A5H     ; start software part 2
```



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenalux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High-Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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