dsPIC30F to dsPIC33F Conversion Guidelines

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GENERAL INFORMATION

This document provides an overview of considerations for converting from dsPIC30F to dsPIC33F devices. If you are undertaking this conversion, it is recommended that you download data sheets and errata documents on these devices from our web site, *www.microchip.com*.

The dsPIC33F devices are 3.3 VDC operational devices. If the dsPIC30F design was originally implemented at 3.3 VDC, this would greatly simplify the conversion to the dsPIC33F family.

Both families are pin-compatible with the exception of one pin on the 64- and 80-pin devices. The dsPIC33F VDDCORE pin (pin 56 on 64-pin TQFP and pin 70 on 80-pin TQFP) must be connected to circuit ground via a 1µF capacitor. This same pin on the dsPIC30F devices is a VSS pin and hence must be tied to ground. A jumper can be used to replace the capacitor to connect to the Vss pin.

The Low-Voltage-Detect (LVD) feature on the dsPIC30F devices is not available on the dsPIC33F devices. Conversion can be simplified if the dsPIC30F LVD feature is not implemented.

The dsPIC33F devices support a Brown-out Reset (BOR) feature, but not an equivalent dsPIC30F BOR with adjustable trip points.

Both families support Programmable Power-up Timer (POR). The port I/O sink/source current is 4mA for the dsPIC33F devices versus 25mA for the dsPIC30F devices.

Run, Sleep and Idle currents are not yet characterized. Run and Idle currents will be reduced on the dsPIC33F devices versus the dsPIC30F devices.

The dsPIC33F devices have a programmable PLL, whereas the dsPIC30F PLL features x4, x8 or x16 modes.

The instruction set on the dsPIC33F and dsPIC30F devices is 100% identical. In general, Assembly and C language code developed for the dsPIC30F devices is directly portable to dsPIC33F devices using the associated device header (.h), include (.inc) and linker (.gld) support files. dsPIC33F devices support more interrupt sources, therefore the interrupt vector table length has increased. User code starts at 0x200 versus 0x100 on the dsPIC30F devices. Using the associated device linker (.gld) support file makes this change transparent.

Some peripherals have new features hence additional bits have been added in respective SFRs. Some SFR bits have moved or been renamed between the dsPIC30F and dsPIC33F devices. If the Assembly and C language code utilizes the provided device support files, code migration is straight forward.

Table 1 presents a summary of the key differences between the dsPIC30F to dsPIC33F devices. Please refer to the specific device data sheets for further information.

TABLE 1: KEY DIFFERENCES BETWEEN dsPIC30F AND dsPIC33F DEVICES

Peripheral Module	Channels		Comments
	dsPIC30F	dsPIC33F	
Interrupt Controller	45	67	SFR bits are located in different SFRs. There are more interrupts and associated SFRs on the dsPIC33F devices. Old SFR bit names are retained for compatibility.
Timers 16-bit	5	9	No SFR bit name changes. Four new timers on the dsPIC33F devices.
Input Capture	5	8	No SFR bit name changes. Three new channels on the dsPIC33F devices.
Output Compare	5	8	No SFR bit name changes. Three new channels on the dsPIC33F devices.
10-bit 1 Msps ADC	16	0	New module on the dsPIC33F devices.
12-bit 200 Ksps ADC	16	0	New module on the dsPIC33F devices.

TABLE 1: KEY DIFFERENCES BETWEEN dsPIC30F AND dsPIC33F DEVICES (CONTINUED)

Peripheral Module	Channels		Comments
	dsPIC30F	dsPIC33F	
10- to 12-bit ADC 10-bit 1.1 Msps 12-bit 500 Ksps	0	32	ADxCON1 SFR: No bit name changes. New modes/SFR bits added: 10/12 ADC mode bit. Added SFR bits to support 32 ADC channels.
UART	2	2	UxMODE SFR: No bit name changes. New modes/ SFR bits added. UxSTA SFR: No bit name changes. New mode/SFR bit added. Features added on dsPIC33F devices: IrDA®, LIN support and Interrupt-on-TSR empty.
I^2C™	1	2	No SFR bit name changes. New SFR (I2CxMSK) and address masking feature added.
SPI	2	2	SPIxSTAT SFR: No bit name changes. SPIxCON1 SFR: No bit name changes. New bits added and some relocated to new SFR SPIxCON2. FIFO and Frame modes added.
DCI (CODEC)	1	1	No SFR bit name changes.
CAN	2	0	N/A
ECAN™ Technology	0	2	New module on dsPIC33F devices.
Motor Control PWM	8	8	No SFR bit name changes.
QEI	1	1	No SFR bit name changes.
I/O Ports	Ports A-G	Ports A-G	New feature added: Open Drain output on some ports.
DMA	0	8	New feature on dsPIC33F devices.
Clock Switching	Yes	Yes	Additional clock modes/features on dsPIC33F devices. Oscillator control SFRs are different.
Power Savings	Yes	Yes	New Doze mode added to existing Sleep and Idle modes.
Device Configuration	—	—	Use new device support files (.h, .inc and .gld) for support.
PLL modes	x4, x8 and x16 PLL	Programmable PLL	See Section 8.1 of the dsPIC33F data sheet (DS70165) for system clock selection information.
Programming Pins	1 pair	3 pairs	There are now 3 PGC/EMUC and PGD/EMUD pairs of pins, which can be used for both programming and debugging.
Debugging Pins	4 pairs	3 pairs	

PERIPHERALS

The dsPIC33F peripheral set is enhanced versus the first generation dsPIC30F product family. Several peripherals have identical features with some peripherals supporting additional features.

The DCI CODEC peripheral on the dsPIC33F devices is identical to the DCI peripheral featured on the dsPIC30F6011A/12A/13A/14A devices.

Note:	If using the DCI peripheral on the "non-A" dsPIC30F devices, the work around called out in the dsPIC30F6011/6012/6013/6014 Rev. B2 errata (DS80198C), specifically item 12, is no longer required.

The ADC module on the dsPIC33F devices is slightly different from the dsPIC30F ADC module. The basic functionality is the same, however the dsPIC33F ADC module is selectable between 10- and 12-bit operation, supporting higher conversion rates and featuring more external ADC pins.

The dsPIC33F devices have 8 channels of DMA, which are assignable to the following peripherals: UART, SPI, ADC, CODEC Interface, Input Capture, Output Compare/Standard PWM and ECAN™ technology.

Additional status bits for determination of specific Math Exception Traps are available on the dsPIC33F devices. These bits are located in the INTCON1 SFR.

dsPIC33F digital I/O ports are 5V tolerant. New open drain features are provided on some ports. dsPIC33F analog pins configured as digital I/O pins are 3.6V tolerant. See the data sheet for further information.

FLASH PROGRAM MEMORY

Like the dsPIC30F devices, the dsPIC33F devices support Run-Time-Self-Programming (RTSP) . Table 2 lists some small RTSP differences between the two families.

TABLE 2: RTSP DIFFERENCES BETWEEN dsPIC33F AND dsPIC30F FAMILIES

Parameter	dsPIC33F	dsPIC30F
Smallest PM Erase Size	1 Page - 512 instructions/1536 bytes	1 Row - 32 instructions/96 bytes
Smallest PM Program Size	1 Row - 64 instructions/192 bytes	1 Row - 32 instructions/96 bytes

Basic PM Erase Code Sequence	`; Setup NVMCON for page erase operation`
	`MOV #0x4042, w0`
	`MOV w0, NVMCON`
	`; Init pointer for Erase Op.`
	`MOV #tblpage(PROG_ADDR), w0`
	`MOV w0, TBLPAG`
	`MOV #tbloffset(PROG_ADDR), w0`
	`TBLWTL w0, [w0]  ; Set base address of erase block`
	`; Disable interrupts, if enabled;`
	`Write the KEY sequence`
	`MOV #0x55, w0`
	`MOV w0, NVMKEY`
	`MOV #0xAA, w0`
	`MOV w0, NVMKEY`
	`; Start the erase operation`
	`BSET NVMCON, #WR`
	`; Insert two NOPs (required)`
	`NOP`
	`NOP`
	`Re-enable interrupts, if needed`
		`; Setup NVMCON for row erase operation`
		`MOV #0x4041, w0`
		`MOV w0, NVMCON`
		`; Init pointer for Erase Op.`
		`MOV #tblpage(PROG_ADDR), w0`
		`MOV w0, NVMADRU`
		`MOV #tbloffset(PROG_ADDR), w0`
		`MOV w0, NVMADR`
		`; Disable interrupts, if enabled`
		`; Write the KEY sequence`
		`MOV #0x55, w0`
		`MOV w0, NVMKEY`
		`MOV #0xAA, w0`
		`MOV w0, NVMKEY`
		`; Start the erase operation`
		`BSET NVMCON, #WR`
		`; Insert two NOPs (required)`
		`NOP`
		`NOP`
		`Re-enable interrupts, if needed`

TABLE 2: RTSP DIFFERENCES BETWEEN dsPIC33F AND dsPIC30F FAMILIES (CONTINUED)

Parameter	dsPIC33F	dsPIC30F

Basic PM Program Code Sequence (Example loading 1 write latch only)	`; Setup the address pointer to program space`
	`MOV #tblpage(PROG_ADDR), w0`
	`; get table page value`
	`MOV w0, TBLPAG ; load TBLPAG register`
	`MOV #tbloffset(PROG_ADDR), w0`
	`; load address LS word`
	`; Load write data into W registers`
	`MOV #PROG_LOW_WORD, w2`
	`MOV #PROG_HI_BYTE, w3`
	`; Perform the table writes to load the latch`
	`TBLWTL w2, [w0]`
	`TBLWTH w3, [w0++]`
		`; Setup the address pointer to program space`
		`MOV #tblpage(PROG_ADDR), w0`
		`; get table page value`
		`MOV w0, TBLPAG ; load TBLPAG register`
		`MOV #tbloffset(PROG_ADDR), w0`
		`; load address LS word`
		`; Load write data into W registers`
		`MOV #PROG_LOW_WORD, w2`
		`MOV #PROG_HI_BYTE, w3`
		`; Perform the table writes to load the latch`
		`TBLWTL w2, [w0]`
		`TBLWTH w3, [w0++]`

SFR registers, NVMADR and NVMADRU, are not available or utilized for programming/erasing operations on dsPIC33F Flash program memory and data EEPROM is not supported. Likewise there is no vector location for the NVM interrupt as there is on the dsPIC30F devices. The interrupt vector location is reserved.

The dsPIC33F Program Flash Erase/Write endurance specifications differ between the dsPIC33F and dsPIC30F families. Please refer to the device data sheet for further information.

All program/erase operations of the dsPIC33F devices are self-timed like the dsPIC30F devices, therefore no additional timer is required to terminate a program/erase operation.

ELECTRICAL CHARACTERISTICS

Operating from 3.0 to 3.6 VDC and rated at 40 MIPS @ 85ºC, the dsPIC33F product family is designed using 0.25 µm process technology. Therefore, the DC and AC Electrical Specifications are different from the dsPIC30F product family. Please refer to the dsPIC33F data sheet (DS70165) for further information.

PACKAGE CONVERSION CONSIDERATIONS

Table 3 presents a summary of the programming/debugging pin differences between the dsPIC30F "A" devices and the dsPIC33F devices.

Check the mechanical/package footprint of a 64-pin TQFP dsPIC30F and a 64-pin TQFP dsPIC33F. Layout PCB to accommodate common 10x10x1 mm package.

Check the mechanical/package footprint of the 80-pin TQFP dsPIC30F and 80-pin TQFP dsPIC33F. Layout PCB to accommodate a common 12x12x1 mm package.

TABLE 3: PROGRAMMING/DEBUGGING PIN DIFFERENCES

Programming/Debugging Pins	dsPIC30F	dsPIC33F	dsPIC30F	dsPIC33F
	64-pin	64-pin	80-pin	80-pin
PGC/EMUC + PGD/EMUD	RB6 + RB7	—	RB1 + RB0	—
EMUC1/EMUD1	RC14 + RC13	—	RC14 + RC13	—
EMUC2/EMUD2	RD0 + RD1	—	RD0 + RD1	—
EMUC3/EMUD3	RF6 + RF3	—	RF6 + RF8	—
PGC1/EMUC1 + PGD1/EMUD1	—	RB6 + RB7	—	RB6 + RB7
PGC2/EMUC2 + PGD2/EMUD2	—	RC14 + RC13	—	RC14 + RC13
PGC3/EMUC3 + PGD3/EMUD3	—	RB1 + RB0	—	RB1 + RB0

Legend: PGC - Primary Programming Clock Pin;
PGD - Primary Programming Data Pin
EMUCx - Debugging Clock Pin (where x = 1, 2 or 3)
EMUDx - Debugging Data Pin (where x = 1, 2 or 3)

PROGRAMMING SUPPORT

No high voltage is required or provided by the MPLAB® ICD 2 or MPLAB PM 3 tools when programming the dsPIC33F devices. The ~12.5 VDC currently supplied by MPLAB ICD 2 or MPLAB PM 3, when programming the dsPIC30F devices, is not required for the dsPIC33F devices.

Note: Possible damage to the $\overline{\text{MCLR}}$ pin will be sustained if more than 5.5 VDC is applied.

DEVELOPMENT TOOLS AND BOARDS

MPLAB IDE, MPLAB C30, MPLAB ICD 2 and MPLAB PM3 tools support the dsPIC33F product family of devices. See Table 4 below for information on tool version support.

TABLE 4: DEVELOPMENT TOOL SUPPORT FOR THE dsPIC33F FAMILY

Development Tools	dsPIC33F
MPLAB® IDE	MPLAB IDE 7.22 or later
MPLAB C30	MPLAB C30 1.33.01 or later with specific language support files
MPLAB ICD 2 Programmer/Debugger	Yes
MPLAB PM3 Device Programmer	Yes
MPLAB ICE 4000	No

The dsPICDEM™ 80-pin Starter Development Board (DM300019) and the Explorer 16 Development Board (DM240001) support the dsPIC33F silicon.

dsPIC33FJ256GP710I/PF based 100-to-80-pin Plug-in-Modules (PIMS), part number MA330012, are used to support the dsPICDEM 80-pin Starter Development Board.

dsPIC33FJ256GP710I/PF based 100-pin Plug-in-Modules (PIMS), part number MA330011, are used to support the Explorer 16 Development Board.

APPLICATION LIBRARIES

All advanced application libraries developed for the dsPIC30F product family support the dsPIC33F product family. Several libraries have been tested and released. Others are scheduled for testing and release.

APPENDIX A: REVISION HISTORY

Revision A (01/2006)

Original version of the document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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