

**ENT-AN1281**  
**Application Note**  
**VSC8504/VSC8552/VSC8572/VSC8574 Transition Design**  
**Guide**

September 2018



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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.0

Revision 1.0 was published in September 2018. It was the first publication of this document.

## 2 VSC8504/VSC8552/VSC8572/VSC8574 Transition Design Guide

This document highlights considerations for transitioning from revision D to revision E of the VSC8504/VSC8552/VSC8572/VSC8574 devices.

### 2.1 Pinout and Marking Changes

There are no pinout changes to consider when migrating from revision D to revision E.

Revision E devices are marked with new ordering part numbers, as listed in the following table.

**Table 1 • Revision D to E Devices**

Current Revision (D)	New Revision (E)
VSC8504XKS-01	VSC8504XKS-02
VSC8504XKS-04	VSC8504XKS-05
VSC8552XKS-01	VSC8552XKS-02
VSC8552XKS-04	VSC8552XKS-05
VSC8572XKS-01	VSC8572XKS-02
VSC8572XKS-04	VSC8572XKS-05
VSC8574XKS-01	VSC8574XKS-02
VSC8574XKS-04	VSC8574XKS-05

### 2.2 Device ID Changes

As a result of the change from revision D to E, an extended device revision identification has been added to revision E silicon at bit 0 of the general purpose register 30G (Ext REV ID). In addition, for revision E of the VSC8572 and VSC8574 devices, register 3 was added in the 1588 PROC register space containing the value 0x21 (VERSION\_CODE) in the revision E silicon. Customers are encouraged to ensure that this change will have no impact on their software.

**Note:** The device revision number in bits 3:0 (REV\_ID) at register 3 is unchanged from revision D in an attempt to maintain software compatibility.

Device revision readback through JTAG will not be able to differentiate between a revision D and E device.

### 2.3 Unified API Software

For the non-1588 devices (VSC8504 and VSC8552), the device is software backwards compatible with existing API stacks.

For the 1588 devices (VSC8572 and VSC8574), the device is software backwards compatible with existing API stacks for applications that do not use the serial timestamp output interface pins. Customers using 1588 with the PHY's serial timestamp output interface should review [1588 SPI Timestamping Design Considerations](#) for more details.

### 2.4 Errata Differences Between Revision D and Revision E

The following sections detail the differences in errata between revision D and revision E devices.

#### 2.4.1 Long Link-Up Times in Forced 100BASE-TX Mode

Although API 4.67.04's new revision E "init script" introduces long link-up times in forced 100BASE-TX mode for revision E only, the resolution is automatically applied when customers use the complete API. Users who attempt to only run the revision E "init script" from API 4.67.04 will lack the additional long link-up times fix and must address it.

API 4.67.04 is fully backwards compatible with revision D as it uses the same “init script” as prior API versions.

The revision E “init script” improves performance to several compliance tests. For this reason, it is not recommended to apply the prior “init script” to the revision E device.

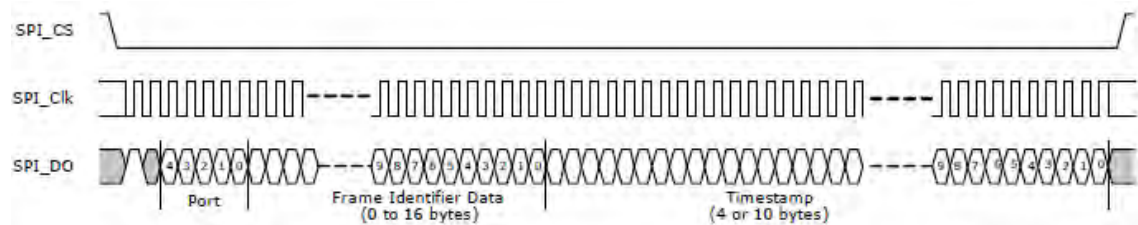
## 2.4.2 1588 Timestamp Out-of-Sync (OOS) FIFOs

Revision E silicon includes a new 1588 processor that eliminates the OOS vulnerability described in [ENT-AN1238 VSC8574 Out-of-Sync \(OOS\) Summary](#). Likewise, recent Unified API releases (starting with version 4.67.03) check for revision E VSC8574 and VSC8572 devices in order to skip the OOS software workaround procedure described in ENT-AN1238. As a result, the customer experience for 1588 applications is far superior with revision E silicon, so it is the recommended revision for all 1588 designs using VSC8574 or VSC8572. For more information about the OOS issue present in revision D, please consult the relevant datasheets in addition to ENT-AN1238.

## 2.4.3 1588 SPI Timestamping Design Considerations

As documented in the VSC8574-02 and VSC8572-02 datasheets, the serial timestamp output interface generates (or pushes) timestamp and frame signature pairs that have been enqueued and packed into timestamp FIFOs to the external chip interface. The external chip interface consists of three output pins: 1588\_SPI\_DO, 1588\_SPI\_CLK, and 1588\_SPI\_CS. These pins are shared by all ports of the VSC8574 and VSC8572 devices. The following illustration shows the output format.

**Figure 1 • VSC8572-02/VSC8574-02 SPI TS/Signal Output**



**Note:** The silicon defaults to generating output bits on the falling edge of the SPI clock, so a SPI receiver implementation will latch the bits at its input pin on the rising edge of the SPI clock.

The VSC8572XKS-02, VSC8572XKS-05, VSC8574XKS-02, and VSC8574XKS-05 devices have an errata concerning clock signal generation on the serial timestamp interface, which is also known as the push-out serial peripheral interface (SPI). The serial timestamp output interface may not generate the final 1588\_SPI\_CLK cycle for certain timestamp push-out transactions. This issue can be worked around by programming the SI\_CLK\_LO\_CYCS within the 1588 register configuration to value 0x1. This workaround was first introduced in PHY API version 4.67.04.

### 2.4.3.1 Failure Mode

As documented in the design considerations of the VSC8574-02 and VSC8572-02 datasheets, the serial timestamp output interface may fail to provide a terminating SPI clock cycle. The failure may appear under two conditions:

- An egress timestamp for a Delay\_Req PTP message (T3) is processed on physical port 1 (and/or port 3 for the VSC8574XKS-02 and VSC8574XKS-05 devices)
- T3 timestamps are concurrently processed on multiple physical ports of a single device

These conditions are typically encountered when all ports of the device are processing PTP traffic. The bug only impacts content on the serial output interface itself—that is, egress timestamps accessed over the 1588 register interface that are stored in the TS FIFO are unaffected.

The terminating SPI clock cycle is lost only when the SI\_CLK\_LO\_CYCS value is programmed to 0x2 or greater, which is usually the case because the hardware default is a 50% duty cycle, 31.25 MHz SPI clock (SI\_CLK\_LO\_CYCS and SI\_CLK\_HI\_CYCS default to 0x2). However, a SI\_CLK\_LO\_CYCS value of 0x1 prevents the final SPI clock cycle from being lost, and so can be exploited as one workaround to this bug.

### 2.4.3.2 Receiver T3 Timestamp Behavior

As a consequence of the SPI clock cycle termination failure, the final bit of a faulty serial timestamp transaction will not be latched at the receiver. The failure phenomenon can be inferred from the following oscilloscope capture.

Figure 2 • SPI Timestamp Error



The timestamp transaction shown utilizes a PTP Delay\_Req message with a known T3 timestamp ending in nibble 0xE (serial output order is MSB→LSB). The scope capture shows the final three rising edges of 1588\_SPI\_CLK (yellow) are all 1s, while the terminating 1588\_SPI\_DO (magenta) transition from 1→0 lacks a corresponding rising edge of 1588\_SPI\_CLK. Instead, the transaction terminates prematurely, which results in the 1588\_SPI\_DO (magenta) returning to value 1.

Depending on the SPI receiver implementation, the timestamp may be merged with bits in the subsequent T3 timestamp or it might never be latched at the receiver. The failure effects can vary due to unpredictable behavior at the SPI receiver, but the PTP Slave will generally not be able to lock with the PTP Master as a result of corrupted Delay\_Req timestamps.

### 2.4.3.3 Application Workarounds

The following sections describe the workarounds for affected device applications.

### 2.4.3.3.1 API-4.67.04 Workaround

API-4.67.04 forcibly configures the 1588 serial timestamp output interface to have a SI\_CLK\_HI\_CYCS of 0x3 and SI\_CLK\_LO\_CYCS of 0x1. In other words, a 31.25 MHz SPI clock with 24 ns high time and 8 ns low time. Other 1588 devices are unaffected.

### 2.4.3.3.2 API-4.67.03 Patch

API code prior to version 4.67.04 can be patched with the following to implement the same functionality on affected devices.

```

/* ***** API 4.67.03 Released CODE ***** */
/* Function: vtss_phy_ts_init() */
/* Approximate Line 16408 of the file vtss_phy_ts_api.c */
/* ***** */
#ifdef VTSS_CHIP_CU_PHY
    if ((phy_type == VTSS_PHY_TYPE_8574) || (phy_type == VTSS_PHY_TYPE_8572)) {
        /* initialize all the 1588 engines: this should be done only once
         i.e. engine initialization should be done through base port or
         alternate port (for 2-channel PHY); otherwise engine config
         for one port might be lost by another port initialization.
         This is reqd for Tesla RevA, RevB fixed in HW.
        */
        if (revision == VTSS_PHY_TESLA_REV_A) {
            if (vtss_state->phy_ts_port_conf[base_port_no].eng_init_done == FALSE) {
                VTSS_D("1588 Analyzer init, port_no %u", port_no);
                if ((rc = VTSS_RC_COLD(vtss_phy_ts_analyzer_init_priv(vtss_state,
                    base_port_no))) != VTSS_RC_OK) {
                    VTSS_E("1588 Analyzer init failed, port_no %u", port_no);
                    break;
                }
                vtss_state->phy_ts_port_conf[base_port_no].eng_init_done = TRUE;
            }
            vtss_state->phy_ts_port_conf[port_no].eng_init_done = TRUE;
        }
    }
    /* ***** Updated API 4.67.04 CODE Changes for Tesla Rev. E follow here ***** */
    /* Tesla Rev E needs these values to be configured with fixed values */
    if (revision >= VTSS_PHY_TESLA_REV_E) {
        VTSS_RC(VTSS_PHY_TS_READ_CSR(port_no, VTSS_PHY_TS_PROC_BLK_ID(0),
            VTSS_PTP_TS_FIFO_SI_TS_FIFO_SI_CFG, &value));
        /* clearing bitfields SI_CLK_HI_CYCS(10:6),SI_CLK_LO_CYCS(5:1) */
        value = VTSS_PHY_TS_CLR_BITS(value, 0x7fe);
        value |= VTSS_F_PTP_TS_FIFO_SI_TS_FIFO_SI_CFG_SI_CLK_HI_CYCS(3);
        value |= VTSS_F_PTP_TS_FIFO_SI_TS_FIFO_SI_CFG_SI_CLK_LO_CYCS(1);
        VTSS_RC(VTSS_PHY_TS_WRITE_CSR(port_no, VTSS_PHY_TS_PROC_BLK_ID(0),
            VTSS_PTP_TS_FIFO_SI_TS_FIFO_SI_CFG, &value));
        VTSS_I("Overwriting Push-SPI config for Tesla E on port %u ,
            CLK_HI_CYCS = 3, CLK_LO_CYCS = 1\n", port_no);
    }
    /* ***** Updated API 4.67.04 CODE Changes for Tesla Rev. E precede here ***** */
    /* Set the PHY latency for Tesla, for 10G it is not reqd */
    if ((rc = vtss_phy_ts_phy_latency_set_priv(vtss_state, port_no)) != VTSS_RC_OK) {
        VTSS_E("1588 PHY Latency config fail!, port_no %u", port_no);
        break;
    }
}
#endif /* VTSS_CHIP_CU_PHY */

```

#### 2.4.3.4 Reconfigurable SPI Receivers in FPGAs

For customer applications that implement the serial timestamp SPI receiver in an FPGA, another workaround option involves programmable logic changes instead of a software workaround.

As indicated previously, the pushed T3 timestamp has nanosecond units. Because these PHYs timestamp with a minimum 4 ns resolution, the least-significant bit of the pushed timestamp is not meaningful for PTP slave timing accuracy. In other words, the least-significant bit of the T3 timestamp can be unconditionally set to a 0 inside the FPGA receiver logic without degrading system accuracy. This way, the SPI receiver could ignore the last bit of every pushed timestamp, whether or not the least significant bit is made available by the serial timestamp interface of the PHY.

This solution works across both revision D and revision E.

## 2.5 Energy-Efficient Ethernet (EEE) Differences Between Revision D and Revision E

Revision E silicon contains several performance improvements related to Energy-Efficient Ethernet (EEE). While an anomalous PCS error indication errata exists in datasheets for both revisions, revision E silicon offers superior performance. However, the level of packet error degradation in revision D EEE mode versus revision E has not been quantified due to interoperability testing limitations. In other words, actual EEE performance on revision D silicon may have more degradation than currently indicated by its EEE errata.



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