TB3222

EEPROM Emulation for Flash-Only Devices

Introduction

When migrating from 8-bit MCUs to 32-bit MCUs, one of the biggest obstacles is the lack of real EEPROM memory in majority of 32-bit MCUs. Several software emulation layers exist to address this issue. However, while providing a seamless emulation of the EEPROM interface, they all have significant drawbacks like excessive wear on the underlying Flash memory and may result in complete data loss in case of power interruption while the write is ongoing.

A better approach is described in this document. This approach requires minor changes to the application flow, but yields a robust EEPROM emulation with minimal wear of the MCU Flash memory.

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1. The Problem

Given the lack of an EEPROM in the majority of modern 32-bit MCUs, the only available location for storing the variable data is the Flash memory.

The disadvantage of the Flash memory is that it cannot be erased or written in single bytes, as is typically done for EEPROM memory. Flash memory can only be erased and written in large blocks. A typical erase block size may be 256 to 8192 bytes, and a typical write block is 64 to 512 bytes. Some Flash implementations support partial writes, a mode where an erased block may be written multiple times as long as bits only changed from “1” (erased state) to “0” (programmed state). Even if the Flash supports partial writes, it often comes with further limitations. In some cases, there is a limit on the number of partial writes that may be performed before an erase is necessary. In other cases, writes must happen in some specific alignment and size combinations.

Additionally, the Flash memory allocated for the data storage is often located in the same Flash array as the application code. This leads to the need to pause the application execution while data is written. The implementation proposed here enables the user to define the point at which this block is going to happen. On the other hand, MCU manufacturers recognize this problem, and in many modern MCUs there is a separate data Flash section available for this use. In some cases, the main Flash array is split into multiple independent banks, which can be written while other banks are available for reading and code execution.

2. The Solution

The proposed solution is to combine all the variables to be stored persistently in a structure along with a few service members. The structure can be mapped to the address in the Flash memory or copied into the SRAM for faster access and possibility of cumulative updates.

The following code shows a typical structure for the data layout. The first part shows the original structure, and the second part shows the layout after two version updates in addition to the original version.

```
---------------------------------------
typedef struct
{
  uint32_t     counter;
  uint8_t      version;
  // User Values
  uint32_t     crc;
} EepromLayout_v1;

typedef struct
{
  uint32_t     counter;
  uint8_t      version;
  // Version 1 User Values
  uint32_t     crc1;
  // Version 2 User Values
  uint32_t     crc2;
  // Version 3 User Values
  uint32_t     crc3;
} EepromLayout_v3;
---------------------------------------
```

The version field identifies the version of the structure. Applications that do not have firmware updates and implement a fixed layout, may omit the version field.

The counter field is a monotonically incrementing counter. Along with CRC field, the highest counter value identifies the recent valid version of the structure. The 32-bit value will never overflow in practice, because the counter is only incremented on writes, and the Flash write endurance is limited.

The size of the structure for CRC calculation may be inferred from the version field, or explicitly defined at part of the structure.

The robustness of this approach comes from allocating the storage for multiple copies of the structure. Multiple copies may be allocated in the same erase block if the Flash supports partial writes, but the care must be taken to allocate at least two erase blocks. At the same time at least two copies must be allocated. This will ensure data protection against damage in case of power interruptions when one of the blocks must be erased.

Allocating multiple copies has an additional benefit of implementing wear leveling at no additional cost.

The size of the data allocated for each copy must be enough to cover the current size of the structure. It must also be big enough to cover possible future extensions with the new versions. Updating the allocation size with the firmware update to a new version is possible but may be complicated.

At the time of the initialization, the application must iterate over all possible copies of the structure. On each iteration it must calculate the CRC of the current copy and compare the counter field to the best candidate so far. The copy with the higher counter and version values and the valid CRC value is the recent valid data that must be loaded into SRAM and used by the application.

If no valid copy is found, the application must initialize all fields to their default value. This can only happen on a freshly programmed device.

The application may detect that the copy is valid, but the version of the structure is lower than currently supported by the application. This will happen on the first boot after the firmware update that changes the layout of the data. In this case parts of the data from the old version should be loaded as is, and the new fields should be initialized to the default values. The version field should be updated to the latest value, after that the structure will be saved in the new version format the next time it is written.

Applications that support firmware updates must support all prior versions of the structure in order to load the data in the old format. If a firmware downgrade is supported, then the application must preserve the layout of the data structure to be compatible with the old versions. This includes keeping and updating the CRC values for all previous versions. If firmware downgrade is not possible, then only one CRC may be used for the recent version of the structure.

If firmware downgrade is supported, then the version field indicates the latest version. After firmware downgrade, the application may see an unsupported version set in the version field. In this case it must assume that the version was set by the recent firmware and use the CRC alone as an indicator for the validity of the data.

When saving the data to the Flash, the index of the next entry to be written is calculated as (C + 1) % N, where C is the index of the current valid entry and N is the total number of entries allocated for the persistent storage.

After a structure is saved, if the new index is pointing to another erase block, the application may choose to erase the next block ahead of time. This will move erase operation to the time of the last write, making the next write much faster.

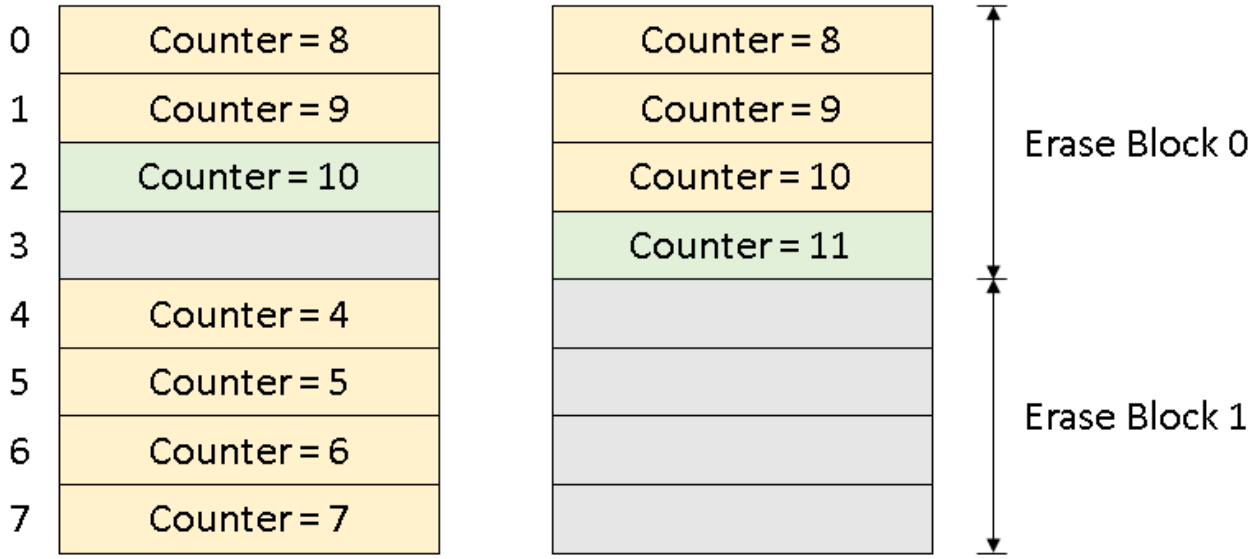
Typically write operation is much faster than erase. Erasing the block ahead of time may give enough time to the application to detect power failure and save the currently unsaved data.

After the initialization, the application cannot assume that the next block was properly erased after the previous write, since it may have been interrupted by the power failure. Application must always perform an erase in this case, even if the Flash appears to be erased.

3. Practical Implementation Considerations

The following figure shows a typical memory layout. In the memory layout, eight copies are allocated, that is, four copies for each erase block. In the first case the entry with the index 2 (Counter = 10) is the recent copy. After the data is updated, the entry with the index 3 (Counter = 11) will be the recent. Simultaneously the erase block ‘1’ is erased, because it will contain the next written entry. All entries are used in a round-robin fashion, ensuring equal wear of the Flash memory.

Figure 3-1. Memory Layout



To limit the number of Flash erase cycles, an actual write must be initiated by the application. This may happen on each field update, or after several fields were updated simultaneously. Additionally, the application may choose to save updated values periodically after a set timeout. Any changes to the data within the same timeout period will be written simultaneously saving Flash erase cycles.

In cases, when EEPROM access is rare and mostly read-only, for example, when EEPROM is used to store calibration data, it may make more sense to access the data directly from the Flash without maintaining a copy in the SRAM. In this case a temporary copy of the data structure must be created in the SRAM every time the data must be saved.

Special care must be taken when the persistent memory is allocated in the separate data section of the device that is accessible for writes while the main Flash is available for the code execution. In this case the code is executed in parallel with the Flash write and erase operations, which minimized the impact of the EEPROM emulation on the code execution. However, the EEPROM emulation code must keep track of the fields that are changed during the ongoing write. The data saving code may either create a copy of the data that is being saved, or block execution of the update operations while Flash access is in progress.

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