
AT13053: Differences between ATtiny4/5/9/10 and ATtiny102/104

APPLICATION NOTE

Introduction

This application note highlights the differences between the existing Atmel® tinyAVR® devices ATtiny4/5/9/10 and ATtiny102/104.

ATtiny102/104 devices are not a drop-in replacement for ATtiny4/5/9/10. However, the functionalities are backward compatible with the existing ATtiny4/5/9/10 functionalities.

For differences in errata, typical characteristics, and electrical characteristics between ATtiny4/5/9/10 and ATtiny102/104, refer to the specific device datasheets.

For more details about the device, refer to the latest version of the ATtiny102/104 datasheet.

Features

- Pin functionality difference
- Code compatibility
- Enhancement and added features
- Package type

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1. Pin Functionality Difference

ATtiny102/104 features additional pins than ATtiny4/5/9/10. ATtiny102/104 has both PORTA and PORTB whereas ATtiny4/5/9/10 have only PORTB.

ATtiny102/104 contains additional GPIOs. ATtiny102 is an 8-pin device with 6 GPIOs. ATtiny104 is a 14-pin device with 12 GPIOs.

Table 1-1. Port Pin Functionality Difference between ATtiny102/104 and ATtiny4/5/9/10

Port pin	ATtiny102/104	ATtiny4/5/9/10
PB[0]	ADC4 / PCINT8	ADC0 / AIN0 / OC0A / PCINT0 / TPIDATA
PB[1]	ADC5 / OC0A / PCINT9 / INT0 / CLKO	ADC1 / AIN1 / CLKI / ICP0 / OC0B / PCINT1 / TPICLK
PB[2]	ADC6 / ICP0 / TxD0 / PCINT10	ADC2 / CLKO / INT0 / PCINT2 / T0
PB[3]	ACO / ADC7 / T0 / RxD0 / PCINT11	ADC3 / PCINT3 / RESET

Note:

- PB [0] PORTB Pin 0 is not present in ATtiny102.
- The code that is built for your existing ATtiny4/5/9/10 will continue to successfully build on the new ATtiny104 device. But, such existing code may not build for ATtiny102 - if the code uses the PORTB Pin 0. To ensure the working of the code, the differences in the pin functionalities must be noted.

2. Enhancement and Added Features

Compared to existing ATtiny4/5/9/10 the following enhancements or additional features are available in ATtiny102/104.

- Self-programming flash
- USART module
- Shorter startup time
- Improved Internal 8MHz RC Oscillator accuracy
- Improved ADC Module
- Bandgap Reference Connected to Analog Comparator
- Additional Pin Change Interrupt

2.1. Self-programming Flash

ATtiny102/104 supports both external programming and internal programming (self-programming). Whereas, the ATtiny4/5/9/10 does not support internal programming (self-programming).

The ATtiny102/104 provides a Self-Programming mechanism where a bootloader can be used to program an application code into the internal flash. Flash Self-programming is supported for the full supply voltage range (1.8 – 5.5V).

The flash in ATtiny104/102 does not support Read-While-Write, and cannot be read during an erase or write operation. Therefore, the CPU will halt during the execution of a write or erase operation. Only WORD_WRITE and PAGE_ERASE commands are supported in self-programming. The CPU can execute Page Erase and Word Write in the NVM code memory section to perform programming operations.

2.2. USART Module

ATtiny102/104 features a dedicated USART module with individual configuration registers. Refer to the **Register Description** section under the USART module in the ATtiny102/104 device datasheet for detailed description of these registers. They also have a separate TX, RX, and XCK pins, refer to the section **I/O Multiplexing** in the ATtiny102/104 device datasheet for details on the pin mapping for this peripheral. This USART module supports Asynchronous as well as Synchronous operation. It also supports serial frames with 5, 6, 7, 8, or 9 data bits and 1 or 2 stop bits.

The Universal Synchronous and Asynchronous Serial Receiver and Transmitter (USART) can be set to a master SPI compliant mode of operation by configuring the **UMSELn1:0** bits in **UCSR0C** register, these bits select the mode of operation of the USART0.

Table 2-1. USART Mode Selection

UMSEL0[1:0]	Mode
00	Asynchronous USART
01	Synchronous USART
10	Reserved
11	Master SPI (MSPIM)

2.3. Shorter Startup Time

ATtiny102/104 supports two selectable startup time options:

1. Normal startup time – 64ms.
2. Shorter startup time – 8ms.

These are not user configurable, but are available on selected CPNs (Customer Part Number). They are available in CPNs starting with ATtiny102F or ATtiny104F.

Table 2-2. Start-Up Times when Using the Internal Calibrated Oscillator with Shorter Start-up Time

Reset	Oscillator	Configuration	Total start-up time
8ms	6 cycles	21 cycles	8ms + 6 oscillator cycles + 21 system clock cycles

2.4. Improved Internal 8MHz RC Oscillator Accuracy

The factory calibration accuracy of internal 8MHz RC oscillator is improved from $\pm 10\%$ in ATtiny4/5/9/10 to $\pm 3\%$ in ATtiny102/104. It is also possible to manually calibrate the internal oscillator to be more accurate than default factory calibration.

Table 2-3. Calibration Accuracy of Internal RC Oscillator

Calibration method	Target frequency	V _{CC}	Temperature	Accuracy at given voltage and temperature
Factory calibration	8.0MHz	2.7 - 4.0V	0°C - 85°C	$\pm 3\%$
User calibration	Fixed frequency within: 7.3 - 8.1MHz	Fixed voltage within: 1.8 - 5.5V	Fixed temp. within: -40°C - 85°C	$\pm 1\%$

2.5. Improved ADC Module

ATtiny102/ATtiny104 features a 10-bit, successive approximation ADC. The ATtiny102/104 ADC module has more number of ADC channels. The differences are highlighted in the following table.

Table 2-4. Number of ADC Channels in ATtiny104/102 and ATtiny5/10

Parameter	ATtiny104	ATtiny102	ATtiny5/10
ADC Channels	8 ADC channels	5 ADC Channels	4 ADC Channels
PORTs for ADC	ADC pins are available on PORTA and PORTB	ADC pins are available on PORTA and PORTB	ADC pins are available only on PORTB

While ATtiny5/10 (ATtiny4/9 does not have ADC) features internal reference voltage of V_{CC}, the ATtiny102/104 have internal reference voltage of nominally 1.1V, 2.2V, and 4.3V. Alternatively, V_{CC} can be used as reference voltage for single ended channels.

ATtiny102/104 has optional left adjustment for ADC result readout. The ADLAR bit in ADCSRB register affects the presentation of the ADC conversion result in the ADC data register. Write one to ADLAR to left

adjust the result. Otherwise, the result is right adjusted. Changing the ADLAR bit affects the ADC Data Register immediately, regardless of any ongoing conversions.

Figure 2-1. ADLAR

ADLAR = 0

Bit	15	14	13	12	11	10	9	8	
0x1A	—	—	—	—	—	—	ADC9	ADC8	ADCH
0x19	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	ADCL
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

ADLAR = 1

Bit	15	14	13	12	11	10	9	8	
0x1A	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADCH
0x19	ADC1	ADC0	—	—	—	—	—	—	ADCL
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

Refer to the **Register Description** section under the ADC module in the ATtiny102/104 device datasheet for detailed description of registers and refer to section **I/O Multiplexing** in the ATtiny102/104 device datasheet for details about the pin mapping for this peripheral.

2.6. Bandgap Reference Connected to Analog Comparator

The Analog Comparator module in ATtiny102/104 has one Internal reference (1.1V – Bandgap) connected to the positive input. For using Bandgap reference voltage as positive input to AC, it is advisable that Bandgap reference is first enabled by writing '1' to ACSRA.ACBG and then selected by writing '1' to ACSRB.ACPMUX. Refer to the **Register Description** section under the AC module in the ATtiny102/104 device datasheet for detailed description of these registers.

2.7. Additional Pin Change Interrupt

ATtiny102/104 has an additional pin change interrupt vector. Two pin change interrupt vectors PCINT0 and PCINT1 are available. Refer to the **Register Description** section under Interrupts to configure these pin change interrupts. Refer to the section **I/O Multiplexing** in the ATtiny104/102 device datasheet for details on the pin mapping for this peripheral.

3. Difference in Package Types

The following table highlights the various packages available for ATtiny104/102 and ATtiny4/5/9/10.

Table 3-1. Package Types Available in ATtiny102/104 and ATtiny4/5/9/10

Device type	Package type	
ATtiny104	14-pin SOIC150	14 Leads - 1.27mm Pitch, 8.65 x 3.90 x 1.60mm Body Size, Plastic Small Outline Package (SOIC)
ATtiny102	8-pin SOIC150	8 Leads - 1.27mm Pitch, 4.9 x 3.90 x 1.60mm Body Size, Plastic Small Outline Package (SOIC)
	8-pad UDFN	8-pad, 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra-Thin Dual Flat No-Lead Package (UDFN)
ATtiny4/5/9/10	6ST1	6 Leads, 2.90 x 1.60mm Plastic Small Outline Package (SOT23)
	8MA4	8-pad, 2 x 2 x 0.6mm Plastic Ultra-Thin Dual Flat No Lead (UDFN)

4. Register Differences

This chapter highlights the differences in registers between ATtiny104/102 and ATtiny4/5/9/10.

4.1. New Registers in ATtiny102/104

This section provides the list of registers available only in ATtiny102/104.

4.1.1. Port A Data Direction Register

Name: DDRA

Offset: 0x01

Reset: 0x00

Property:

Bit	7	6	5	4	3	2	1	0
	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – DDRA_n: Port A Input Pins Address [n = 7:0]

4.1.2. Port A Input Pins Address

Name: PINA

Offset: 0x00

Reset: N/A

Property:

Bit	7	6	5	4	3	2	1	0
	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – PINAn: Port A Input Pins Address [n = 7:0]

4.1.3. Port A Data Register

Name: PORTA

Offset: 0x02

Reset: 0x00

Property:

Bit	7	6	5	4	3	2	1	0
	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PORTAn: Port A Data [n = 7:0]

4.1.4. Port A Pull-up Enable Control Register

Name: PUEA

Offset: 0x03

Reset: 0x00

Property:

Bit	7	6	5	4	3	2	1	0
	PUEA7	PUEA6	PUEA5	PUEA4	PUEA3	PUEA2	PUEA1	PUEA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PUEAn: Port A Input Pins Address [n = 7:0]

4.1.5. USART Baud Rate 0 Register High

Name: UBBR0H

Offset: 0x0A

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	(UBBR0[15:8]) UBBR0H[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – (UBBR0[15:8]) UBBR0H[7:0]: USART Baud Rate 0 High Byte

UBBR0H and UBBR0L are combined into UBBR0. It means UBBR0H[7:0] is UBBR0[15:8]. Refer to UBBR0L.

4.1.6. USART Baud Rate 0 Register Low

Name: UBBR0L

Offset: 0x09

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	(UBBR0[7:0]) UBBR0L[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – (UBBR0[7:0]) UBBR0L[7:0]: USART Baud Rate 0

UBBR0H and UBBR0L are combined into UBBR0. It means UBBR0L[7:0] is UBBR0[7:0]. This is a 12-bit register which contains the USART baud rate. The UBBR0H contains the four most significant bits and the UBBR0L contains the eight least significant bits of the USART baud rate. Ongoing transmissions by the Transmitter and Receiver will be corrupted if the baud rate is changed. Writing UBBR0L will trigger an immediate update of the baud rate prescaler.

4.1.7. USART Control and Status Register 0 A

Name: UCSR0A

Offset: 0x0E

Reset: 0x20

Property: -

Bit	7	6	5	4	3	2	1	0
	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0
Access	R	R/W	R	R	R	R	R/W	R/W
Reset	0	0	1	0	0	0	0	0

Bit 7 – RXC0: USART Receive Complete

This flag bit is set when there are unread data in the receive buffer and cleared when the receive buffer is empty (i.e., does not contain any unread data). If the Receiver is disabled, the receive buffer will be flushed and consequently the RXC0 bit will become zero. The RXC0 Flag can be used to generate a Receive Complete interrupt (see description of the RXCIE0 bit).

Bit 6 – TXC0: USART Transmit Complete

This flag bit is set when the entire frame in the Transmit Shift Register has been shifted out and there are no new data currently present in the transmit buffer (UDR0). The TXC0 Flag bit is automatically cleared when a transmit complete interrupt is executed, or it can be cleared by writing a one to its bit location. The TXC0 Flag can generate a Transmit Complete interrupt (see description of the TXCIE0 bit).

Bit 5 – UDRE0: USART Data Register Empty

The UDRE0 Flag indicates if the transmit buffer (UDR0) is ready to receive new data. If UDRE0 is one, the buffer is empty, and therefore ready to be written. The UDRE0 Flag can generate a Data Register Empty interrupt (see description of the UDRIE0 bit). UDRE0 is set after a reset to indicate that the Transmitter is ready.

Bit 4 – FE0: Frame Error

This bit is set if the next character in the receive buffer had a Frame Error when received. I.e., when the first stop bit of the next character in the receive buffer is zero. This bit is valid until the receive buffer (UDR0) is read. The FEn bit is zero when the stop bit of received data is one. Always set this bit to zero when writing to UCSR0A.

This bit is reserved in Master SPI Mode (MSPIM).

Bit 3 – DOR0: Data OverRun

The Data OverRun (DORn) Flag indicates data loss due to a receiver buffer full condition. A Data OverRun occurs when the receive buffer is full (two characters), a new character is waiting in the Receive Shift Register, and a new start bit is detected.

If this bit is set, one or more serial frames were lost between the last frame read from UDRn, and the next frame read from UDRn. For compatibility with future devices, always write this bit to zero when writing to UCSRnA. This bit is cleared when the frame received was successfully moved from the Shift Register to the receive buffer.

This bit is reserved in Master SPI Mode (MSPIM).

Bit 2 – UPE0: USART Parity Error

This bit is set if the next character in the receive buffer had a Parity Error when received and the Parity Checking was enabled at that point (UPM0 = 1). This bit is valid until the receive buffer (UDR0) is read. Always set this bit to zero when writing to UCSR0A.

This bit is reserved in Master SPI Mode (MSPIM).

Bit 1 – U2X0: Double the USART Transmission Speed

This bit only has effect for the asynchronous operation. Write this bit to zero when using synchronous operation.

Writing this bit to one will reduce the divisor of the baud rate divider from 16 to 8 effectively doubling the transfer rate for asynchronous communication.

This bit is reserved in Master SPI Mode (MSPIM).

Bit 0 – MPCM0: Multi-processor Communication Mode

This bit enables the Multi-processor Communication mode. When the MPCMn bit is written to one, all the incoming frames received by the USART Receiver that do not contain address information will be ignored. The Transmitter is unaffected by the MPCM0 setting.

This bit is reserved in Master SPI Mode (MSPIM).

4.1.8. USART Control and Status Register 0 B

Name: UCSR0B
Offset: 0x0D
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – RXCIE0: RX Complete Interrupt Enable 0

Writing this bit to one enables interrupt on the RXC0 Flag. A USART Receive Complete interrupt will be generated only if the RXCIE0 bit is written to one, the Global Interrupt Flag in SREG is written to one and the RXC0 bit in UCSR0A is set.

Bit 6 – TXCIE0: TX Complete Interrupt Enable 0

Writing this bit to one enables interrupt on the TXC0 Flag. A USART Transmit Complete interrupt will be generated only if the TXCIE0 bit is written to one, the Global Interrupt Flag in SREG is written to one and the TXC0 bit in UCSR0A is set.

Bit 5 – UDRIE0: USART Data Register Empty Interrupt Enable 0

Writing this bit to one enables interrupt on the UDRE0 Flag. A Data Register Empty interrupt will be generated only if the UDRIE0 bit is written to one, the Global Interrupt Flag in SREG is written to one and the UDRE0 bit in UCSR0A is set.

Bit 4 – RXEN0: Receiver Enable 0

Writing this bit to one enables the USART Receiver. The Receiver will override normal port operation for the Rx/Dn pin when enabled. Disabling the Receiver will flush the receive buffer invalidating the FE0, DOR0, and UPE0 Flags.

Bit 3 – TXEN0: Transmitter Enable 0

Writing this bit to one enables the USART Transmitter. The Transmitter will override normal port operation for the Tx/D0 pin when enabled. The disabling of the Transmitter (writing TXEN0 to zero) will not become effective until ongoing and pending transmissions are completed, i.e., when the Transmit Shift Register and Transmit Buffer Register do not contain data to be transmitted. When disabled, the Transmitter will no longer override the Tx/D0 port.

Bit 2 – UCSZ02: Character Size 0

The UCSZ02 bits combined with the UCSZ0[1:0] bit in UCSR0C sets the number of data bits (Character Size) in a frame the Receiver and Transmitter use.

This bit is reserved in Master SPI Mode (MSPIM).

Bit 1 – RXB80: Receive Data Bit 8 0

RXB80 is the ninth data bit of the received character when operating with serial frames with nine data bits. Must be read before reading the low bits from UDR0.

This bit is reserved in Master SPI Mode (MSPIM).

Bit 0 – TXB80: Transmit Data Bit 8 0

TXB80 is the ninth data bit in the character to be transmitted when operating with serial frames with nine data bits. Must be written before writing the low bits to UDR0.

This bit is reserved in Master SPI Mode (MSPIM).

4.1.9. USART Control and Status Register 0 C

Name: UCSR0C

Offset: 0x0C

Reset: 0x06

Property: -

Bit	7	6	5	4	3	2	1	0
	UMSEL01	UMSEL00	UPM01	UPM00	USBS0	UCSZ01 / UDORD0	UCSZ00 / UCPHA0	UCPOL0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	0

Bits 7:6 – UMSEL0n: USART Mode Select 0 n [n = 1:0]

These bits select the mode of operation of the USART0

Table 4-1. USART Mode Selection

UMSEL0[1:0]	Mode
00	Asynchronous USART
01	Synchronous USART
10	Reserved
11	Master SPI (MSPIM) ⁽¹⁾

Note:

1. The UDORD0, UCPHA0, and UCPOL0 can be set in the same write operation where the MSPIM is enabled.

Bits 5:4 – UPM0n: USART Parity Mode 0 n [n = 1:0]

These bits enable and set type of parity generation and check. If enabled, the Transmitter will automatically generate and send the parity of the transmitted data bits within each frame. The Receiver will generate a parity value for the incoming data and compare it to the UPM0 setting. If a mismatch is detected, the UPE0 Flag in UCSR0A will be set.

Table 4-2. USART Mode Selection

UPM0[1:0]	ParityMode
00	Disabled
01	Reserved
10	Enabled, Even Parity
11	Enabled, Odd Parity

These bits are reserved in Master SPI Mode (MSPIM).

Bit 3 – USBS0: USART Stop Bit Select 0

This bit selects the number of stop bits to be inserted by the Transmitter. The Receiver ignores this setting.

Table 4-3. Stop Bit Settings

USBS0	Stop Bit(s)
0	1-bit
1	2-bit

This bit is reserved in Master SPI Mode (MSPIM).

Bit 2 – UCSZ01 / UDORD0: USART Character Size / Data Order

UCSZ0[1:0]: USART Modes: The UCSZ0[1:0] bits combined with the UCSZ02 bit in UCSR0B sets the number of data bits (Character Size) in a frame the Receiver and Transmitter use.

Table 4-4. Character Size Settings

UCSZ0[2:0]	Character Size
000	5-bit
001	6-bit
010	7-bit
011	8-bit
100	Reserved
101	Reserved
110	Reserved
111	9-bit

UDPRD0: Master SPI Mode: When set to one the LSB of the data word is transmitted first. When set to zero the MSB of the data word is transmitted first. Refer to the *USART in SPI Mode - Frame Formats* for details.

Bit 1 – UCSZ00 / UCPHA0: USART Character Size / Clock Phase

UCSZ00: USART Modes: Refer to UCSZ01.

UCPHA0: Master SPI Mode: The UCPHA0 bit setting determine if data is sampled on the leading edge (first) or trailing (last) edge of XCK0. Refer to the *SPI Data Modes and Timing* for details.

Bit 0 – UCPOL0: Clock Polarity 0

USART0 Modes: This bit is used for synchronous mode only. Write this bit to zero when asynchronous mode is used. The UCPOL0 bit sets the relationship between data output change and data input sample, and the synchronous clock (XCK0).

Table 4-5. USART Clock Polarity Settings

UCPOL0	Transmitted Data Changed (Output of TxD0 Pin)	Received Data Sampled (Input on RxD0 Pin)
0	Rising XCK0 Edge	Falling XCK0 Edge
1	Falling XCK0 Edge	Rising XCK0 Edge

Master SPI Mode: The UC POL0 bit sets the polarity of the XCK0 clock. The combination of the UC POL0 and UC PHA0 bit settings determine the timing of the data transfer. Refer to the *SPI Data Modes and Timing* for details.

4.1.10. USART Control and Status Register 0 D

This register is not used in Master SPI Mode (UMSEL0[1:0] = 11)

Name: UCSR0D

Offset: 0x0B

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	RXIE	RXS						
Access	R/W	R/W						
Reset	0	0						

Bit 7 – RXIE: USART RX Start Interrupt Enable

Writing this bit to one enables the interrupt on the RXS flag. In sleep modes this bit enables start frame detector that can wake up the MCU when a start condition is detected on the RxD line. The USART RX Start Interrupt is generated only, if the RXSIE bit, the Global Interrupt flag, and RXS are set.

Bit 6 – RXS: USART RX Start

The RXS flag is set when a start condition is detected on the RxD line. If the RXSIE bit and the Global Interrupt Enable flag are set, an RX Start Interrupt will be generated when the flag is set. The flag can only be cleared by writing a logical one on the RXS bit location.

If the start frame detector is enabled (RXSIE = 1) and the Global Interrupt Enable flag is set, the RX Start Interrupt will wake up the MCU from all sleep modes.

4.1.11. USART I/O Data Register 0

The USART Transmit Data Buffer Register and USART Receive Data Buffer Registers share the same I/O address referred to as USART Data Register or UDR0. The Transmit Data Buffer Register (TXB) will be the destination for data written to the UDR0 Register location. Reading the UDR0 Register location will return the contents of the Receive Data Buffer Register (RXB).

For 5-, 6-, or 7-bit characters the upper unused bits will be ignored by the Transmitter and set to zero by the Receiver.

The transmit buffer can only be written when the UDRE0 Flag in the UCSR0A Register is set. Data written to UDR0 when the UDRE0 Flag is not set, will be ignored by the USART Transmitter. When data is written to the transmit buffer, and the Transmitter is enabled, the Transmitter will load the data into the Transmit Shift Register when the Shift Register is empty. Then the data will be serially transmitted on the TxD0 pin.

The receive buffer consists of a two level FIFO. The FIFO will change its state whenever the receive buffer is accessed. Due to this behavior of the receive buffer, do not use Read-Modify-Write instructions (SBI and CBI) on this location. Be careful when using bit test instructions (SBIC and SBIS), since these also will change the state of the FIFO.

Name: UDR0

Offset: 0x08

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	TXB / RXB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TXB / RXB[7:0]: USART Transmit / Receive Data Buffer

4.2. Registers in ATtiny102/104 with Bit Differences

This sections provides the list of registers in both ATtiny4/5/9/10 and ATtiny102/104 with difference in bits.

4.2.1. Digital Input Disable Register 0

When the respective bits are written to logic one, the digital input buffer on the corresponding ADC pin is disabled. The corresponding PIN Register bit will always read as zero when this bit is set. When an analog signal is applied to the ADC[7:0] pin and the digital input from this pin is not needed, this bit should be written logic one to reduce power consumption in the digital input buffer.

Name: DIDR0

Offset: 0x17

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
					ADC3D	ADC2D	ADC1D	ADC0D
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – ADC3D: ADC3 Digital Input Disable

Not apply for AC.

Bit 2 – ADC2D: ADC2 Digital Input Disable

Not apply for AC.

Bit 1 – ADC1D: ADC1 Digital Input Disable

When this bit is written logic one, the digital input buffer on the corresponding ADC pin is disabled. The corresponding PIN register bit will always read as zero when this bit is set. When an analog signal is applied to the ADC[7:0] pin and the digital input from this pin is not needed, this bit should be written logic one to reduce power consumption in the digital input buffer.

Bit 0 – ADC0D: ADC0 Digital Input Disable

When this bit is written logic one, the digital input buffer on the corresponding ADC pin is disabled. The corresponding PIN register bit will always read as zero when this bit is set. When an analog signal is applied to the ADC[7:0] pin and the digital input from this pin is not needed, this bit should be written logic one to reduce power consumption in the digital input buffer.

4.2.2. ADC Data Register High Byte (ADLAR=1)

Name: ADCL

Offset: 0x19

Reset: 0x00

Property:

Bit	7	6	5	4	3	2	1	0
	ADC1	ADC0						
Access	R	R						
Reset	0	0						

Bits 6, 7 – ADC0, ADC1: ADC Conversion Result

Refer to ADCH register.

4.2.3. ADC Conversion Result Low Byte (ADLAR=1)

When an ADC conversion is complete, the result is found in the ADCL and ADCH registers.

Name: ADCH

Offset: 0x1A

Reset: 0x00

Property:

Bit	7	6	5	4	3	2	1	0
	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – ADC2, ADC3, ADC4, ADC5, ADC6, ADC7, ADC8, ADC9: ADC Conversion Result

These bits represent the result from the conversion.

4.2.4. Digital Input Disable Register 0

Name: DIDR0

Offset: 0x17

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
					ADC3D	ADC2D	ADC1D	ADC0D
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – ADC3D: ADC3 Digital Input Disable

Not apply for AC.

Bit 2 – ADC2D: ADC2 Digital Input Disable

Not apply for AC.

Bit 1 – ADC1D: ADC1 Digital Input Disable

When this bit is set, the digital input buffer on pin AIN1 (ADC1) / AIN0 (ADC0) is disabled and the corresponding PIN register bit will read as zero. When used as an analog input but not required as a digital input the power consumption in the digital input buffer can be reduced by writing this bit to logic one.

Bit 0 – ADC0D: ADC0 Digital Input Disable

When this bit is set, the digital input buffer on pin AIN1 (ADC1) / AIN0 (ADC0) is disabled and the corresponding PIN register bit will read as zero. When used as an analog input but not required as a digital input the power consumption in the digital input buffer can be reduced by writing this bit to logic one.

4.2.5. Pin Change Interrupt Control Register

Name: PCICR

Offset: 0x12

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
								PCIE0
Access								R/W
Reset								0

Bit 0 – PCIE0: Pin Change Interrupt Enable 0

When the PCIE0 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), pin change interrupt 0 is enabled. Any change on any enabled PCINT[7:0] pin will cause an interrupt. The corresponding interrupt of Pin Change Interrupt Request is executed from the PCIE0 Interrupt Vector. PCINT[7:0] pins are enabled individually by the PCMSK Register.

4.2.6. Pin Change Interrupt Flag Register

Name: PCIFR

Offset: 0x11

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
								PCIF0
Access								R/W
Reset								0

Bit 0 – PCIF0: Pin Change Interrupt Flag 0

When a logic change on any PCINT[7:0] pin triggers an interrupt request, PCIF0 becomes set (one). If the I-bit in SREG and the PCIE0 bit in PCICR are set (one), the MCU will jump to the corresponding Interrupt Vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical one to it.

4.2.7. Pin Change Mask Register 0

Name: PCMSK0

Offset: 0x0F

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PCINTn: Pin Change Enable Mask [n = 7:0]

Each PCINT[7:0] bit selects whether pin change interrupt is enabled on the corresponding I/O pin. If PCINT[7:0] is set and the PCIE0 bit in PCICR is set, pin change interrupt is enabled on the corresponding I/O pin. If PCINT[7:0] is cleared, pin change interrupt on the corresponding I/O pin is disabled.

4.2.8. Pin Change Mask Register 1

Name: PCMSK1

Offset: 0x10

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
					PCINT11	PCINT10	PCINT9	PCINT8
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 0, 1, 2, 3 – PCINT8, PCINT9, PCINT10, PCINT11: Pin Change Enable Mask [11:8]

Each PCINT[11:8]-bit selects whether pin change interrupt is enabled on the corresponding I/O pin. If PCINT[11:8] is set and the PCICR.PCIE1 is set, pin change interrupt is enabled on the corresponding I/O pin. If PCINT[11:8] is cleared, pin change interrupt on the corresponding I/O pin is disabled.

4.2.9. Port Control Register

Name: PORTCR

Offset: 0x16

Reset: N/A

Property:

Bit	7	6	5	4	3	2	1	0
							BBMB	BBMA
Access							R/W	R/W
Reset							0	0

Bit 1 – BBMB: Break-Before-Make Mode Enable

When this bit is set the Break-Before-Make mode is activated for the entire Port B. The intermediate tri-state cycle is then inserted when writing DDRxn to make an output.

Bit 0 – BBMA: Break-Before-Make Mode Enable

When this bit is set the Break-Before-Make mode is activated for the entire Port A. The intermediate tri-state cycle is then inserted when writing DDRxn to make an output.

5. Revision History

Doc. Rev.	Date	Comments
42676A	02/2016	Initial document release

