APPLICATION NOTE

Atmel AT01617: Using the FAULT Timer/Counter Extension

Atmel AVR XMEGA E

Features

- Extension between the outputs of one timer/counter and WeX waveform inputs
- Synchronous or asynchronous waveforms retriggering
- Event controlled
- Multiple FAULT retriggering inputs
- Two FAULT types:
  - Non-recoverable FAULTs
    - Outputs are forced to a configurable safe state
  - Recoverable FAULTs
    - Outputs are retriggered according to three modes

Introduction

This application note describes the various functions of the FAULT Extension to the Timer/Counter available on the Atmel® XMEGA® E.

This extension provides a hardware control of switching applications.

Benefits of FAULT extensions that PWM signals used, for instance in PFC, Lighting or Motor Control do not require a software retriggering according to conditions inputs. The FAULT control is done by hardware and, so, also operates in Sleep mode.

This application note details also the differences and improvements according to Timer/Counters of the Atmel XMEGA A/B/C/D series (see the AVR®1311: Using the XMEGA Timer/Counter Extensions application note for the XMEGA A/B/C/D series).

Software examples are provided in ASF (Atmel Software Framework). These code examples simplify the use of FAULT modes in typical applications.

Table of Contents

1. Glossary

ASF	Atmel Software Framework
Atmel Studio	Integrated Development Environment (IDE) for Atmel AVR applications
SMPS	Switching Mode Power Supply

2. Pre-requisites

The solutions discussed in this document require basic familiarity with the following skills and technologies.

2.1 Documentation

- Atmel XMEGA E manual
- Atmel XMEGA 32E5 datasheet
- Atmel AT01616: XMEGA E Using the WEX application note
- Atmel AVR1311: Using the XMEGA Timer/Counter Extensions application note

2.2 Tools

- Atmel STK®600 Starter Kit
- Atmel XMEGA-E5 Xplained board
- Atmel Studio 6
- Atmel JTAGICE3 debugger

3. FAULT Overview

In XMEGA E, FAULT module is a specific extension to Timer/Counter and is linked to outputs of some Timer/Counters (see Figure 3-1). This extension is placed between the Timer/Counter and WeX extension. FAULT input signals are Timer/Counter Compare outputs and FAULT outputs are the WeX extension inputs (see also Atmel AVR1330: XMEGA E Using the WeX application note).

The only difference between TC4 and TC5 is that TC4 has four Compare outputs whereas TC5 has only two. Figure 3-1 shows that FAULT inputs are Compare A and B outputs. FAULT module has same action on TC4 and TC5.

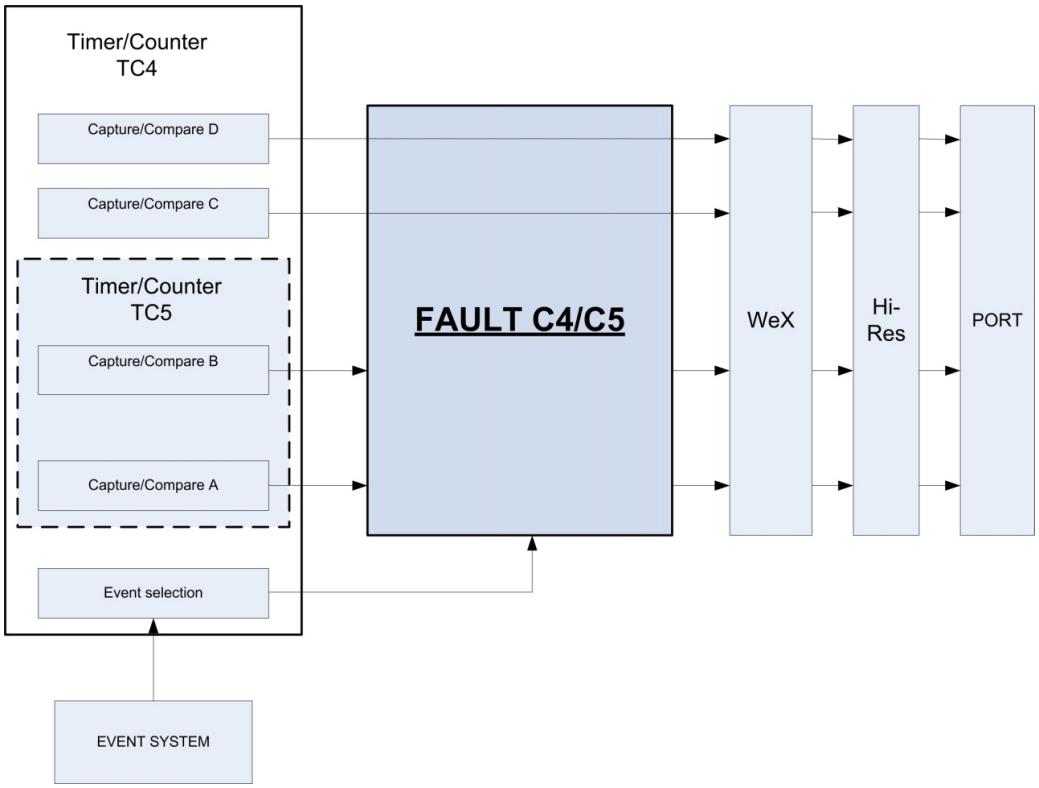
The FAULT extension enables event controlled FAULT protection by acting directly on the waveforms generated from Timer/Counter compare outputs. It can be used to trigger two types of FAULTs with corresponding actions:

- Non-recoverable FAULTs on all Timer/Counter compare outputs, named “FAULT E”
  - It forces the compare outputs to a safe, pre-configured value that is safe for the application. This is typically used for instant and predictable shut-down and disabling of high current or voltage drives
- Recoverable FAULTs on Timer/Counter compare outputs A and B, named “FAULT A” and ”FAULT B”
  - It restarts, halts the timer/counter period, or shortens the output pulse active time or period by clearing the output compare level. This action can be achieved for a certain time, or as long as the FAULT condition is present. This can typically be used for current sensing regulation, zero crossing retriggering, demagnetization retriggering

The FAULT extension reuses event channels from its Timer/Counter, enabling some of them to trigger a FAULT condition.

Important: The FAULT inputs events are the first three input events channels of Timer/Counter.

Figure 3-1. 16-bit timer/counter and closely related peripherals.

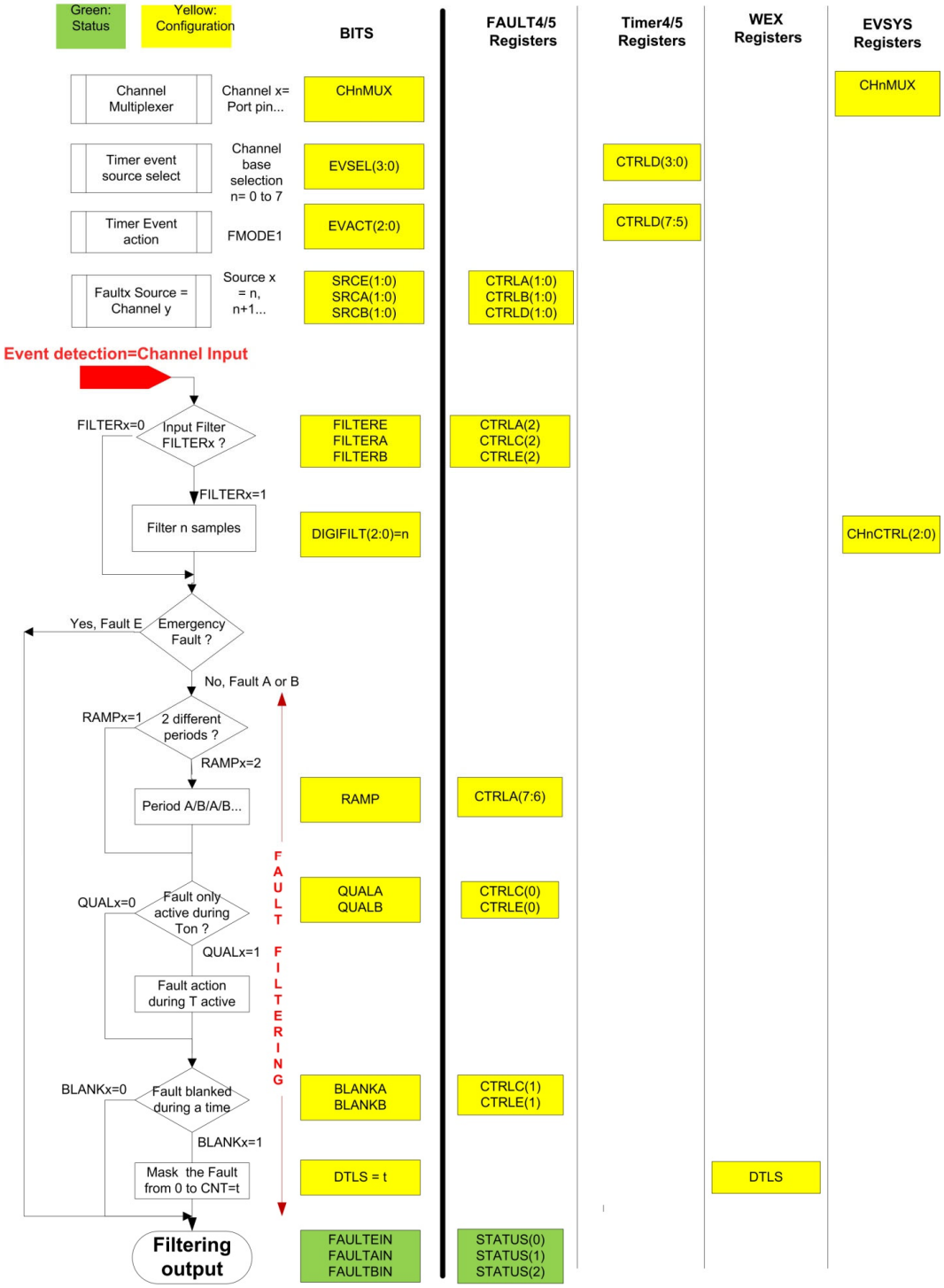


4. FAULT Inputs

In the following sections we will compare the Atmel XMEGA E series to the Atmel XMEGA A/B/C/D series in regards to the FAULT inputs parameters.

Along the descriptions in following sections, refer to Figure 4-1 which describes the FAULT inputs flowchart with the corresponding involved registers.

Figure 4-1. FAULT inputs flowchart and involved bits/registers.



4.2 FAULT input event types

4.2.1 XMEGA A/B/C/D

FAULT inputs are event channels which can be configured with any of the event sources available in the product. All these event sources will have the same action on Timer/Counter outputs (actions are not specific to the Event channel source).

4.2.2 XMEGA E

In XMEGA E FAULT inputs are the Timer/Counter event channels. What is new is that the two FAULT types can be selected among the following sources:

- Non-recoverable FAULT (SRCE):

  This FAULT is named FAULT E and will force the Compare outputs to a pre-configured value. This pre-configured level can be configured with bit FUSE (CTRLA.3) and values in FUSEBYTE6 (see Memory section).

  A non-recoverable FAULT example is, for instance, over-current detection in a Motor Control system. System protection requires that inputs (i.e. external analog comparators) can turn off, asynchronously and with the minimum delay, PWM outputs through a combinary path (independent of system clock).This detection requires an immediate and unconditional action to stop the system.

  Sections 4.3, 4.6, and 4.7 of this document are not relevant to this non-recoverable input.

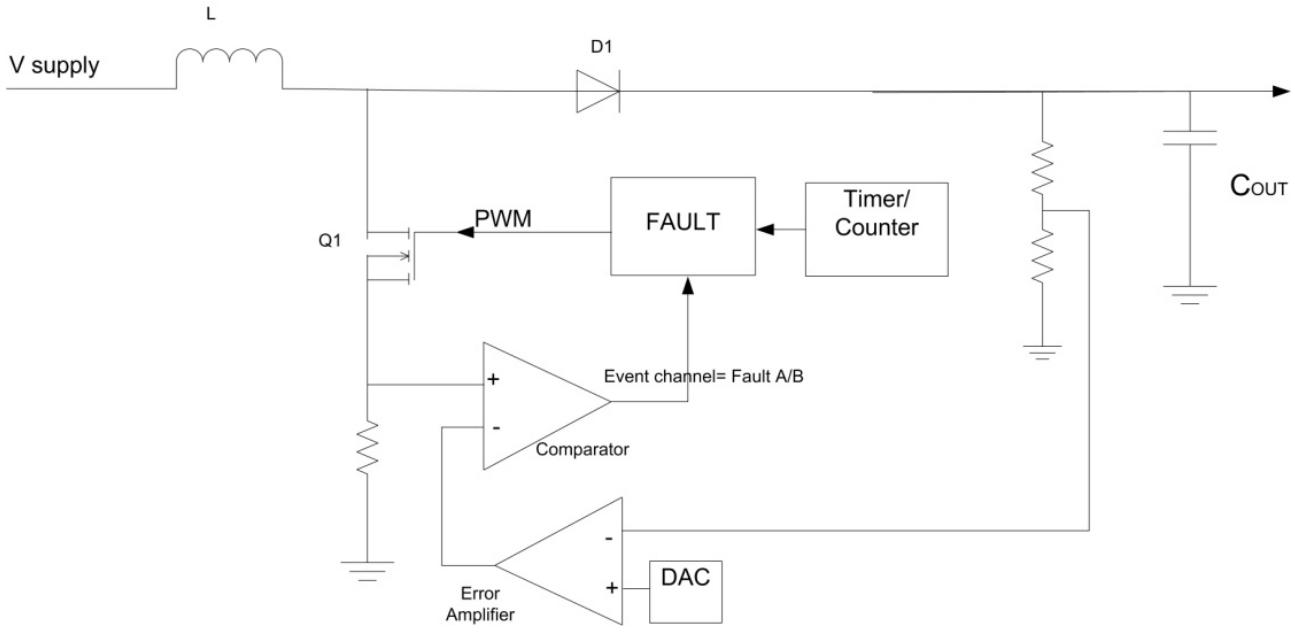
- Recoverable FAULTs (SRCA/SRCB):

  These FAULTs (named FAULT A and FAULT B), provide the ways to retrigger, stop, or halt the waveform outputs. These FAULTs will also force the PWM outputs to inactive level during the time they are present.

  Retriggering is useful for SMPS converters control. Some examples using these input types are PFC, DC/DC converters (i.e. to control the current in converters inductors).

  A basic Boost DC/DC converter system is shown in Figure 4-2. To step-up the voltage, it drives the Q1 transistor with a high-speed PWM signal.

Figure 4-2. Boost DC/DC system.



During the On-state of Q1, the current is flowing through the inductor L and energy is stored in the inductor.

The load is powered from the capacitor C_{OUT}.

During the Off-state, the inductor voltage adds to the source voltage V_{SUPPLY} and the current flows through the diode D1 and recharges the capacitor C_{OUT}.

The output voltage is controlled by varying the duty cycle of the switching. The regulation loop is done, in this example, in current control mode. It is made of:

- An Error amplifier, which provides the voltage error between the voltage output and the setpoint defined by the DAC. This voltage error is the setpoint of the current regulation
- A Comparator, which compares the voltage error (current setpoint) with the current monitored in the shunt resistor. Comparator output is configured as an Event channel
- A Fault feature, which uses the Timer/Counter Event selection to use the Analog comparator output as a Fault input (FAULTA or FAULTB). The PWM output connected to Q1 will be forced inactive as soon as the Comparator output signals the output voltage has reached correct level

4.3 FAULT input event cycles

4.3.1 XMEGA A/B/C/D

There is no difference between two consecutive Timer/Counter cycles. FAULTs have an action (if enabled) during all the Timer/Counter cycles.

4.3.2 XMEGA E

A new Timer/Counter mode provides a way to have two interleaved cycles. In the first cycle only the FAULT A input will have any effect, in the second cycle only the FAULT B input will have any effect. The FAULT mode from one cycle will be propagating to the next cycle if the LINK mode is enabled. This mode is selected if RAMP[1:0] of CTRLA register is set to 10 (RAMP2 mode).

This function is not relevant for FAULT E.

4.4 FAULT input source selection

4.4.1 XMEGA A/B/C/D

FAULT inputs are event channels which can be configured with any of the event sources available in the product. All these event sources will have the same action on Timer/Counter outputs (actions are not specific to the Event channel source).

4.4.2 XMEGA E

The Fault source FAULTE can be selected among the three event channels following the channel selected by the Timer/Counter: n, n+1, n+2.This selection is done with SRCE bits in CTRLA of the FAULT module.

The Fault sources FAULTA, FAULTB can be selected among the two event channels following the channel selected by the Timer/Counter: n, n+1. There is a third possible selection available controlled by SRCA/SRCB[1:0] bits in CTRLB/CTRLD Registers. This third selection, which is only available for recoverable Faults, is named the LINK mode.

For Fault A, the input source is linked to the Fault B state at the end of the previous cycle. It means that if Fault B state was 1 at the end of previous cycle, it will force Fault A state to 1 in next cycle.

For Fault B, the input source is linked to the Fault A state at the end of the previous cycle. It means that if Fault A state was 1 at the end of previous cycle, it will force Fault B state to 1 in following cycle.

4.5 FAULT input event timing

4.5.1 XMEGA A/B/C/D

Event system is synchronous and will require a two CPU cycles maximum time between the Event occurrence and the Event process.

4.5.2 XMEGA E

To avoid any delay in the FAULT path, the Event System has been improved to provide an asynchronous routing. Another advantage is that the FAULT action occurs even if the system clock is stopped. The synchronous mode of the Event system can still be used with FILTERE/FILTERA/FILTERB bits in CTRLA/CTRLC/CTRLE register.

In the default configuration, the FAULT feature uses the Event system in asynchronous mode.

4.6 FAULT input event filtering

4.6.1 XMEGA A/B/C/D

There are no filtering capabilities in these XMEGA products.

4.6.2 XMEGA E

To avoid false FAULT detections on external events (i.e. a glitch on I/O port) digital filtering can be enabled on the event channel. This mode is configured with FILTERE/FILTERA/FILTERB bits in CTRLA/CTRLC/CTRLE registers (according to the three different FAULT inputs.

If FILTERE/FILTERA/FILTERB configuration is selected, the event routing will no more be asynchronous but become synchronous as in XMEGA A/B/C/D. Then the event action will be delayed between two and three peripheral clock cycles + the filtering time. This also requires a running system clock.

4.7 FAULT input event qualification

4.7.1 XMEGA A/B/C/D

There is no way to mask the FAULT inputs versus the status of the PWM output.

4.7.2 XMEGA E

In XMEGA E, it is possible to take into account, or not, the FAULT input if it occurs during the inactive state of the output. If QUALA or QUALB bits (Fault qualification bits of CTRLC/CTRLE registers) are set, and if the corresponding FAULT input occurs during the time the output is inactive, there will not be any action of the FAULT module. FAULT action only occurs when PWM output is active.

There is no qualification option for FAULT E.

Figure 6-5 provides an example with QUAL input mode and KEEP/HALT action modes.

4.8 FAULT input event blanking

4.8.1 XMEGA A/B/C/D

There is no blanking option in these XMEGA A/B/C/D products.

4.8.2 XMEGA E

In XMEGA E, the FAULT input can be masked during a configurable time from the start of Timer/Counter cycles. If BLANKA or BLANKB bit (Blanking bits of CTRLC/CTRLE registers) is set, the corresponding FAULT input will be masked during the time configured in, DTLS for channel A and DLHS for Channel B for TC4/TC5 respectively.

This function is not relevant for FAULT E.

Figure 6-3 provides an example with BLANK input mode and KEEP action mode.

For example, if the Peripheral clock frequency is 32MHz, the Blanking time can be programmed between 0 and a maximum value equal to 256 Peripheral clock periods = 256 / 32 = 8µs.

This mode can be used, for instance, to mask spikes due to transistors switching.

4.9 Software FAULT

4.9.1 XMEGA A/B/C/D

It is not possible to force a Software FAULT input.

4.9.2 XMEGA E

In XMEGA E, the firmware can produce a FAULT which action will be executed by the Hardware FAULT module. This Software FAULT is activated if bits FAULTBSW, FAULTASW, or FAULTESW (Software Fault bits of CTRLGSET register) are set to 1.

In Figure 6-1 the Software FAULT is combined in an OR function with the output of hardware fault filtering functions of previous Flowchart (Figure 4-1).

5. FAULT Outputs

In the following sections we will compare the Atmel XMEGA E series to the Atmel XMEGA A/B/C/D series according to the FAULT outputs.

5.1 Event and interrupt outputs

5.1.1 XMEGA A/B/C/D

The FAULT requires the Peripheral Clock to run, and there are maximum two peripheral clock cycles until the event triggers the FAULT action.

When a FAULT is detected the FAULT Detection Flag is set, the Timer/Counter's Error Interrupt Flag is set and the optional interrupt is generated.

5.1.2 XMEGA E

Since the new Event system supports both asynchronous and synchronous event routing, it ensures predictable and instant FAULT reaction for a wide selection of FAULT triggers.

The default FAULT configuration is asynchronous, enabling immediate asynchronous action on waveform output even if the system clocks are stopped.

5.2 Outputs levels

5.2.1 XMEGA A/B/C/D

Two different FAULT actions can be selected:

- The disable of Timer/Counter outputs. If Output Override Enable register (OUTOVEN) is set, the output will be set by the port pin configuration
- The Direction Clear action (clear the DIR Direction register) in the associated port. The result is that all port pins are in tri-state input mode

5.2.2 XMEGA E

The different FAULT actions are:

1. Recoverable FAULTs (if enabled):
   Force the Timer/Counter outputs to inactive level during the time the FAULT is present. (Inactive level is configured with POLA/POLB/POLC/POLD bit(Output polarity bits of TC45 CTRLC register).
2. Non-recoverable FAULTs:
   If FUSE bit is set (CTRLA Bit3), the pre-configured value of Compare outputs are set to pre-configured values programmed in FUSEBYTE6 (see Memory section). If FUSE bit is cleared, the pre-configured values of Compare outputs are set according to the port configuration.

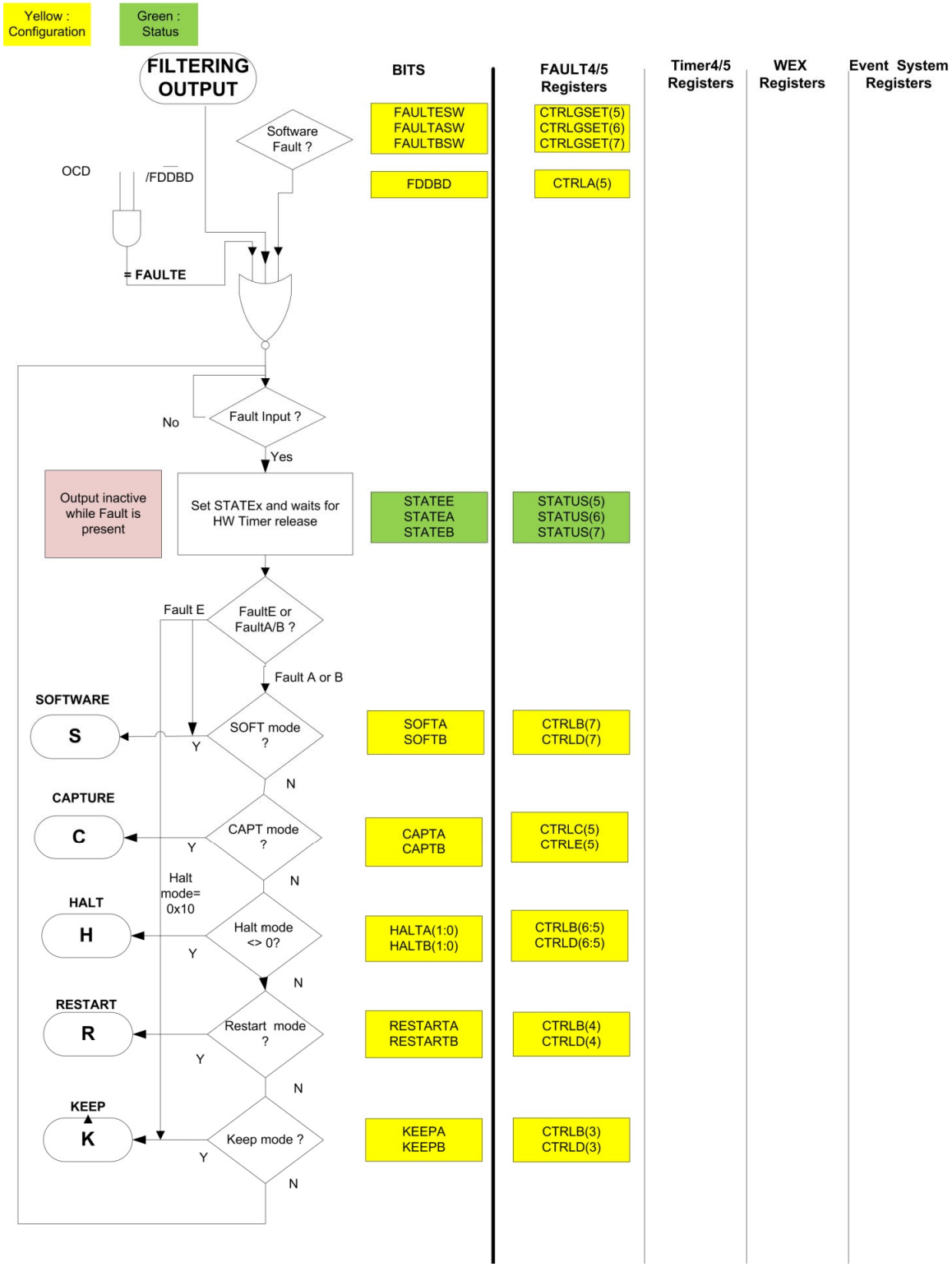
In the second case, users can configure the inactive levels to their application constraints.

FUSEBYTE6 provides also the configuration of PWM outputs during the Timer initialization. These configuration Fuses control the default levels from Reset output until Timer control operates.

6. FAULT Action Modes

In the following sections we will compare the Atmel XMEGA E series to the Atmel XMEGA A/B/C/D series according to the FAULT modes. The flowchart is described in Figure 6-1.

Figure 6-1. FAULT modes flowchart and involved bits/registers.



6.2 Actions and Restore modes

6.2.1 XMEGA A/B/C/D

After a FAULT is no more active, two modes can be selected to return to normal operation:

1. Latched mode:
   In Latched mode the waveform output will remain in the FAULT state until the FAULT condition is no longer active and the FDF has been cleared by software. The waveform output will return to normal operation at the next UPDATE condition when both these conditions are met.
2. Cycle-by-Cycle mode:
   In Cycle-by-Cycle mode the waveform output will remain in the FAULT state until the FAULT condition is no longer active. The waveform output will return to normal operation at the next UPDATE condition when this condition is met.

6.2.2 XMEGA E

According to the two FAULT types, the actions are:

1. Non-recoverable FAULT:
   In case of FAULT E (Non-recoverable FAULT):
   - The FAULT action will force all the Compare outputs to an inactive level. This inactive level can be configured thanks to bits FUSE (CTRLA.3) and values in FUSEBYTE6 (see Memory section) and Port configuration
   - SOFTWARE mode is enabled automatically (see description in Section 6.2.5)
   - HALT action (10 configurations) is also enabled automatically (see description in Section 6.2.4). This HALT Software mode requires a Software action with STATEECLR to recover

To achieve a CAPTURE, the same FAULT E input can be connected to a FAULT A or B input. If CAPTA or CAPTB bits (Fault capture bits of CTRLC and CTRLE registers) are set a Timer/Counter Capture will be automatically done when the non-recoverable FAULT occurs.

2. Recoverable FAULT:
   In case of FAULT A or B, different FAULT action modes can be individually configured. Most FAULT actions are not mutually exclusive. Hence two or more actions can be enabled at the same time to achieve a result that is a combination of FAULT actions.

   The individual modes are summarized below:

   - **KEEP (K)**
     Forces the inactive state until the end of Timer/Counter cycle even if the FAULT is no more present.
   - **ALT (H)**
     Two different Halt modes can be configured:
     - HARDWARE HALT ([0:1] bits mode)
       Halts the Timer/Counter as long the FAULT is active.
     - SOFTWARE HALT ([1:0] bits mode)
       Halts the Timer/Counter as long the FAULT is active (as in Hardware Halt) and requires a Software action.
   - **SOFTWARE (S)**
     Provides the way to raise the Error Interrupt Flag of Timer/Counter on fault detection.
   - **CAPTURE (C)**
     Provides the way to time stamp the FAULT event.
   - **RESTART (R)**
     Restarts a new Timer/Counter cycle.

These action modes are described in details in following sections.

6.2.3 KEEP mode

In this mode, the Compare output is kept at inactive level even if the FAULT input is no more present.

Figure 6-4 provides the flowchart of the KEEP mode process.

Figure 6-2 provides a waveform example if KEEPA and QUALA configurations are set.

With QUALA configuration FAULT Input A has no action when it occurs during the inactive level of channel output A.

Figure 6-2. Waveforms with KEEP and QUAL modes enabled.

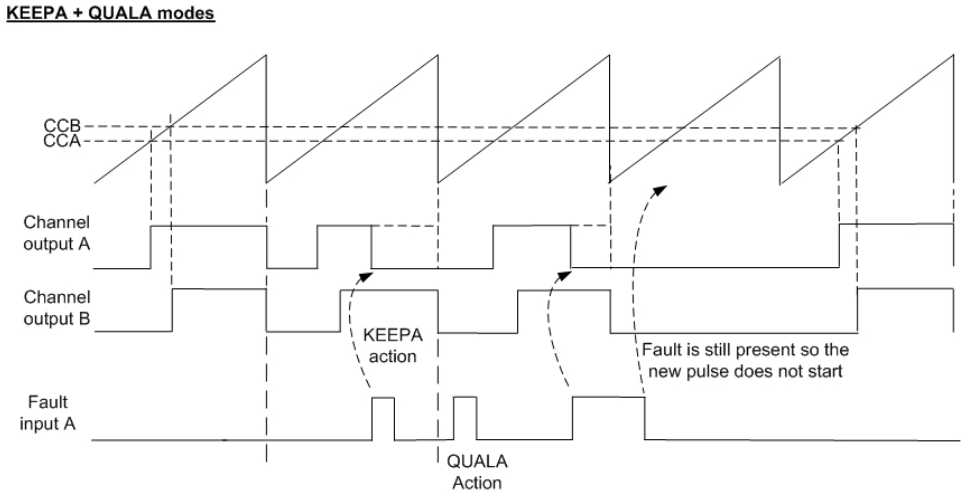


Figure 6-3 provides a waveform example if KEEPA and BLANKA configurations are set.

With this BLANKA configuration FAULT Input A has no action until the Blanking time (programmed in respectively DTLS/DTHS register) is reached (see Section 4.8) for respectively TC4/TC5.

Figure 6-3. Waveforms with KEEP and BLANK modes enabled.

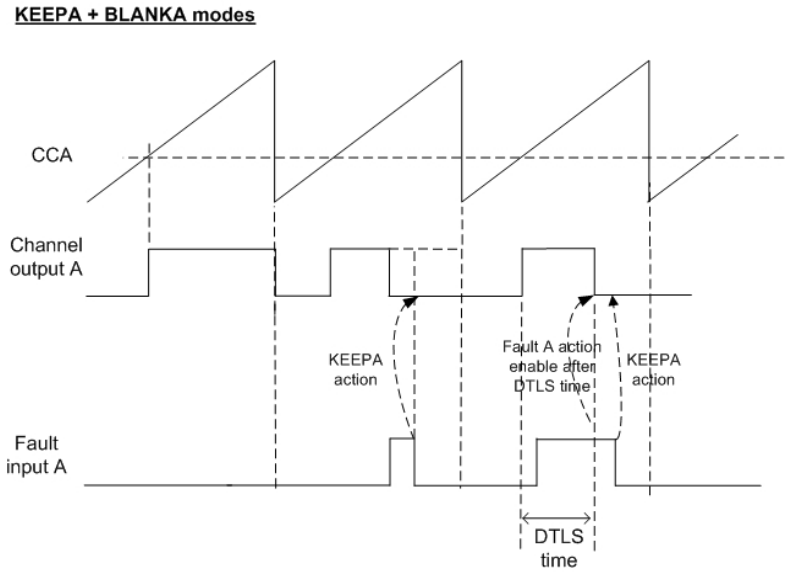
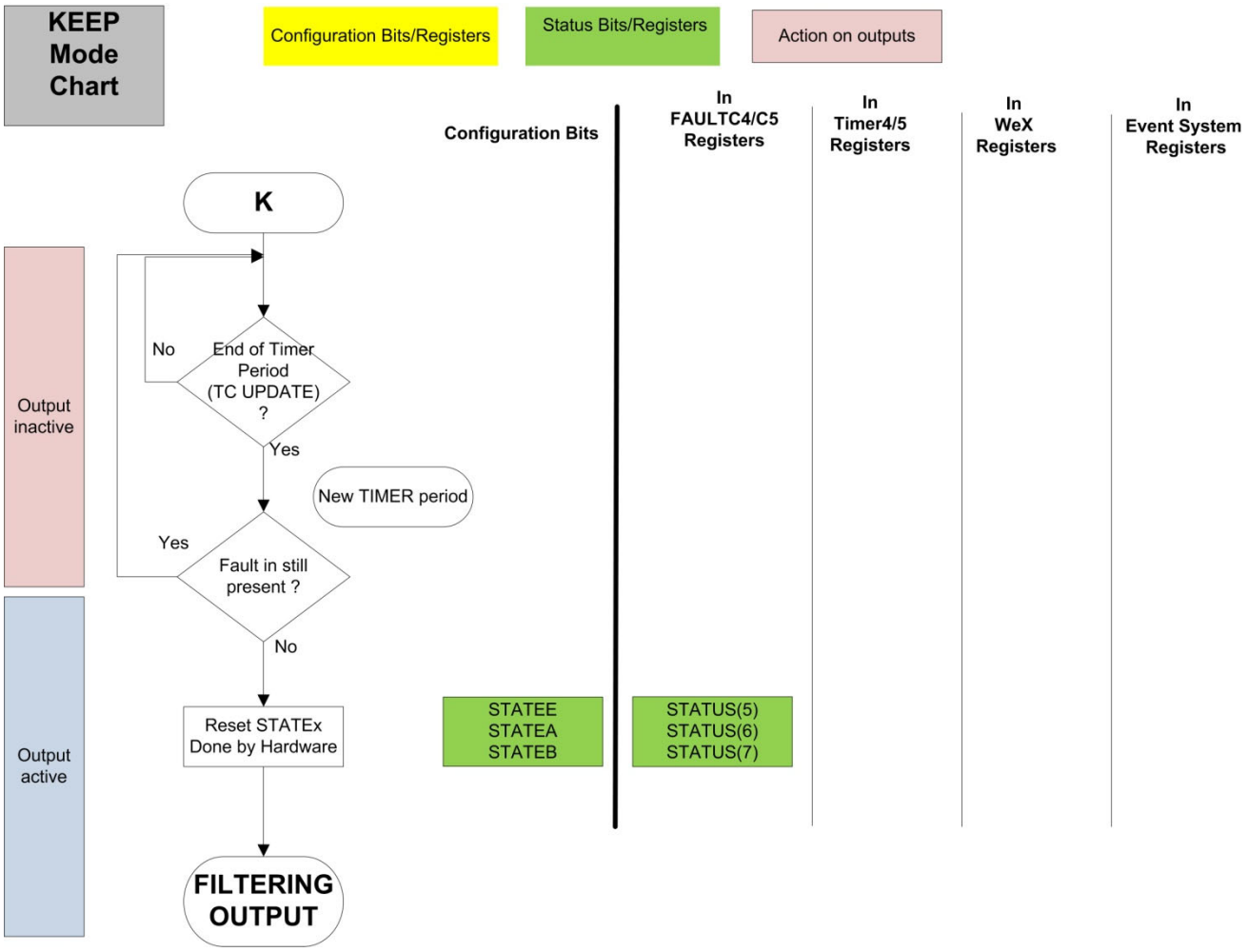


Figure 6-4. KEEP mode flowchart and involved bits/registers.



6.2.4 HALT mode

Figure 6-7 provides the flowchart of the global HALT process.

Two different HALT modes can be configured:

- Hardware HALT
- Software HALT

In Hardware HALT mode, the Timer/Counter is stopped since the FAULT input is present. Timer/counter will continue as soon as FAULT input disappears.

In Software HALT mode, the corresponding Timer/Counter will be stopped until FAULT input disappears and a software clear of Status bit (STATEECLR/HALTACLR/HALTBCLR in CTRLGCLR register). This provides a way to add a software control to the HALT action.

Figure 6-5 provides a waveform example of a Hardware Halt. (HALTA = [0:1]) with KEEPA and QUALA configurations set. Thanks to the QUALA configuration, FAULT Input A has no action if Channel output A is inactive.

Figure 6-5. Waveforms with hardware HALT and KEEP, QUAL modes enabled.

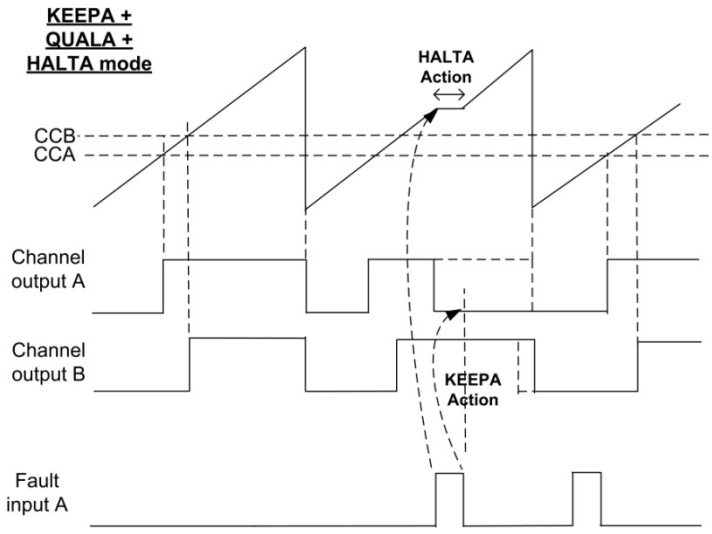


Figure 6-6 provides a waveform example of a Software Halt (HALTA = 0x10).

Figure 6-6. Waveforms with software HALT and KEEP, QUAL modes enabled.

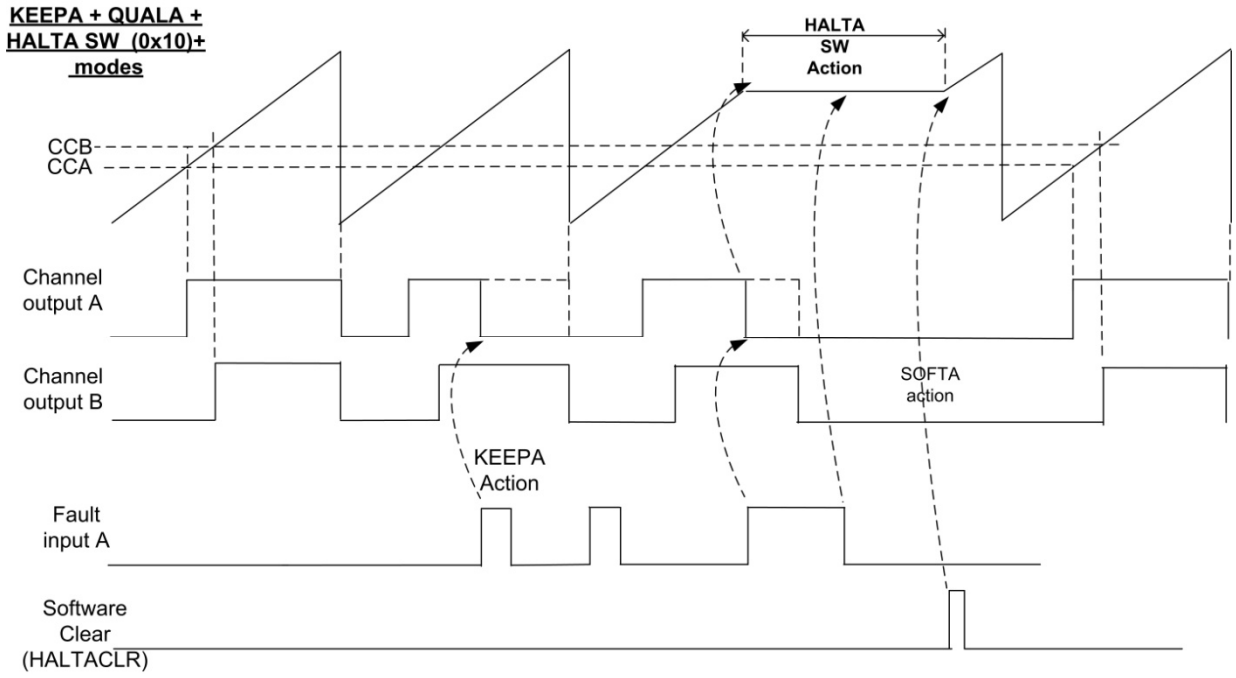
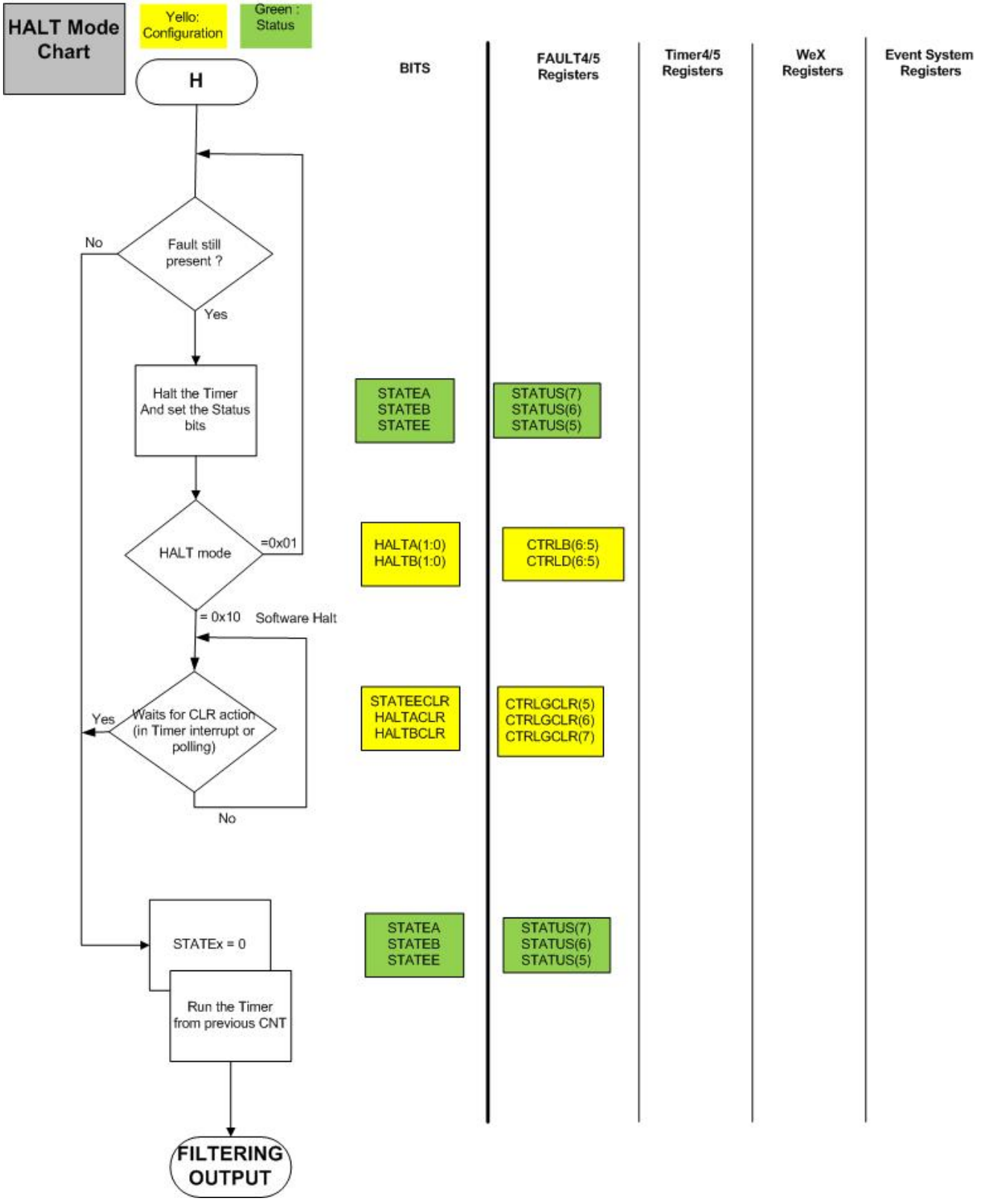


Figure 6-7. HALT mode flowchart and involved bits/registers.



6.2.5 SOFTWARE mode

Figure 6-8 provides the flowchart of the SOFTWARE process.

In this mode, as soon as corresponding FAULT input is detected, the following actions will occur in:

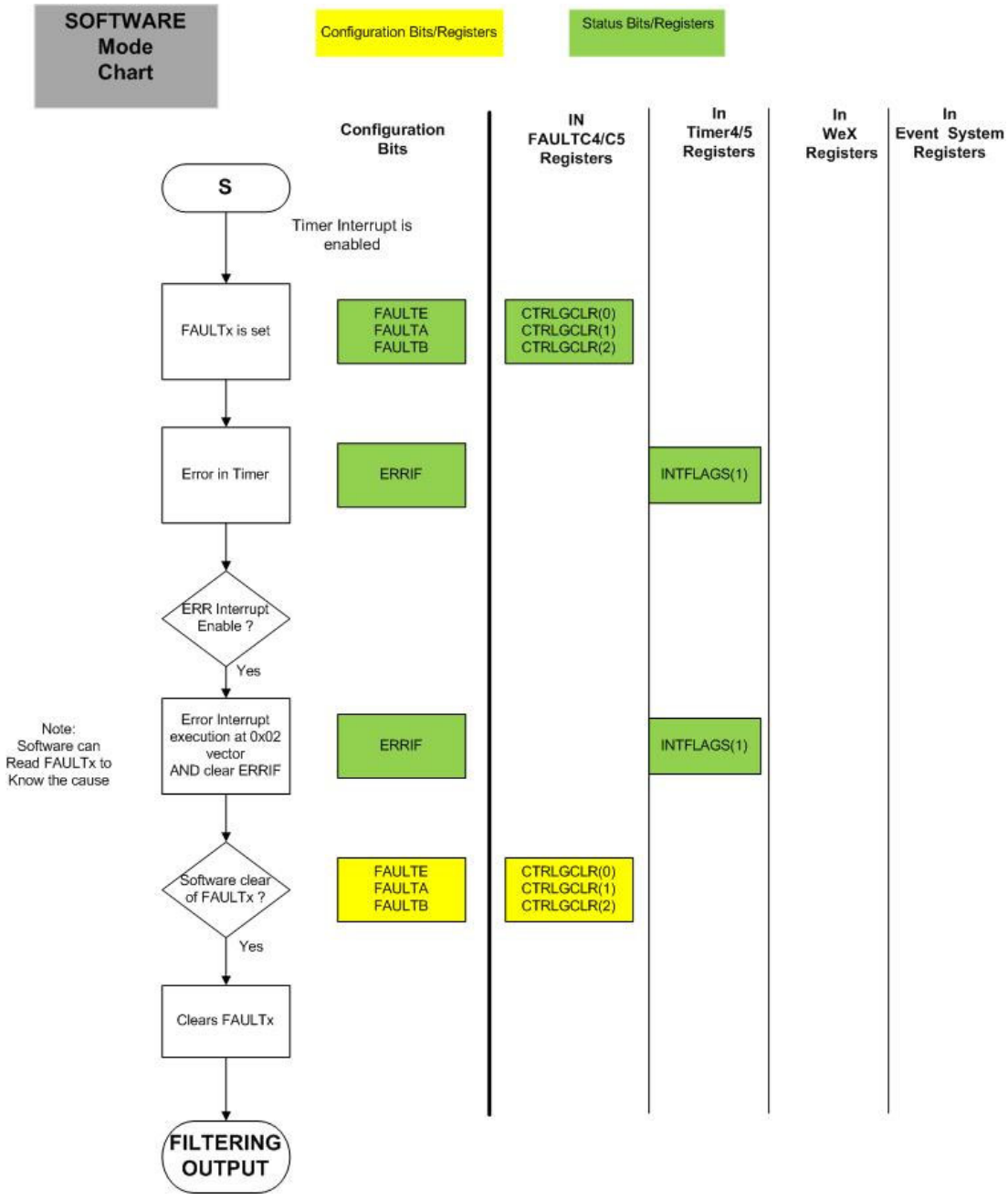
Corresponding Timer/Counter:

- Error Interrupt Flag (ERRIF) is set
- Interrupt routine (0x02 vector) is executed

Corresponding FAULT module:

- FAULTx Flag is set

Figure 6-8. SOFTWARE mode flowchart and involved bits/registers.



6.2.6 CAPTURE mode

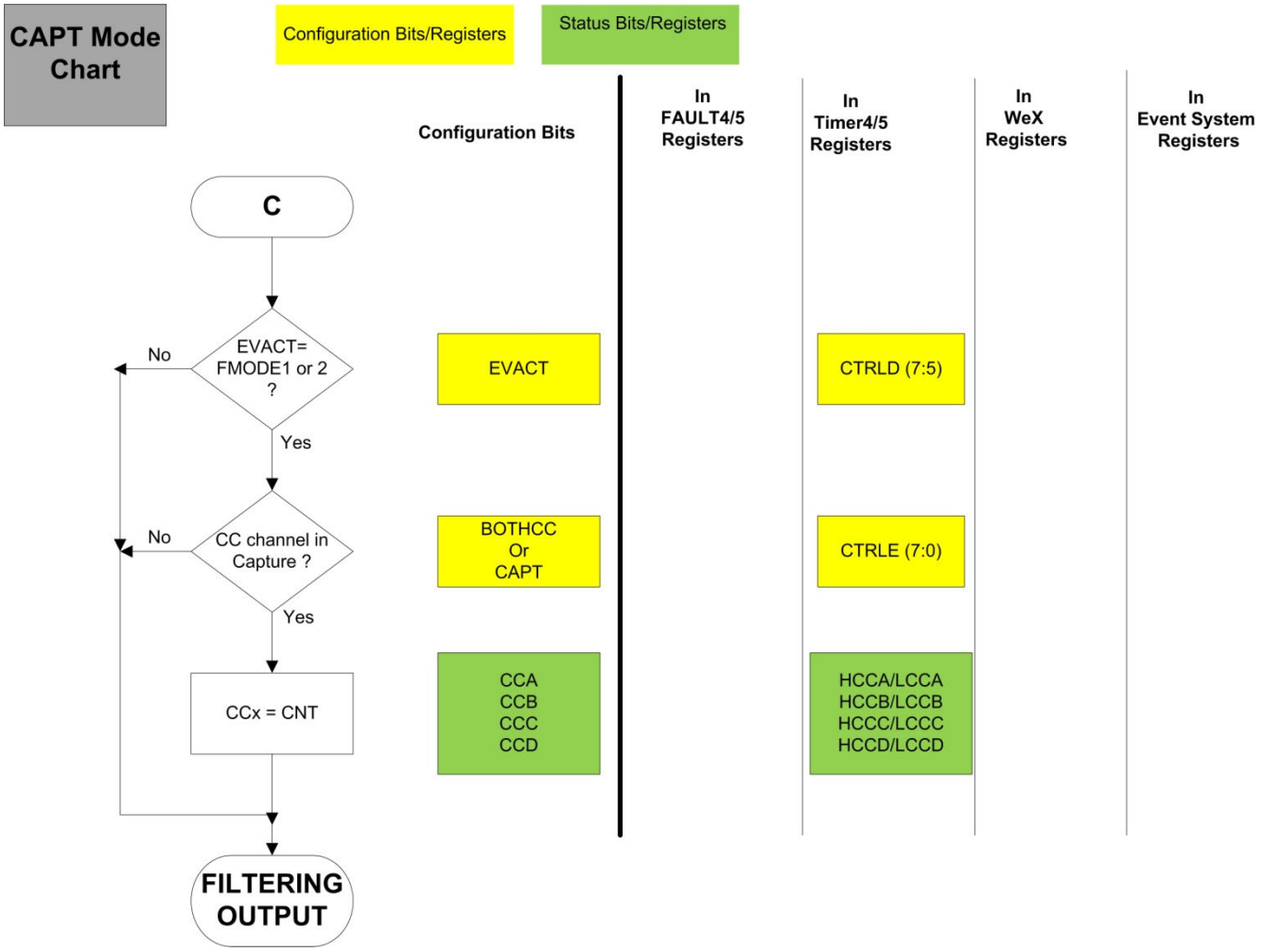
This mode can be used to get a Time stamp when FAULT occurs. This mode can be used, for instance, in a PFC control. It can monitor the time required to get the zero-crossing of the inductor current.

Figure 6-9 provides the flowchart of the CAPTURE process.

In this mode, two conditions are required to get a Capture of the Timer/Counter content when FAULT event occurs:

- Timer/Counter Event action configured in FMODE1 or FMODE2 mode. These modes are configured in EVACT[2:0] in Timer/Counter CTRLD register:
  - In FMODE1 mode, Fault A or B will trigger a Capture on CCA and CCB (if configured in Capture)
  - In FMODE2 mode, Fault A will trigger a Capture on CCA and CCC and Fault B will have an action on CCB and CCD
- Compare/Capture channel must be configured in Capture mode. See CCxMODE[1:0] in Timer/Counter CTRLE register

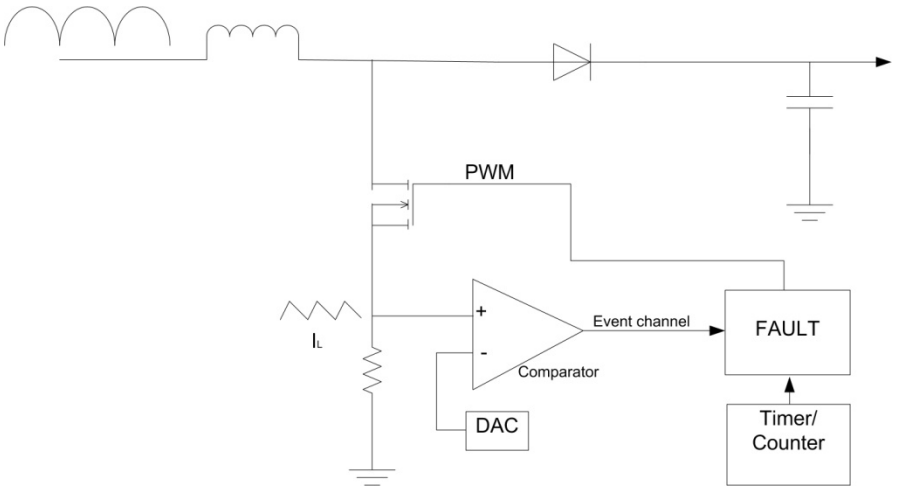
Figure 6-9. CAPT mode flowchart and involved bits/registers.



6.2.7 RESTART mode

This mode can be used for instance in the control of a PFC system, which schematics is described in Figure 6-10.

Figure 6-10. PFC system.



The PWM signal which controls the FET Gate in a PFC system is shown at the bottom of Figure 6-11. On-Time is fixed and PWM cycle is re-trigged when I_L current is zero crossing.

In this discontinuous mode (also named Critical Conduction mode), the inductor current I_L will go to zero during the off-time of every period.

As soon as I_L reaches 0, a new PWM cycle can be restarted.

Figure 6-11. PFC waveform.

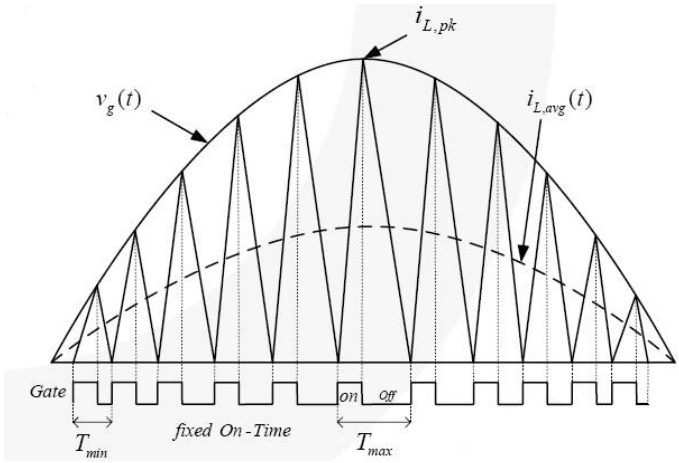


Figure 6-13 provides the RESTART flowchart. If RESTARTA or RESTARTB bit (CTRLB or CTRLD Register) is set, the Timer/Counter will be restarted from 0 when corresponding FAULT occurs. The on-going cycle is stopped and a new Timer/Counter cycle restarts.

Figure 6-12 provides the Channel outputs behaviors in the two following configurations:

- Upper waveforms: 1-Period mode (DeFAULT configuration)
- Lower waveforms: 2-Periods mode (RAMP2 set)

Figure 6-12. Waveforms examples in RESTART mode.

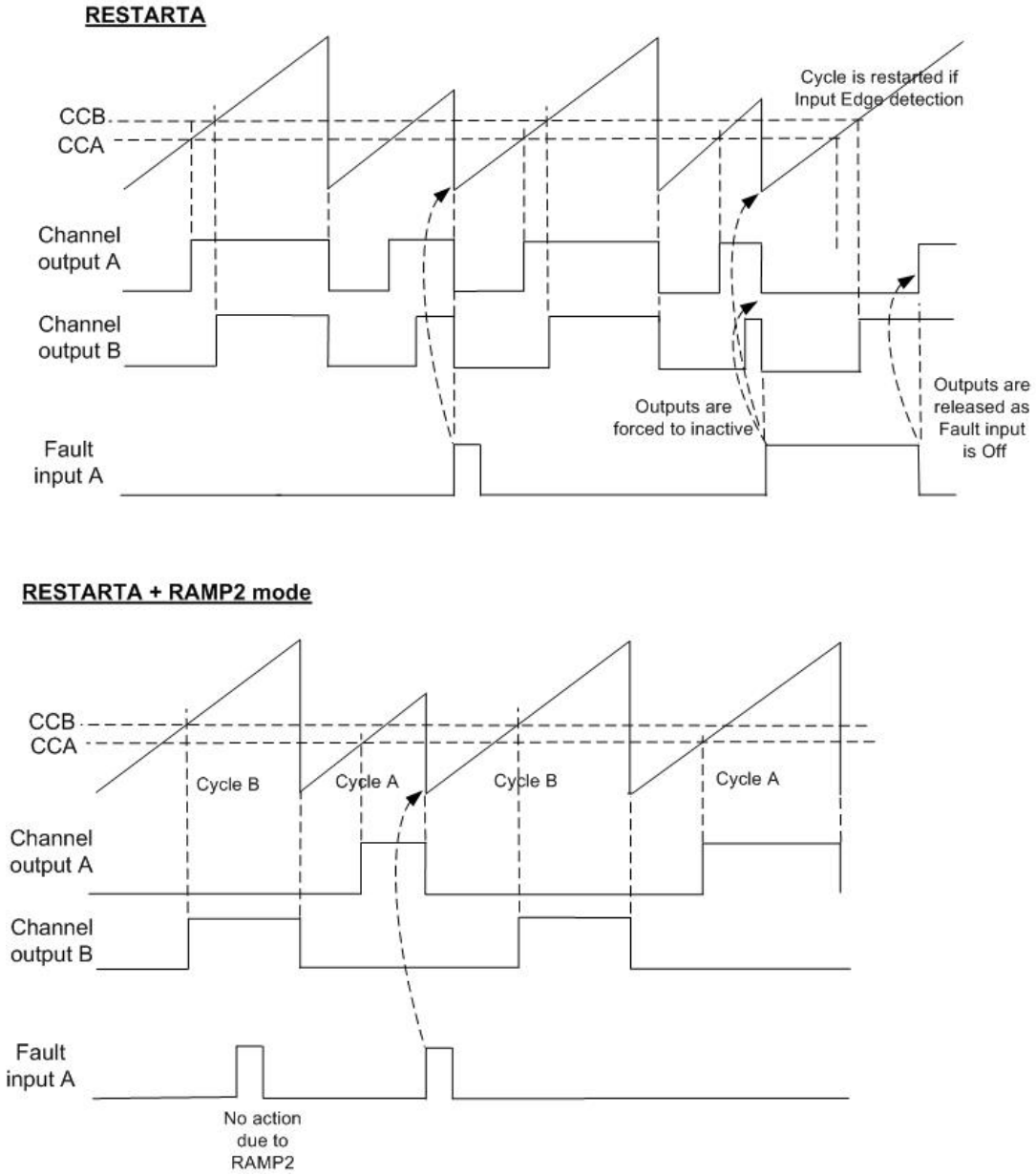
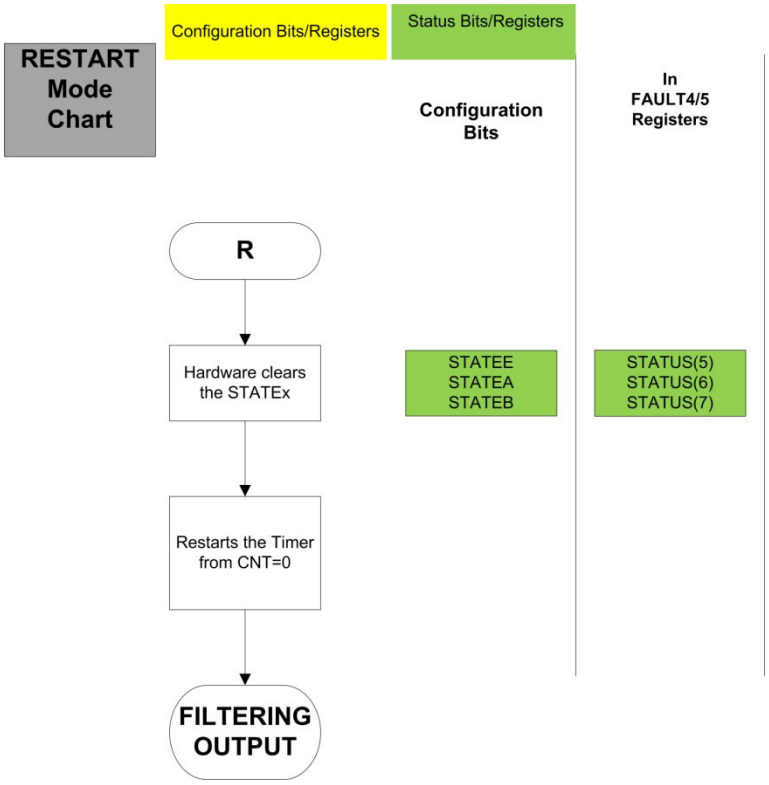


Figure 6-13. RESTART mode flowchart and involved bits/registers.



7. Driver Implementation

The included driver has functions that control all the major features of the FAULT modules. All functions take a pointer to a FAULT module as its first argument, so the same functions can be reused for all FAULT modules on the Atmel XMEGA E.

Note: This driver is **not** written with high performance in mind. It is designed as a library to get started with the XMEGA E Timer/Counters 4 and 5 and an easy-to-use framework for rapid prototyping. For time and code space critical application development, consider replacing function calls with macros or direct access to registers.

7.1 Files

The driver package consists of the following files:

- tc45.c – FAULT driver source file
- tc45.h – FAULT driver header file

8. Revision History

Doc. Rev.	Date	Comments
42088A	04/2013	Initial document release

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