VSC8211

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC8211 product family. It is meant to help customers achieve first-pass design success. These checklist items should be followed when utilizing the VSC8211 in a new design. A summary of these items is provided in Section 11.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Twisted Pair Media Interface (CAT5)"
- Section 5.0, "SGMII/SerDes MAC Interface"
- Section 6.0, "Parallel MAC Interface"
- Section 7.0, "Device Clocks"
- Section 8.0, "Hardware Configuration Using CMODE Pins"
- Section 9.0, "Digital Interface"
- Section 10.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC8211 implementor should have the following documents on hand:

- VSC8211 *Single-Port 10/100/1000BASE-T, 1000BASE-X, and 100BASE-FX PHY Data Sheet*
- Device documents on the VSC8211 product page at www.microchip.com
- VSC8211EV EVB schematics and PCB information in the *VSC8211 Evaluation Board User Guide* as well as VSC8211 PCB design and layout guidelines at www.microchip.com.

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- A single ground reference as a system ground is used for all ground pins. Use one continuous ground plane to ensure a low-impedance ground path and a continuous ground reference for all signals.
- A chassis ground is necessary between the magnetics and RJ45 connector at line side for better EMI and ESD.

3.0 POWER

Table 3-1 shows the power supply pins for the VSC8211.

TABLE 3-1: POWER SUPPLY PINS

Pin Name	117 LBGA Ball	Voltage (V)	Descriptions	Associated Functional Pins
Digital I/O Power Pins				
VDDIOMAC	C6, C3, D3	3.3V or 2.5V	Power for the parallel MAC interface	**RXLOS/SIGDET, RXD7:0], RXDV, RXER, RXCLK, COL, CRS, TXCLK, TXER, GTX-CLK, TXEN, TXD [7:0], MODDEF0/CLK-OUTMAC**
VDDIOMICRO	G7	3.3V or 2.5V	3.3V or 2.5V, Power for SMI, EEPROM interface and CLKOUTMICRO clock	**EECLK/PLLMODE, EEDAT, TXDIS/, *SRESET*, *MDINT*, MODDEF1/MDC, MODD-EF2/MDIO, CLKOUTMICRO/*OSCDIS***
VDDIOCTRL	D10	3.3V or 2.5V	Power for JTAG I/O	***RESET*, TDO, TDI, TMS, TCK, *TRST*,**
Digital Core Power Pins				
VDD12	C10, C11, F3, F4, G3	1.2V	Power for internal digi-tal logic, and SerDes/ SGMII I/O power	**RDP, RDN, TDP, TDN, SCLKP, SCLKN, SDIN, SDIP, SDOP, SDON**
Analog Power Pins				
VDD33A	F10, G10, G9, G8	3.3V	Power for MDI, CMODE, PLL, and LED blocks. For analog core power, use ferrite bead.	**LED [4:0], CMODE7:0], TXVND, TXVPD, TXVNC, TXVPC, TXVNB, TXVPB, TXVNA, TXVPAXTAL2, XTAL1/REFCLK, REF-FILT, REFREXT**
VDD12A	H7	1.2V	Power of PLL and ADC blocks. For analog core power, use ferrite bead.	—
Ground Pins				
VSS	C5, D4, D5, D6, D7, D8, D9, E4, E5, E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, J7, H9, J9, H11, J11	0V	Ground for all blocks	—

3.1 Current and Power Requirements

- Ensure that the voltage regulators and power distribution are designed to adequately support these current requirements for each power rail. Refer to Table 3-2 for different system configurations. Note that the power dissipation values in the table need 25% to 30% based on the maximum current for the power supply designs of 3.3V, 1.2V, and 2.5V. Designs with 100Base-FX need an additional margin of 35% to 50% based on the typical current for the power supply designs of 3.3V and 1.2V. See Table 3-3 for details.

TABLE 3-2: MAXIMUM RAIL CURRENT

Power Rail	Voltage (V)	Maximum Current (mA)	Power Dissipation (mW)
VDDIO at 3.3V, RGMII-CAT5, 1000BASE-T, FD, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode Off			
VDD33A	3.3	110	363
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	3.3	53	175
VDD12	1.2	324	389
VDD12A	1.2	38	46
VDDIO at 2.5V, RGMII-CAT5, 1000BASE-T, FD, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode Off			
VDD33A	3.3	110	363
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	2.5	41	103
VDD12	1.2	324	389
VDD12A	1.2	38	46
VDDIO at 3.3 V, RGMII-CAT5, 100BASE-TX, FD, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode Off			
VDD33A	3.3	91.5	303
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	3.3	19	63
VDD12	1.2	103	124
VDD12A	1.2	26.5	32
VDDIO at 2.5 V, RGMII-CAT5, 100BASE-TX, FD, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode Off			
VDD33A	3.3	91.5	303
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	2.5	15	38
VDD12	1.2	103	124
VDD12A	1.2	26.5	32
VDDIO at 3.3 V, RGMII-CAT5, 10BASE-T, FD, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode Off			
VDD33A	3.3	152	502
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	3.3	14	46
VDD12	1.2	31	37
VDD12A	1.2	27	32
VDDIO at 2.5 V, RGMII-CAT5, 10BASE-T, FD, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode Off			
VDD33A	3.3	152	502
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	2.5	11	28

TABLE 3-2: MAXIMUM RAIL CURRENT

Power Rail	Voltage (V)	Maximum Current (mA)	Power Dissipation (mW)
VDD12	1.2	31	37
VDD12A	1.2	27	32
VDDIO at 3.3 V, RGMII-Fiber, 1000BASE-X, FD, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode Off			
VDD33A	3.3	20	66
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	3.3	53	175
VDD12	1.2	56.5	68
VDD12A	1.2	23	28
VDDIO at 2.5 V, RGMII-Fiber, 1000BASE-X, FD, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode Off			
VDD33A	3.3	20	66
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	2.5	42	105
VDD12	1.2	56.5	68
VDD12A	1.2	23	28
VDDIO at 3.3 V, SerDes-CAT5, 1000BASE-T, FD, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode Off			
VDD33A	3.3	112	370
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	3.3	14	46
VDD12	1.2	343	412
VDD12A	1.2	37	44
VDDIO at 2.5 V, SerDes-CAT5, 1000BASE-T, FD, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode Off			
VDD33A	3.3	112	370
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	2.5	10	33
VDD12	1.2	343	412
VDD12A	1.2	37	44
VDDIO at 3.3 V, SerDes-CAT5, 1000BASE-T, FD, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode On			
VDD33A	3.3	112	370
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	3.3	14	46
VDD12	1.2	283	340
VDD12A	1.2	37	44

TABLE 3-3: TYPICAL RAIL CURRENTS FOR DESIGN WITH 100BASE-FX

Power Rail	Voltage (V)	Typical Current (mA)	Power Dissipation (mW)
VDDIO at 3.3V, RGMII-100BASE-FX, FDX, 1518 Byte Random Data Packet, 100% Utilization, SFP Mode Off			
VDD33A	3.3	96	317
VDDIOMAC, VDDIOMICRO, VDDIOCTRL	3.3	19	63
VDD12 + VDD12A	1.2	145	174

3.2 Power Supply Planes

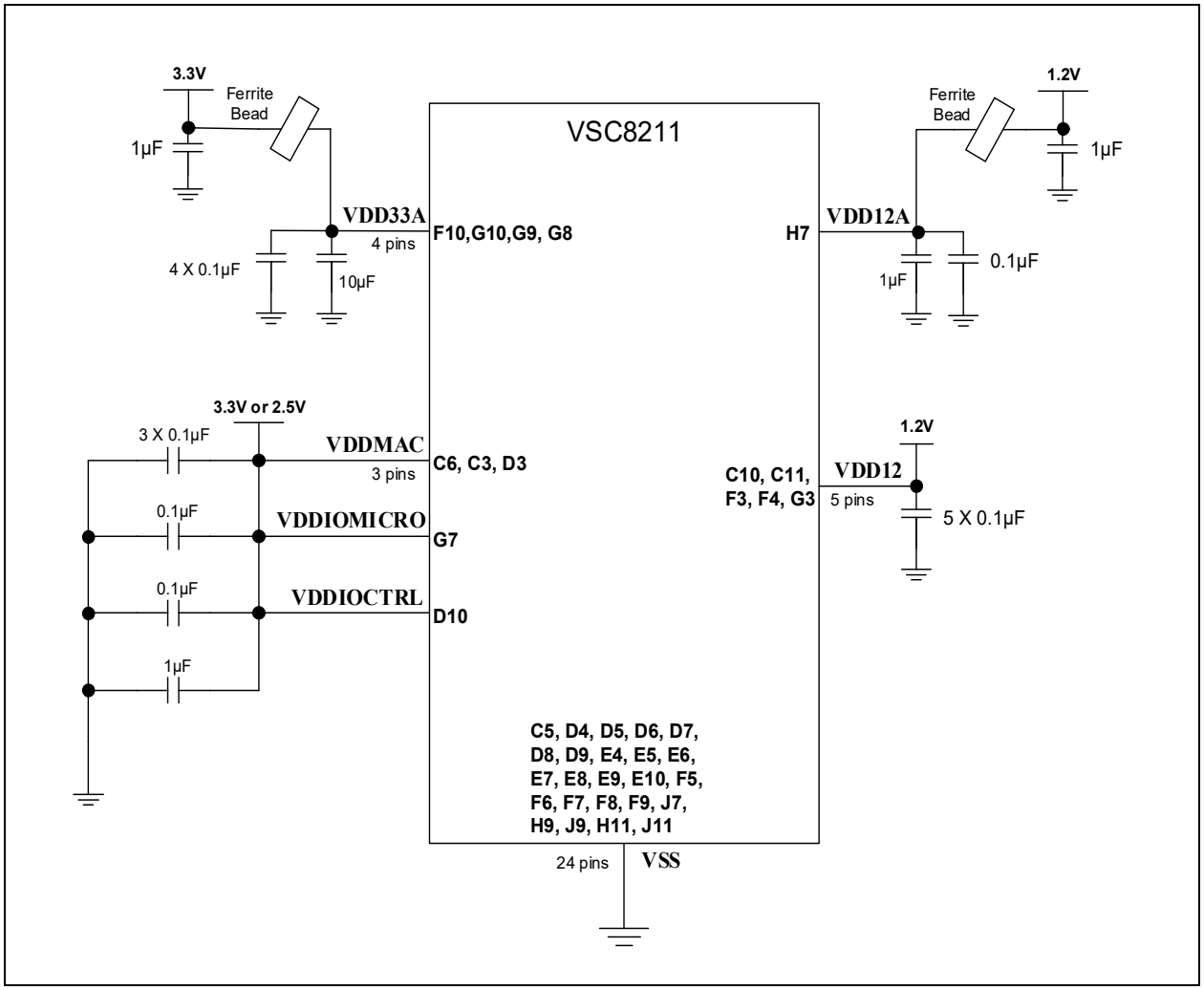
- The VSC8211 requires two power rails of 3.3V and 1.2V or three power rails of VDDIO 2.5V, 3.3V, and 1.2V. The filtered analog 1.2V and 3.3V supplies should not be shorted to any other digital supply at the package or PCB level. See Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering".
- The most important PCB design and layout considerations are as follows:
  - Ensure that the return plane is adjacent to the power plane (without a signal layer in between).
  - Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.
  - Minimize resistive drop while efficiently conducting away heat from the device using 1 oz copper cladding.
- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent random system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power the pins of the device with correctly positioned local decoupling. For more information, see Section 3.4, "Bulk Decoupling Capacitors".
- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or high-power devices.

3.3 Power Circuit Connection and Analog Power Plane Filtering

- The analog power supplies are:
  - **VDD33A**
  - **VDD12A**
- A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.
- Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with 0Ω resistors once a thorough evaluation of system performance is completed.
- Ferrite beads are not recommended for digital supplies **VDDIOMAC**, **VDDIOMICRO**, **VDDIOCTRL**, and **VDD12**.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



3.4 Bulk Decoupling Capacitors

- Bulk decoupling capacitors can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and placed as close as possible to the VSC8211's power pins.
- Make sure that enough bulk capacitors (1 µF to 22 µF) are incorporated in each power rail of the power supply.
- If the VSC8211 device is on the top layer of the printed circuit board (PCB), the best location for local decoupling capacitors is on the bottom or underside of the PCB, directly under the device.

4.0 TWISTED PAIR MEDIA INTERFACE (CAT5)

4.1 10/100/1000 Mbps Interface Connection

The VSC8211 has one GPHY that supports 10/100/1000Base-T Ethernet Gigabit port. Details on the pin numbers for this GPHY are described as follows:

- **TXVNA** (J12): This pin is the transmit/receive negative connection from Pair A of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPA** (J13): This pin is the transmit/receive positive connection from Pair A of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVNB** (H12): This pin is the transmit/receive negative connection from Pair B of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPB** (H13): This pin is the transmit/receive positive connection from Pair B of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVNC** (G12): This pin is the transmit/receive negative connection from Pair C of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPC** (G13): This pin is the transmit/receive positive connection from Pair C of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVND** (F12): This pin is the transmit/receive negative connection from Pair D of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPD** (F13): This pin is the transmit/receive positive connection from Pair D of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.

There are two types of 10/100/1000 Mbps channel connection solutions. As shown in Figure 4-1, the first solution is for cases wherein no electrical noise external environment and ESD are taken into consideration. The second solution, on the other hand, is for instances wherein electrical noise external environment and ESD are considered. See Figure 4-2.

FIGURE 4-1: FIRST SOLUTION FOR 10/100/1000 MBPS CHANNEL CONNECTION

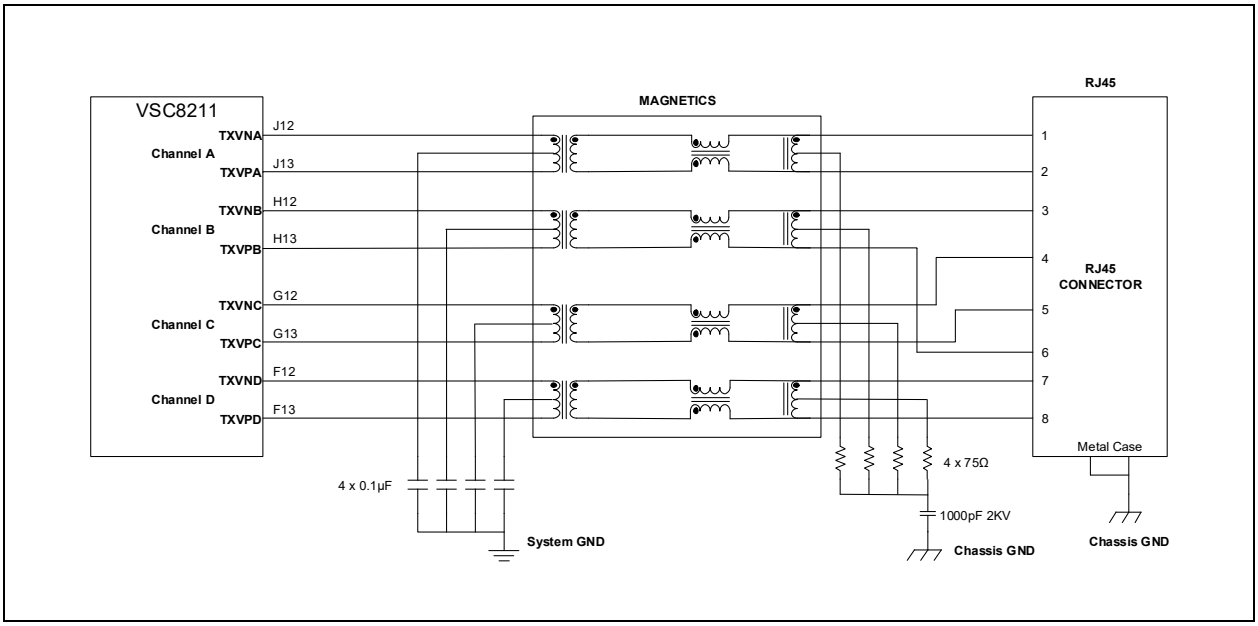
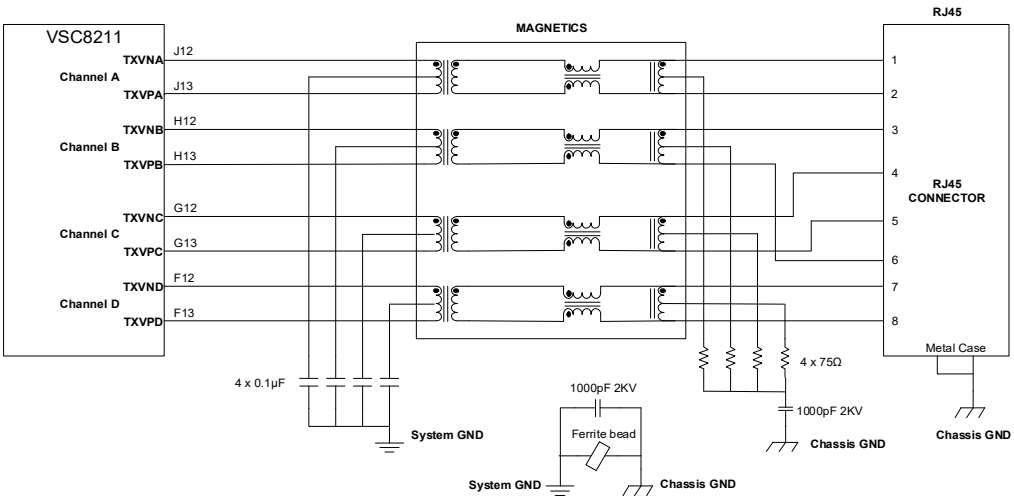


FIGURE 4-2: SECOND SOLUTION FOR 10/100/1000 MBPS CHANNEL CONNECTION



4.2 10/100/1000 Magnetics and RJ45 Connector Connection

- The center tap connection on the VSC8211 side for Pair A channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8211 side for Pair B channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8211 side for Pair C channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8211 side for Pair D channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center taps from all four pairs of the magnetics should not be connected together without the 0.1 µF capacitors to ground. The reason is the common-mode voltage can be different between pairs, especially for 10/100 operation. (Pairs A and B are active, while Pairs C and D are inactive.)
- It is recommended that the center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) be terminated with a 75Ω resistor through a common 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by Pair A, Pair B, Pair C, and Pair D center taps.
- Only one 1000 pF, 2 kV capacitor or a ferrite bead should connect between the chassis ground and the system ground.
- The RJ45 shield should connect to the chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 4.3, "PCB Layout Considerations" for guidance on how the chassis ground should be created from system ground.
- For the magnetics selection, please refer to magnetics suggested guidelines (*ENT-AN0098 Magnetics Guide* on Microchip Technology product page) for reference.

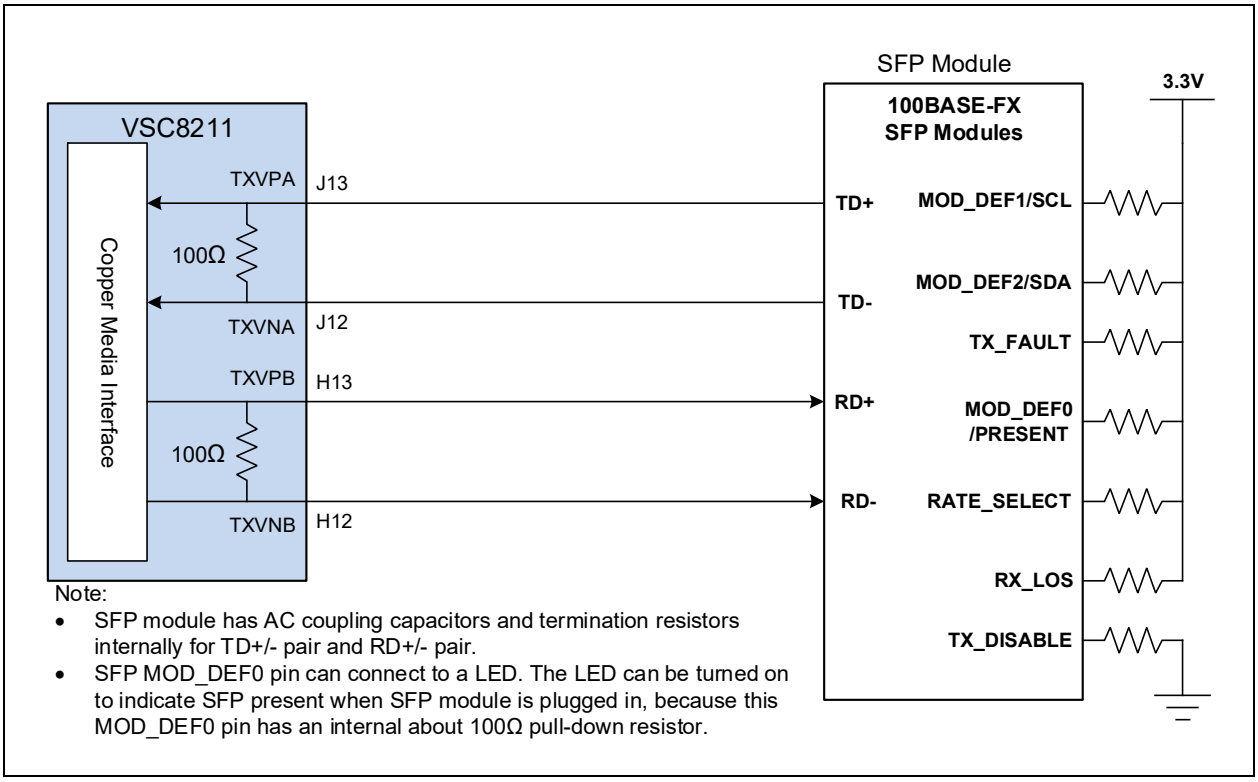
4.3 PCB Layout Considerations

- All differential pairs of the MDI interface traces should have a characteristic impedance of 100Ω to the GND plane. This is a strict requirement to minimize return loss that requires a PCB designer and FAB house.
- Each MDI pair should be placed as close as possible in parallel to minimize EMI and crosstalk. Each member of a pair should be matched in length to prevent mismatch in delay that would cause common-mode noise.
- Ideally, there should be no crossover or via on the signal paths.
- Incorporate a 1000 pF 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor or ferrite bead far away from the VSC8211 device or other sensitive devices in the PCB layout placement for better ESD.

4.4 100 MBPS Fiber Support Over Copper Media Interface

- The VSC8211 supports 100BASE-FX over its copper media interface by using pairs A and B, which provide **TX** and **RX** differential connections, respectively. If the fiber module does not have internal AC coupling capacitors, then they are required between the PHY and fiber module. The value should be 0.1 µF.
- The RXLOS/SIGDET signal is not used in this mode.
- The PHY can be brought into the 100BASE-FX Operation mode using the following configuring sequence:
  1. Initialize the PHY into the specific MAC-to-Copper Operating mode for the MAC interface type required (register23).
  2. Disable Auto-Negotiation and force the 100BASE-T FDX mode (register 0).
  3. Run the 100BASE-FX initialization script. For more details, see Section 33.4 of the data sheet.
- Figure 4-3 shows the copper media interface connections to 100Base-FX SFP.

FIGURE 4-3: COPPER MEDIA INTERFACE CONNECTIONS FOR 100BASE-FX



Note:
- SFP module has AC coupling capacitors and termination resistors internally for TD+/- pair and RD+/- pair.
- SFP MOD_DEF0 pin can connect to a LED. The LED can be turned on to indicate SFP present when SFP module is plugged in, because this MOD_DEF0 pin has an internal about 100Ω pull-down resistor.

5.0 SGMII/SERDES MAC INTERFACE

5.1 SGMII/SerDes MAC Pins and Connection

- The VSC8211 device supports one SGMII (Serial Gigabit Media Independent Interface) MAC or one SerDes MACs.
- Refer to Table 5-1 for pin number details. For SGMII/SerDes interface connections, see Figure 5-1 and Figure 5-2.

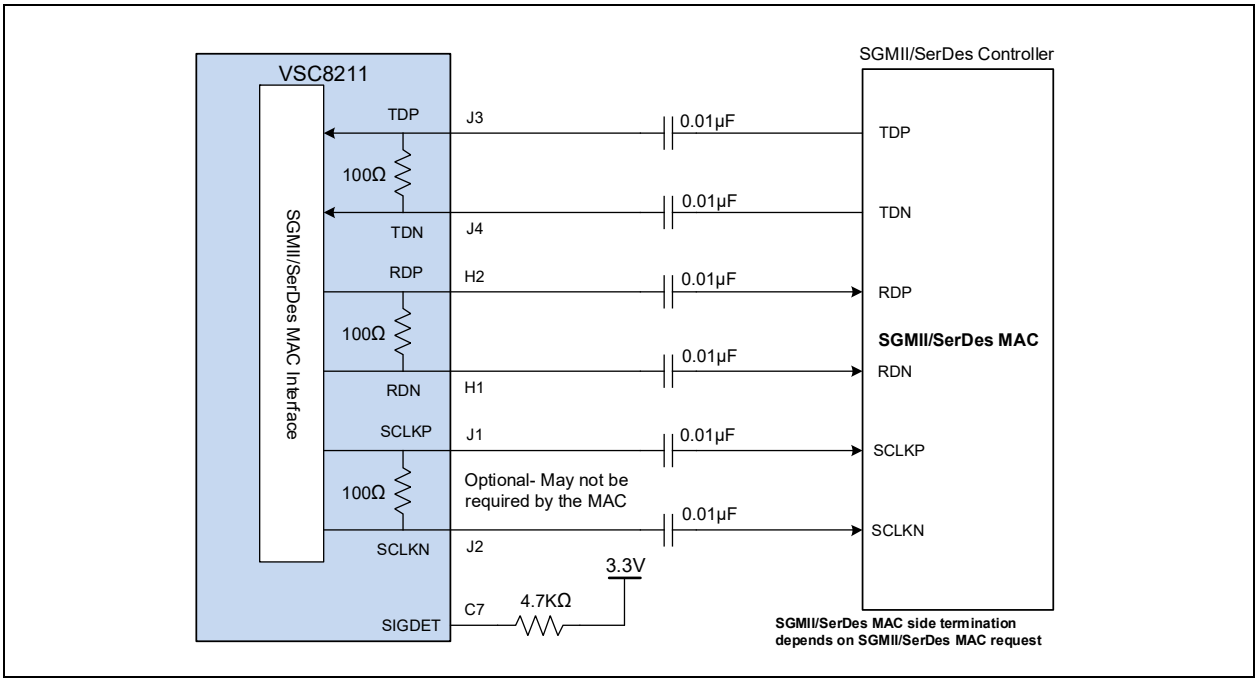
TABLE 5-1: SGMII/SERDES MAC INTERFACE PINS

Pin Name	Pin Number	Type	Description
RDN	H1	Output DIFF	Receiver Data Differential Output Pair (used in SerDes/SGMII to CAT5 and Parallel MAC to SerDes/AMS PHY operating modes)
RDP	H2	Output DIFF	
TDN	J4	Input DIFF	Transmitter Data Differential Input Pair (used in SerDes/SGMII to CAT5 and Parallel MAC to SerDes/AMS PHY operating modes)
TDP	J3	Input DIFF	
SCLKN	J2	Output DIFF	SGMII Clock Differential Output Pair (used in SGMII to CAT5/SerDes/ AMS PHY operating modes).
SCLKP	J1	Output DIFF	
SDIP	G2	Input DIFF	Fiber Transceiver Differential Input Pair (used in SGMII to SerDes)
SDIN	G1	Input DIFF	Fiber 1000Base-X SFP operation mode
SDOP	F2	Output DIFF	Fiber Transceiver Differential Output Pair (used in SGMII to SerDes)
SDON	F1	Output DIFF	Fiber 1000Base-X SFP operation mode

5.2 SGMII/SerDes MAC

- SGMII (Serial Gigabit Media Independent Interface) serializes a gigabit interface (such as GMII) into a high-speed, two-pin differential interface. Using SGMII/SerDes can reduce the pin count to four pins per Ethernet port.

FIGURE 5-1: SGMII/SERDES MAC INTERFACE CONNECTIONS



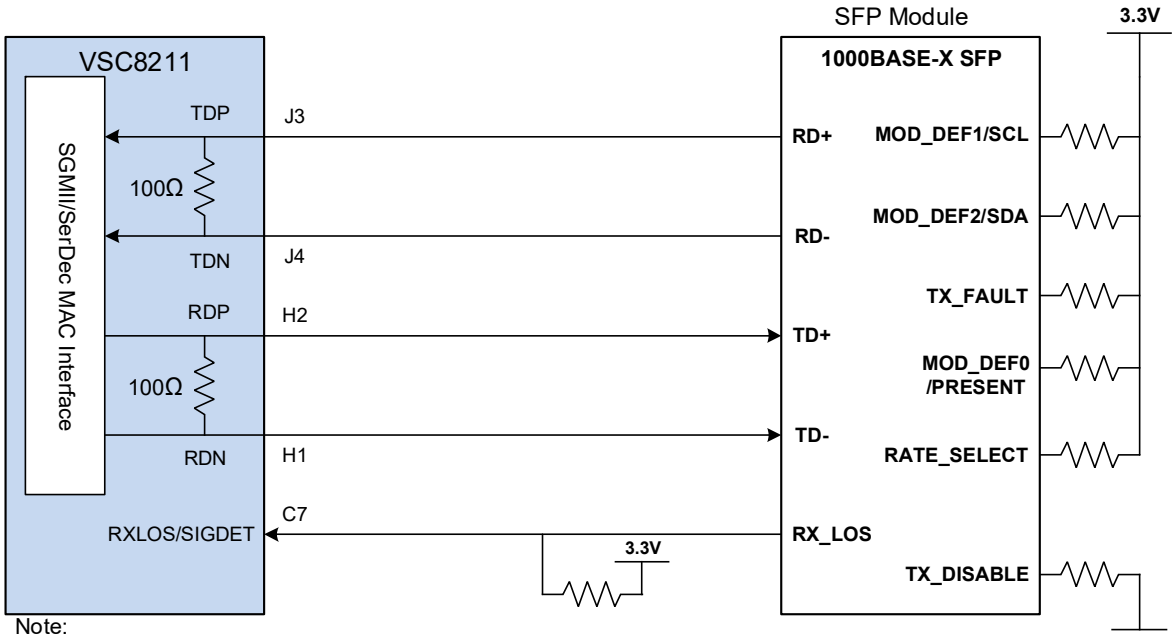
5.3 SerDes MAC Interface to SFP

- When connected to a SerDes MAC-compliant to 1000BASE-X, the VSC8211 device provides data throughput at a rate of 1000 Mbps only. 10 Mbps and 100 Mbps rates are not supported.
- For additional pin in SerDes MAC interface to SFP fiber transceiver module, see Table 5-2. Figure 5-2 shows the SerDes MAC interface connection to 1000Base-X SFP.

TABLE 5-2: ADDITIONAL PIN RXLOS FOR SERDES TO SFP

Pin Name	Pin Number	Type	Description
RXLOS/SIGDET	C7	I/O	The customer can connect the **SIGDET** pin from a Fiber module (or the **RXLOS** from an SFP). See Table 8-4 for information on using **CMODE** configuration pin CMODE1[3] to set either **RXLOS** or **SIGDET**.
			RXLOS – Receiver Loss of Signal Output (valid in SFP mode, when MII Register 21E.15 = 1) **RXLOS** pin is input, the receiving loss signal comes from the output of **SFP LOS** pin. This active-high signal is asserted when receiving signal loss.
			SIGDET – SerDes Signal Detect (I/O) (valid in IEEE Mode, when MII Register 21E.15= 0) **SIGDET** can be configured as an input or output and can be configured to function as active-low or active-high by using CMODE1[1] and CMODE1[3] at startup. See Table 8-3 and Table 8-4 for details. **SIGDET as Input:** When used as an input, the SIGDET signal is meant to be connected to the signal detect output of the fiber optic transceiver. If **SIGDET** is high, this indicates received activity on the fiber optic transceiver. If **SIGDET** is not used as an input, the PHY internally generates the signal detect function from the incoming data on the **TDP** and **TDN** signal pins. **SIGDET as Output:** For Serial MAC to CAT5 Media PHY Operating modes, **SIGDET** is asserted if a valid CAT5 link has been established.

FIGURE 5-2: SERDES MAC INTERFACE TO 1000BASE-X SFP OR 1000BASE-T SFP CONNECTIONS



Note:
- SFP module has AC coupling capacitors and termination resistors internally for TD+/- pair and RD+/- pair.
- SFP MOD_DEF0 pin can connect to a LED. The LED can be turned on to indicate SFP present when SFP module is plugged in, because this MOD_DEF0 pin has an internal about 100Ω pull-down resistor.

5.4 SGMII/SerDes MAC Interface Design Rules

- Use AC coupling with 0.01 µF capacitors for chip-to-chip applications. Place the capacitors at the receiving end of the signals.
- Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or strip-line).
- Traces should be of equal length (within 10 mils) on each differential pair to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Spacing equal to five times the ground plane gap is recommended between adjacent tracks to reduce cross-talk between differential pairs. Minimum spacing of three times the ground plane gap is required.
- Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to reduce the strength of any radiating spurious fields.
- Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.
- If the SGMII/SerDes port is unused, both the **RDx** pair and **TDx** pair pins can be left floating (no-connect).

6.0 PARALLEL MAC INTERFACE

The VSC8211 parallel MAC interface supports GMII, RGMII, MII as well as TBI and RTBI interfaces. For detailed GMII/RGMII/MII pin descriptions and system design connections, refer to Section 6.1, "GMII/RGMII/MII Interface Pins". For detailed TBI/RTBI pin descriptions and system design connections, refer to Section 6.2, "TBI/RTBI Interface Pins".

6.1 GMII/RGMII/MII Interface Pins

The VSC8211 supports GMII, RGMII, and MII interfaces. The GMII and RGMII support all three speeds—10 Mbps, 100 Mbps, and 1000 Mbps—and can be used to interface to other end devices with GMII and RGMII interfaces. The MII interface supports all two speeds of 10 Mbps and 100 Mbps. It can also be used to interface to other end devices with MII interface. See Table 6-1 for pin details.

TABLE 6-1: GMII/RGMII/MII INTERFACE PINS

Pin Name	Pin Number	Type	Description
RXCLK, RXC	B5	O	**Receive Clock Output** (GMII, RGMII, and MII modes) Receive data is sourced from the PHY synchronous to the rising edge of **RXCLK** in GMII/MII modes or **RXC** in RGMII mode. This clock is recovered from the media.
RXER, RXCTL	A4	O	**RXER – Receiver Error Output** for **GMII** and **MII** **RXCTL –** Multiplexed receive data valid for **RGMII** receive control output
RD [7:4], RD [3:0], RXD [3:0]	A7, B7, A6, B6	O	**RD [7:4]** – **RGMII** data output. Use the falling edge of **RXC**. **RD [3:0]** – **RGMII** data output. Use the rising edge of **RXC**. **RXD [3:0]** – **GMII/MII** data output. Use the rising edge of **RXCLK**.
RXD [7:4]	A9, B9, A8, B8	O	Receive Data Code Group (GMII mode) Receive data is driven out of the device synchronously to the rising edge of **RXCLK**.
RXDV	A5	O	**Receive Data Valid Output** (GMII, MII modes) **RXDV** is asserted by the PHY to indicate that the PHY is presenting recovered and decoded data on the **RXD** pins. **RXDV** is synchronous with respect to **RXDK**.
CRS	C4	O	**Carrier Sense Output** (GMII, MII modes) Valid only in GMII and MII Half-Duplex modes, CRS is asserted high when a valid carrier is detected on the media.
COL	B4	O	**Collision Detect Output** (GMII, MII modes) This output is asserted high when a collision is detected on the media. For Full-Duplex modes, this output is always low.
TXCLK	A3	O	**Transmit Clock** (MII mode) 25 MHz (100 Mb mode) or 2.5 MHz (10 Mb mode) MII clock output The MAC uses the rising edge of this clock to synchronize **TXD** data.

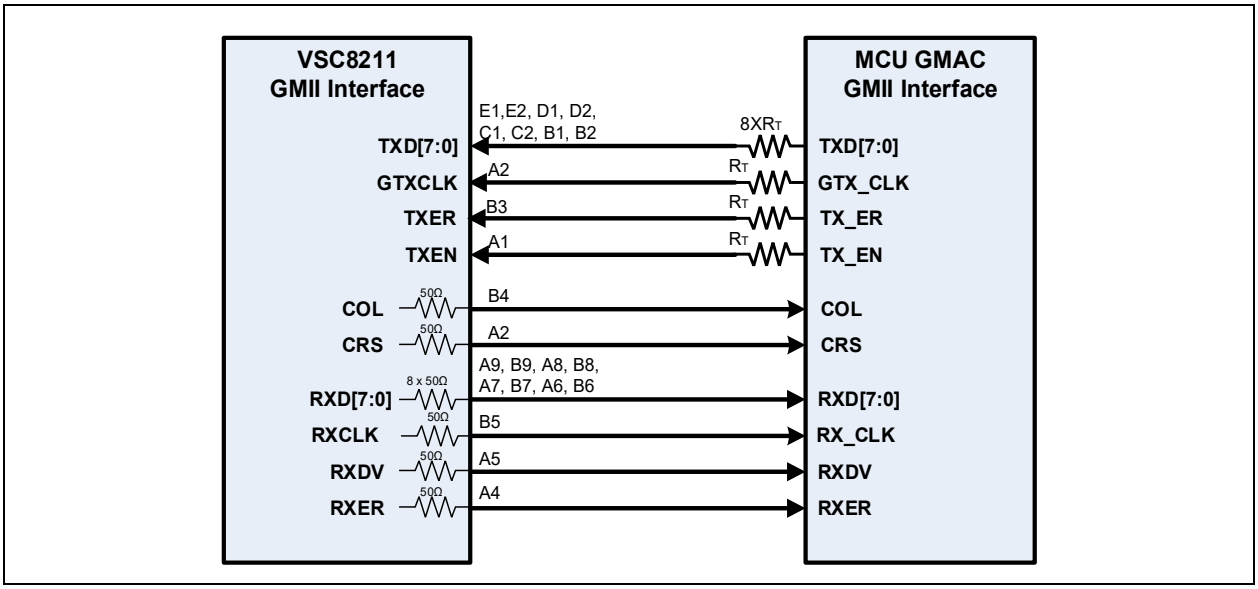
TABLE 6-1: GMII/RGMII/MII INTERFACE PINS

Pin Name	Pin Number	Type	Description
GTXCLK, TXC	A2	I	**Transmit Clock Input** (GMII mode) The transmit clock **GTXCLK** is a 125 MHz, +/–100 ppm reference clock used to synchronize the **TXD** data code group, **TXD [7:0]**, into the PHY. **Transmit Clock Input** (RGMII mode) The transmit clock **TXC** shall be either a 125 MHz or 25 MHz (for 1000 Mb or 100 Mb modes, respectively), with a +/–50 ppm tolerance.
TXER, TXCTL	B3	I	**TXER** – Transmit Error Input for **GMII** and **MII** **TXCTL** – Multiplexed transmit data valid for **RGMII** transmit control Input
TD [7:4], TD [3:0], TXD [3:0]	C1, C2, B1, B2	I	**TD [7:4] – RGMII** data input. Use the falling edge of **TXC**. **TD [3:0] – RGMII** data input. Use the rising edge of **TXC**. **TXD [3:0] – GMII/MII** data input. Use the rising edge of **GTXCLK.**
TXD [7:4]	E1, E2, D1, D2	I	Transmit Data Inputs (GMII mode) Transmit code-group data is input on these pins synchronously to the rising edge of **GTXCLK** in GMII mode.
TXEN	A1	I	Transmit Enable Input (GMII, MII modes) Synchronized to the rising edge of **GTXCLK** (1000 Mb mode) or **TXCLK** (100 Mb mode), this input indicates valid data is present on the **TXD** bus.

6.1.1 GMII INTERFACE

- The VSC8211 GMII interface supports 1000 Mbps only. GMII is used as an interface to a GMII-compatible MAC. The devices are compliant with the GMII interface specification when **VDDIOMAC** is operating at 3.3 V. The devices can also support the GMII interface at 2.5V.
- The GMII interface contains two distinct groups of signals—one is for transmission, and the other is for receiving. The VSC8211 GMII and MCU GMII connections are shown in Figure 6-1. Refer to Table 6-1 for the pin details.

FIGURE 6-1: CONNECTIONS BETWEEN VSC8211 GMII AND MCU GMII INTERFACE

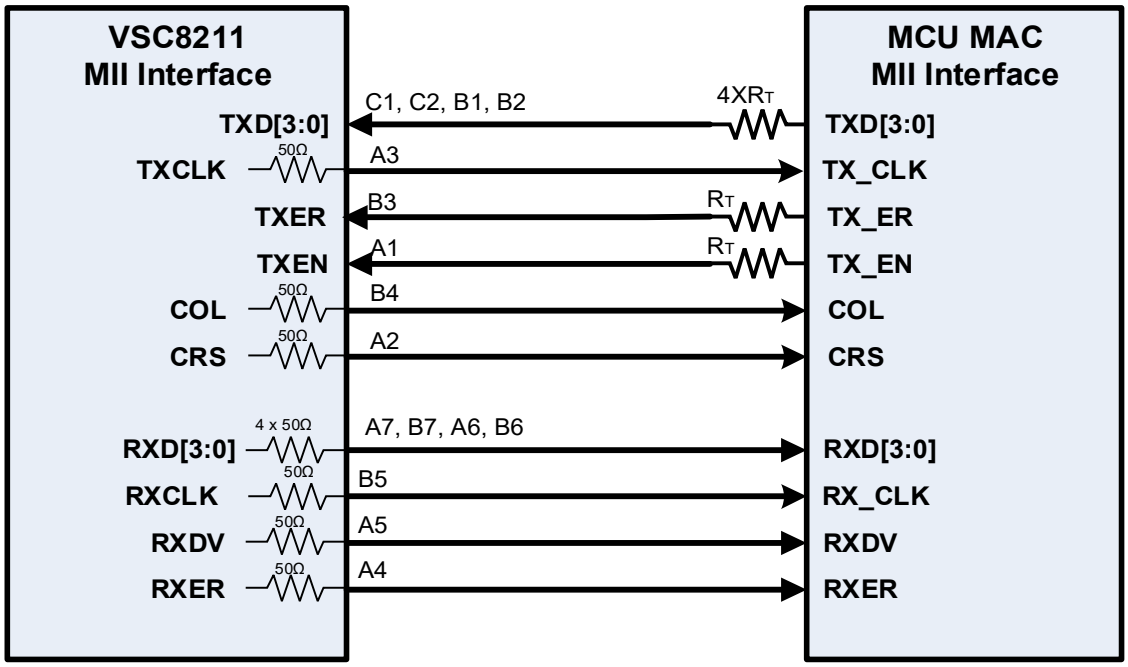


- VSC8211 GMII drive pins do not require external series termination resistors because they include internal 50Ω series termination resistors.
- Other-end GMII interface drive pins need external series termination resistor R_T if there are not enough internal 50Ω series termination resistors in GMAC GMII. It is recommended to use 22Ω to 33Ω for R_T or use the resistor value by using its IBIS model simulation result.

6.1.2 MII INTERFACE

- The MII interface supports all two speeds—10 Mbps and 100 Mbps. MII is used as an interface to an MII-compatible MAC. The devices are compliant with the MII interface specification. The devices can also support the MII interface at 3.3V or 2.5 V.
- The MII interface contains two distinct groups of signals—one for transmission and one for receiving. The VSC8211 MII and MCU MII connections are shown in Figure 6-2. Refer to Table 6-1 for the pin details.

FIGURE 6-2: CONNECTIONS BETWEEN VSC8211 MII AND MII MCU INTERFACE



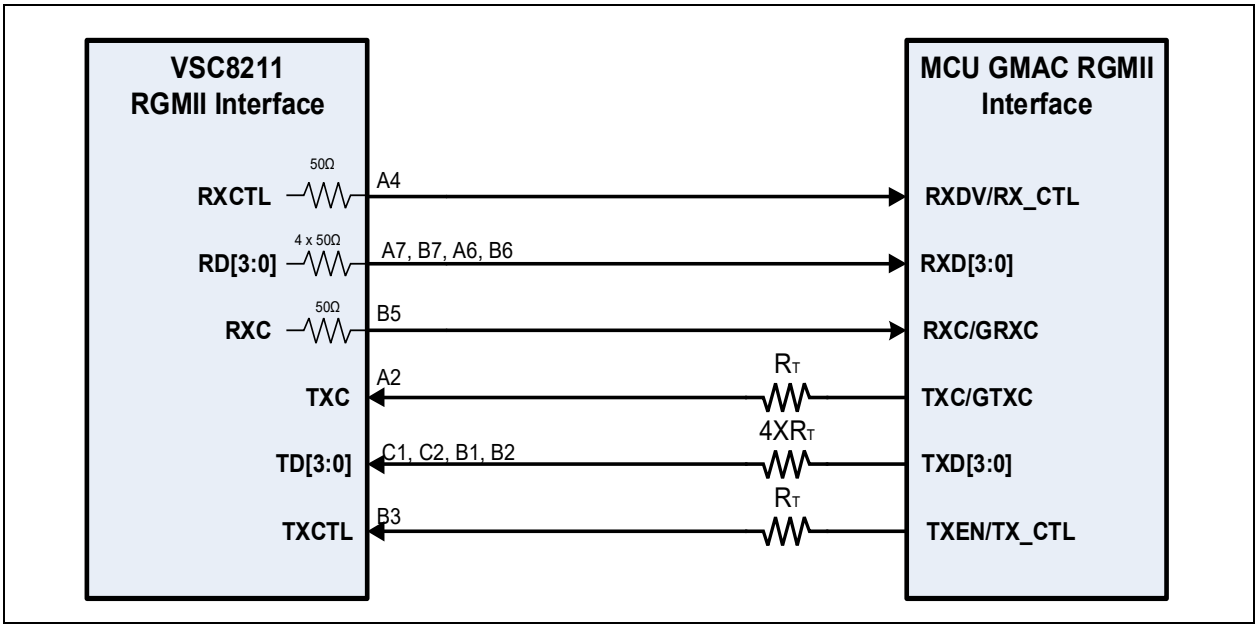
If MAC MII interface does not have a TX_ER pin, then VSC8211 TXER pin B3 should have a pull-down resistor to ground.

- The VSC8211 MII drive pins do not need external series termination resistors because they have internal 50Ω series termination resistors.
- Other-end MII interface drive pins need external series termination resistor R_T if there are not enough internal 50Ω series termination resistors in MAC MII. It is recommended to use 22Ω to 33Ω for R_T or use the resistor value by using its IBIS model simulation result.

6.1.3 RGMII INTERFACE CONNECTIONS

- The VSC8211 provides RGMII. The RGMII interface supports all three speeds 10 Mbps, 100 Mbps, and 1000 Mbps. The RGMII interface contains two distinct groups of signals—one for transmission and one for receiving.
- The VSC8211 device supports RGMII that is used as an interface to an RGMII-compatible MAC. The devices are compliant with the RGMII interface specification 2.0. The devices can also support the RGMII interface at 3.3V or 2.5 V.
- MCU GMAC RGMII should have the same speed and duplex as the VSC8211 RGMII interface. The VSC8211 RGMII interface connections with MCU RGMII are shown in Figure 6-3. Refer to Table 6-1 for the pin details.

FIGURE 6-3: CONNECTIONS BETWEEN VSC8211 MII AND RGMII MCU INTERFACE



6.1.4 TIMING CONSIDERATIONS FOR DESIGN WITH RGMII INTERFACE

- The VSC8211 supports RGMII V2.0 specifications. The RGMII interfaces need to meet a minimum of 1.0 ns and a maximum of 2.6 ns of data to input clock delay/skew in RGMII V2.0 specification by setting the Ingress Clock Delay and the Egress Clock Delay. The recommended VSC8211 RGMII data to input/output clock delay/skew setting principles are specified in Table 6-2.
- There are two ways to set RGMII data to input/output clock delay/skew. Designers may use either strap pin CMODE5 or the register 23 (17h) bits [11:8]. For using CMODE5 strapping, refer to Table 8-2 and Table 8-3.
- The VSC8211 RGMII register setting is based on other end RGMII clock input/output clock delay/skew and RGMII interface traces routing with equal length for two distinct groups of signals in the PCB layout.

TABLE 6-2: REFERENCE FOR RGMII STRAP PINS OR REGISTER CONFIGURATION

Case Number	VSC8211 Strap Pins CMODE5 Bits	VSC8211 RGMII Data to RXC and TXC Output and Input Delay/Skew	VSC8211 RGMII Setting Control Register 23 (17h)	VSC8211 RGMII Clock Delay/Skew Setting	Other End RGMII Data to RXC and TXC Output and Input Delay/Skew
1	CMODE5[1:0] =10 Receive 0.0 ns Delay	Data to Ingress Clock Input Skew (RGMII_TXC)	Bits [11:10] = 00 0.0 ns Delay	No Delay 0.0 ns	Data to Egress Clock Output Default is about 1.5 ns delay
	CMODE5[3:2] =10 Transmit 0.0 ns Delay	Data to Egress Clock Output Skew (RGMII_RXC)	Bits [9:8] = 00 0.0 ns Delay	No Delay 0.0 ns	Data to Ingress Clock Input Default is about 1.5 ns delay

Note 1: If other-end RGMII data to RXC output and data to TXC input delay is not 0.0 ns/0.2 ns (NO DELAY) as default or the DELAY is not 1.5 ns/1.7 ns as default, then there is a need to set the strap pin CMODE5 or the register 23 bits [11:8] to other values to meet the minimum 1.0 ns and maximum 2.6 ns specification in RGMII V2.0 for both VSC8211 and other-end RGMII data to clock input/output delay/skew.

TABLE 6-2: REFERENCE FOR RGMII STRAP PINS OR REGISTER CONFIGURATION

Case Number	VSC8211 Strap Pins CMODE5 Bits	VSC8211 RGMII Data to RXC and TXC Output and Input Delay/Skew	VSC8211 RGMII Setting Control Register 23 (17h)	VSC8211 RGMII Clock Delay/Skew Setting	Other End RGMII Data to RXC and TXC Output and Input Delay/Skew
2	CMODE5[1:0] =11 Receive 1.5 ns Delay	Data to Ingress Clock Input Skew (RGMII_TXC)	Bits [11:10] = 01 1.5 ns Delay	Suggest set to 1.5 ns delay (1 ns and 2.6 ns)	Data to Egress Clock Output Default is No delay 0.0 ns
	CMODE5[3:2] =11 Transmit 1.5 ns Delay	Data to Egress Clock Output Skew (RGMII_RXC)	Bits [9:8] = 01 1.5 ns Delay	Suggest set to 1.5 ns delay (1 ns and 2.6 ns)	Data to Ingress Clock Input Default is No delay 0.0 ns
3	CMODE5[1:0] =10 Receive 0.0 ns Delay	Data to Ingress Clock Input Skew (RGMII_TXC)	Bits [11:10] = 00 0.0 ns Delay	No Delay 0.0 ns	Data to Egress Clock Output Default is about 1.5 ns delay
	CMODE5[3:2] =11 Transmit 1.5 ns Delay	Data to Egress Clock Output Skew (RGMII_RXC)	Bits [9:8] = 01 1.5 ns Delay	Suggest set to 1.5 ns delay (1 ns and 2.6 ns)	Data to Ingress Clock Input Default is No delay 0.0 ns
4	CMODE5[1:0] =11 Receive 1.5 ns Delay	Data to Ingress Clock Input Skew (RGMII_TXC)	Bits [11:10] = 01 1.5 ns Delay	Suggest set to 1.5 ns delay (1 ns and 2.6 ns)	Data to Egress Clock Output Default is No delay 0.0 ns
	CMODE5[3:2] =10 Transmit 0.0 ns Delay	Data to Egress Clock Output Skew (RGMII_RXC)	Bits [9:8] = 00 0.0 ns Delay	No Delay 0.0 ns	Data to Ingress Clock Input Default is about 1.5 ns delay

Note 1: If other-end RGMII data to RXC output and data to TXC input delay is not 0.0 ns/0.2 ns (NO DELAY) as default or the DELAY is not 1.5 ns/1.7 ns as default, then there is a need to set the strap pin CMODE5 or the register 23 bits [11:8] to other values to meet the minimum 1.0 ns and maximum 2.6 ns specification in RGMII V2.0 for both VSC8211 and other-end RGMII data to clock input/output delay/skew.

6.2 TBI/RTBI Interface Pins

The VSC8211 supports TBI and RTBI interfaces. The TBI and RTBI support all three speeds—10 Mbps, 100 Mbps, and 1000 Mbps—and can be used to interface to other end devices with TBI and RTBI interfaces. See Table 6-3 for pin details.

TABLE 6-3: TBI/RTBI INTERFACE PINS

Pin Name	Pin Number	Type	Description
PMARXCLK0, RXC	B5	O	**PMA Receiver Clock 0 Output** – **PMARXCLK0** for TBI mode **Receive Clock Output** – **RXC** for RTBI modes Receive data is sourced from the PHY synchronous to the rising edge of **PMARXCLK0** in TBI modes or **RXC** in RTBI mode. This clock is recovered from the media.

TABLE 6-3: TBI/RTBI INTERFACE PINS

Pin Name	Pin Number	Type	Description
RX [9], RD [9], RD [4]	A4	O	**Receive Data Code Group**, bit [9] (TBI mode) Bit [9] of 10-bit parallel receive code-group data. When code groups are properly aligned, any received code group containing a comma is clocked by the rising edge of **PMARXCLK1**. **Multiplexed Receive Data Nibbles** (RTBI mode) The MAC synchronously inputs Bit [4] on the rising edge of **RXC**, and bit [9] (MSB) on the falling edge of **RXC**.
RD [8:5], RD [3:0], RX [3:0]	A7, B7, A6, B6	O	**RD [8:5]** – **RTBI** data output. Use the falling edge of **RXC**. **RD [3:0]** – **RTBI** data output. Use the rising edge of **RXC**. **RX [3:0]** – **TBI** data output. Use the rising edge of **PMARXCLK1**.
RX [7:4]	A9, B9, A8, B8	O	**Receive Data Code Group** (TBI mode) Receive data is driven out of the device synchronously to the rising edge of **PMARXCLK1**.
RX [8]	A5	O	**Receive Data Code Group**, bit [8] (TBI modes) Bit [8] of 10-bit parallel receive code-group data. When code groups are properly aligned, any received code group containing a comma is clocked by the rising edge of **PMARXCLK1**.
COMDET	C4	O	**Comma Detect Output** (TBI mode) A high on this signal indicates that the code-group associated with the current **PMARXCLK1** contains a valid comma. In TBI mode, the PHY detects and code-group-aligns to the comma+ bit sequence.
RXCLK125	B4	O	**Receiver Clock 125 MHz Output** (TBI mode) This signal behaves differently, depending on whether TBI Loopback mode is enabled: 1) When TBI Loopback mode is enabled, **RXCLK125** becomes one-half the frequency of the **GTXCLK** input clock from the protocol device (or MAC). 2) When no carrier is present on the media, this signal is the same as the device's free running output clock signal, **CLKOUTMAC**. 3) When a valid carrier is detected on the media, this output signal is the recovered clock from the TBI's data stream.
PMARXCLK1	A3	O	**PMA Receiver Clock 1 Output** (TBI mode) The protocol device (MAC) uses the rising edge of this 62.5 MHz receive clock to latch even-numbered code groups on the received PHY bit stream. **PMARXCLK1** is 180^{o} out-of-phase with **PMARX-CLK0**. This clock may be stretched during code-group alignment and is not shortened.

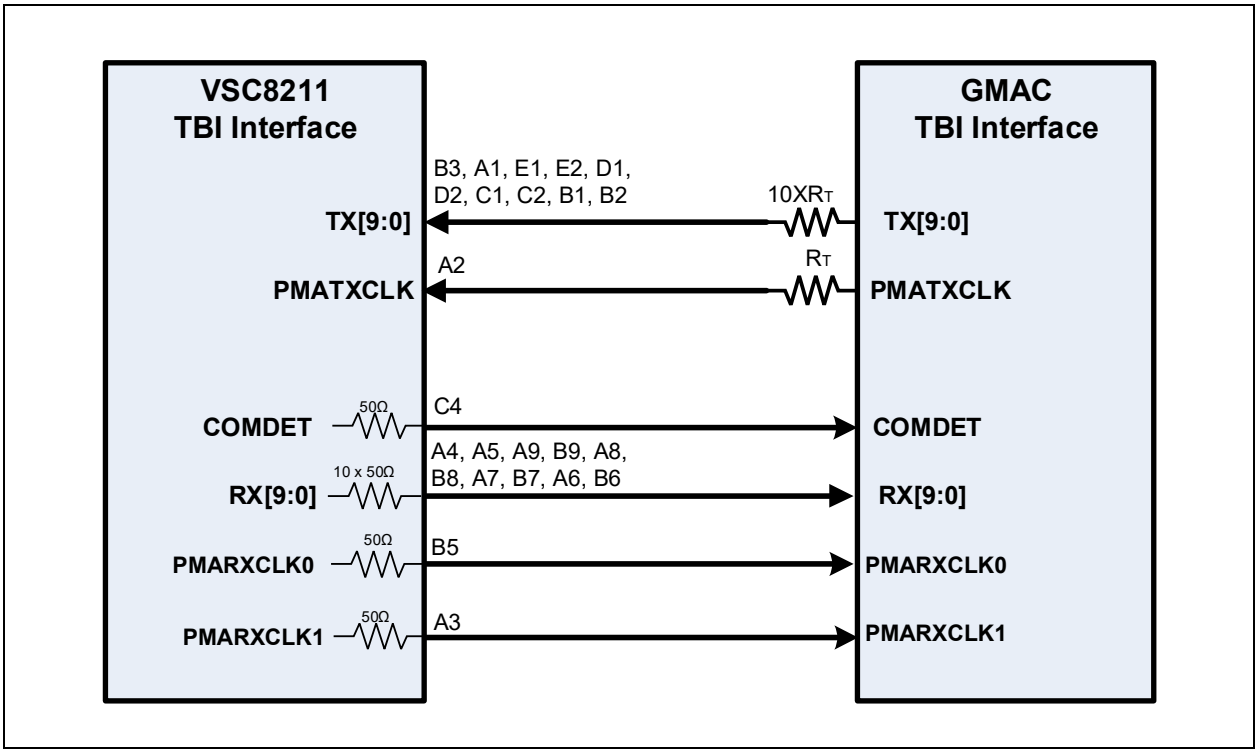
TABLE 6-3: TBI/RTBI INTERFACE PINS

Pin Name	Pin Number	Type	Description
PMATXCLK, TXC	A2	I	**PMA Transmit Code Group Clock Input** (TBI mode) 125 MHz transmit code-group clock **PMATXCLK**. This code-group clock is used to latch data into the PMA (in this case, the PHY) for transmission. **Transmit Clock Input** (RTBI mode) The transmit clock **TXC** shall be either a 125 MHz or 25 MHz (for 1000 Mb or 100 Mb modes, respectively), with a +/–50 ppm tolerance.
TX [9], TD [9], TD [4]	B3	I	**Transmit Data Input** (TBI mode) Transmit code-group data bit 9 **TX [9]** is input on this pin synchronously to the rising edge of **PMATXCLK** in TBI mode. **Multiplexed Transmit Data Input** (RTBI mode) Bit [4] TD [4] is synchronously input on the rising edge of **TXC**, and bit [9] TD [9] on the falling edge of **TXC**.
TX [3:0], TD [8:5], TD [3:0]	C1, C2, B1, B2	I	**Transmit Data Inputs** (TBI mode) Transmit code-group data is input on these pins **TX [3:0]** synchronously to the rising edge of **PMATXCLK** in TBI mode. **Multiplexed Transmit Data Nibbles** (RTBI mode) Bits [3:0] TD [3:0] are synchronously input on the rising edge of **TXC**, and bits [8:5] TD [8:5] on the falling edge of **TXC**.
TX [7:4]	E1, E2, D1, D2	I	**Transmit Data Inputs** (TBI mode) Transmit code-group data is input on these pins **TX [7:4]** synchronously to the rising edge of **PMATXCLK** in TBI mode.
TX [8]	A1	I	**Transmit Data Input** (TBI mode) Transmit code-group data bit 8 is input on this pin **TX** [8] synchronously to the rising edge of **PMATXCLK** in TBI mode.

6.2.1 TBI INTERFACE

- The TBI interface supports the speeds of 1000 Mbps. TBI is used as an interface to a TBI-compatible MAC. The devices are compliant with the TBI interface specification when **VDDIOMAC** is operating at 3.3 V. The devices can also support the TBI interface at 2.5 V.
- The TBI interface contains two distinct groups of signals—one for transmission and one for receiving. The VSC8211 TBI and GMAC TBI connections are shown in Figure 6-4. Refer to Table 6-3 with detailed pin descriptions for the TBI interface.

FIGURE 6-4: CONNECTIONS BETWEEN VSC8211 TBI AND A GMAC TBI INTERFACE



- VSC8211 TBI drive pins do not need external series termination resistors because they have internal 50Ω series termination resistors.
- Other-end TBI interface drive pins need external series termination resistor R_T if there are no internal enough 50Ω series termination resistors in GMAC TBI. It is recommended to use 22Ω to 33Ω for R_T or use the resistor value with its IBIS model simulation result.

6.2.2 RTBI INTERFACE CONNECTIONS

- The VSC8211 provides RTBI. The RTBI interface supports all three speeds—10 Mbps, 100 Mbps, and 1000 Mbps. The RTBI interface contains two distinct groups of signals—one for transmission and one for receiving.
- The VSC8211 device supports RTBI that is used as an interface to a RTBI-compatible MAC. The devices are compliant with the RTBI interface specification 2.0. The devices can also support the RTBI interface at 3.3V or 2.5V.
- GMAC RTBI should have the same speed and duplex as the VSC8211 RTBI interface. The VSC8211 RTBI interface connections with GMAC RTBI are shown in Figure 6-5 and Figure 6-6. Refer to Table 6-3 for the detailed pin descriptions for the RTBI interface.

FIGURE 6-5: CONNECTIONS BETWEEN VSC8211 RTBI AND GMAC RTBI FOR USING CLOCK RISING EDGE

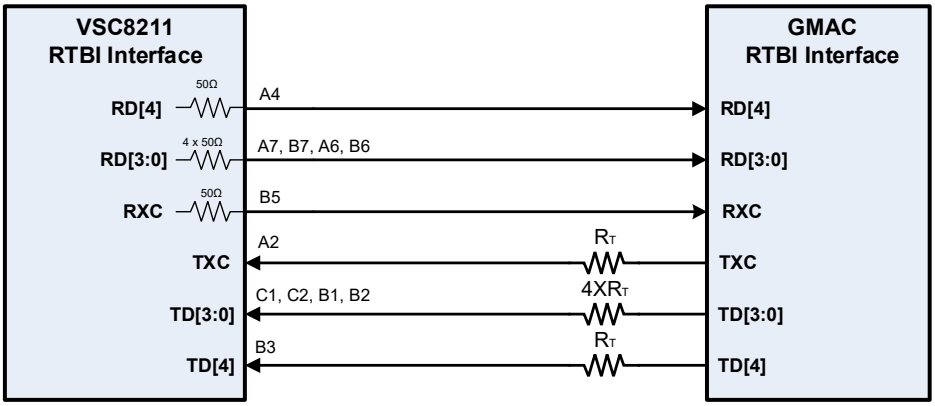
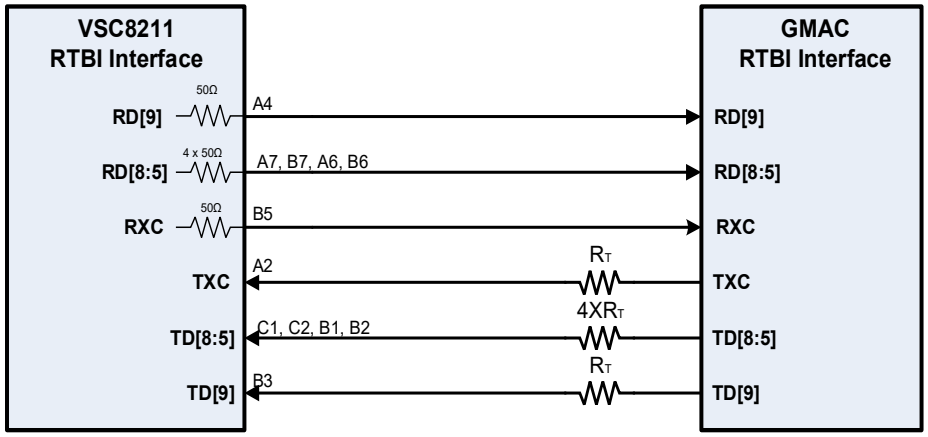


FIGURE 6-6: CONNECTIONS BETWEEN VSC8211 RTBI AND GMAC RTBI FOR USING CLOCK FALLING EDGE



6.2.3 TIMING CONSIDERATIONS FOR DESIGN WITH RTBI INTERFACE

- The VSC8211 supports RTBI V2.0 specifications. The RTBI interfaces need to meet the minimum 1.0 ns and maximum 2.6 ns of data to input clock delay/skew in RGMII/RTBI V2.0 specification. This can be achieved by setting the Ingress Clock Delay and the Egress Clock Delay. The VSC8211 RTBI data to input/output clock delay/skew setting principles are detailed in Table 6-4.
- There are two ways to set RTBI data to input/output clock delay/skew. Designers may use either the strap pin CMODE5 or the register 23 (17h) bits [11:8]. Refer refer to Table 8-2 and Table 8-3 when using the CMODE5 strapping.
- VSC8211RTBI register setting is based on other end RTBI clock input/output clock delay/skew and RTBI interface traces routing with equal length for two distinct groups of signals in the PCB layout.

TABLE 6-4: REFERENCE FOR RTBI STRAP PINS OR REGISTER CONFIGURATION

Case Number	VSC8211 Strap Pins CMODE5 Bits	VSC8211 RTBI Data to RXC and TXC Output and Input Delay/Skew	VSC8211 RTBI Setting Control Register 23 (17h)	VSC8211 RTBI Clock Delay/Skew Setting	Other End RTBI Data to RXC and TXC Output and Input Delay/Skew
1	CMODE5[1:0] =10 Receive 0.0 ns Delay	Data to Ingress Clock Input Skew (RTBI_TXC)	Bits [11:10] = 00 0.0 ns Delay	No Delay 0.0 ns	Data to Egress Clock Output Default is about 1.5 ns delay
	CMODE5[3:2] =10 Transmit 0.0 ns Delay	Data to Egress Clock Output Skew (RTBI_RXC)	Bits [9:8] = 00 0.0 ns Delay	No Delay 0.0 ns	Data to Ingress Clock Input Default is about 1.5 ns delay
2	CMODE5[1:0] =11 Receive 1.5 ns Delay	Data to Ingress Clock Input Skew (RTBI_TXC)	Bits [11:10] = 01 1.5 ns Delay	Suggest set to 1.5 ns delay (1 ns and 2.6 ns)	Data to Egress Clock Output Default is No delay 0.0 ns
	CMODE5[3:2] =11 Transmit 1.5 ns Delay	Data to Egress Clock Output Skew (RTBI_RXC)	Bits [9:8] = 01 1.5 ns Delay	Suggest set to 1.5 ns delay (1 ns and 2.6 ns)	Data to Ingress Clock Input Default is No delay 0.0 ns
3	CMODE5[1:0] =10 Receive 0.0 ns Delay	Data to Ingress Clock Input Skew (RTBI_TXC)	Bits [11:10] = 00 0.0 ns Delay	No Delay 0.0 ns	Data to Egress Clock Output Default is about 1.5 ns delay
	CMODE5[3:2] =11 Transmit 1.5 ns Delay	Data to Egress Clock Output Skew (RTBI_RXC)	Bits [9:8] = 01 1.5 ns Delay	Suggest set to 1.5 ns delay (1 ns and 2.6 ns)	Data to Ingress Clock Input Default is No delay 0.0 ns
4	CMODE5[1:0] =11 Receive 1.5 ns Delay	Data to Ingress Clock Input Skew (RTBI_TXC)	Bits [11:10] = 01 1.5 ns Delay	Suggest set to 1.5 ns delay (1 ns and 2.6 ns)	Data to Egress Clock Output Default is No delay 0.0 ns
	CMODE5[3:2] =10 Transmit 0.0 ns Delay	Data to Egress Clock Output Skew (RTBI_RXC)	Bits [9:8] = 00 0.0 ns Delay	No Delay 0.0 ns	Data to Ingress Clock Input Default is about 1.5 ns delay

Note 1: If other-end RTBI data to RXC output and data to TXC input delay is not 0.0 ns to 0.2 ns (NO DELAY) as default or the DELAY is not 1.5 ns to 1.7 ns as default, then there is a need to set the strap pin CMODE5 or the register 23 bits [11:8] to other values to meet the minimum 1.0 ns and the maximum 2.6 ns specification in RGMII/RTBI V2.0 for both VSC8211 and other-end RTBI data to clock input/output delay/skew.

6.3 GMII/RGMII/MII and TBI/RTBI Interface Series Terminations

- Provisions should be made for series resistors for all outputs on the GMII/RGMII/MII and TBI/RTBI interfaces. Series resistors will enable designers to closely match the output driver impedance of the device and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application-dependent and must be analyzed in-system.
- VSC8211 GMII/RGMII/MII and TBI/RTBI drive pins do not need external series termination resistors because they have internal 50Ω series termination resistors.
- Other-end GMII/RGMII/MII and TBI/RTBI interface drive pins need external series termination resistor R_T if there are not enough internal 50Ω series termination resistors in the drive pins of their GMII/RGMII/MII and TBI/RTBI. It is recommended to use 22Ω to 33Ω for R_T or use the resistor value by using its IBIS model simulation result.
- The series resistors should be placed as close as possible to the other-end device drive pins in PCB layout.
- The unused pins of the interfaces should be unconnected except unused **I/O** pin without internal pull-up or pull-down.

7.0 DEVICE CLOCKS

7.1 Reference Clock

- The device reference clock supports both 25 MHz and 125 MHz clock signals.
- Refer to Table 7-1 for pin details. For information on reference circuit connection, see Figure 7-1, Figure 7-2, and Figure 7-3.

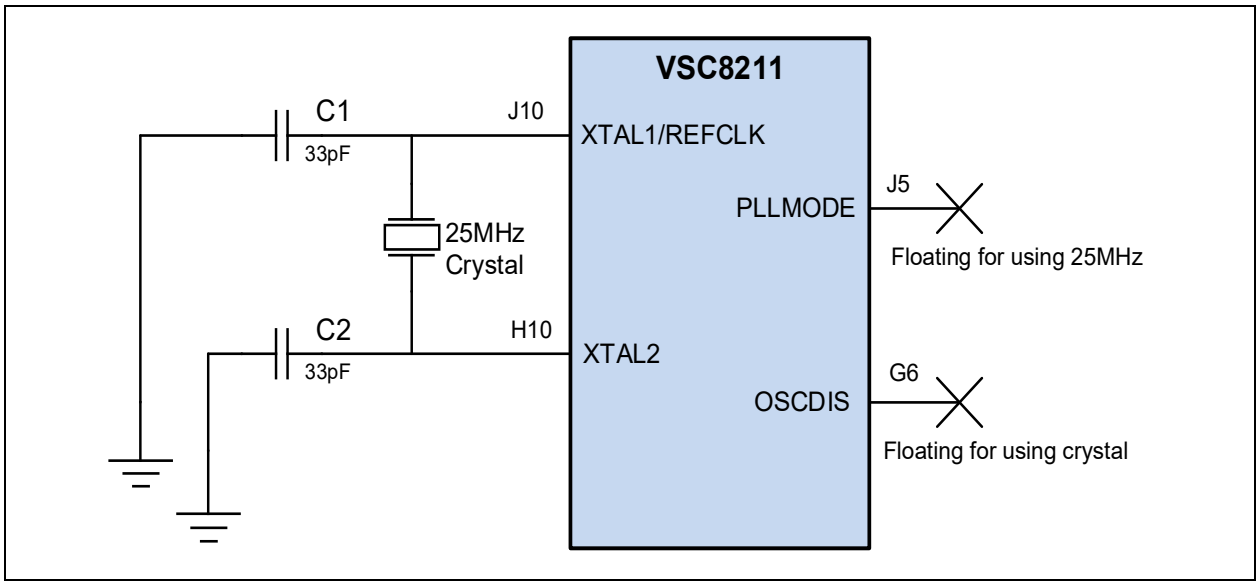
TABLE 7-1: REFERENCE CLOCK RELATED PINS

Pin Name	Pin Number	Type	Description
XTAL1/REFCLK	J10	I	**XTAL1/REFCLK –** Crystal or Oscillator Input **XTAL1** is used as 25 MHz crystal circuit input. **REFCLK** is used as 25 MHz or 125 MHz oscillator clock input.
XTAL2	H10	O	**XTAL2 Crystal Output** **XTAL2** is used for 25 MHz crystal circuit output.
EECLK/**PLLMODE**	J5	O, IPD	**PLLMODE** – PLL Mode Select Input 0 = When low (default), a reference clock of 25 MHz is expected at the **REFCLK** pin from either a 25 MHz crystal or a 25 MHz oscillator. 1 = When **PLLMODE** is high, the PHY expects a 125 MHz clock input as the PHY's reference clock.
CLKOUTMICRO/$\overline{\textit{OSCDIS}}$	G6	O, IPU	**CLKOUTMICRO** – Clock Output This is a 4 MHz (default) or a 125 MHz output clock depending on the value of Extended MII Register 20E.8. The clock output frequency can be set at startup by hardware configuration of **CMODE6** pin. The voltage levels of the clock are based on the **VDDIOMICRO** power supply. $\overline{\textit{OSCDIS}}$ **– Active Low on-chip Oscillator Disable Input** 1 = When high (default), the PHY enables the internal on-chip oscillator allowing operation with a 25 MHz crystal by using **XTAL1** and **XTAL2**. 0 = When low, the PHY's oscillator is turned off and the PHY must be supplied with an external 25 MHz or 125 MHz oscillator clock on the **REFCLK** pin.

7.2 25 MHz Crystal Circuit

The **OSCDIS** strap pin should be high (default). A 25 MHz parallel resonant crystal with a +/–50 ppm frequency tolerance should be connected between **XTAL1** and **XTAL2** pins. Each pin requires a capacitor to ground directly when a crystal is used. Since every system is unique, the capacitor values are system independent based on the C_L specifications of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. For more information on this topic, refer to the article titled, *Calculating Crystal Load Capacitor* at microchip-support.force.com. The **PLLMODE** pin should be left floating (or pulled low) when using 25 MHz clock frequency. See Figure 7-1 for details.

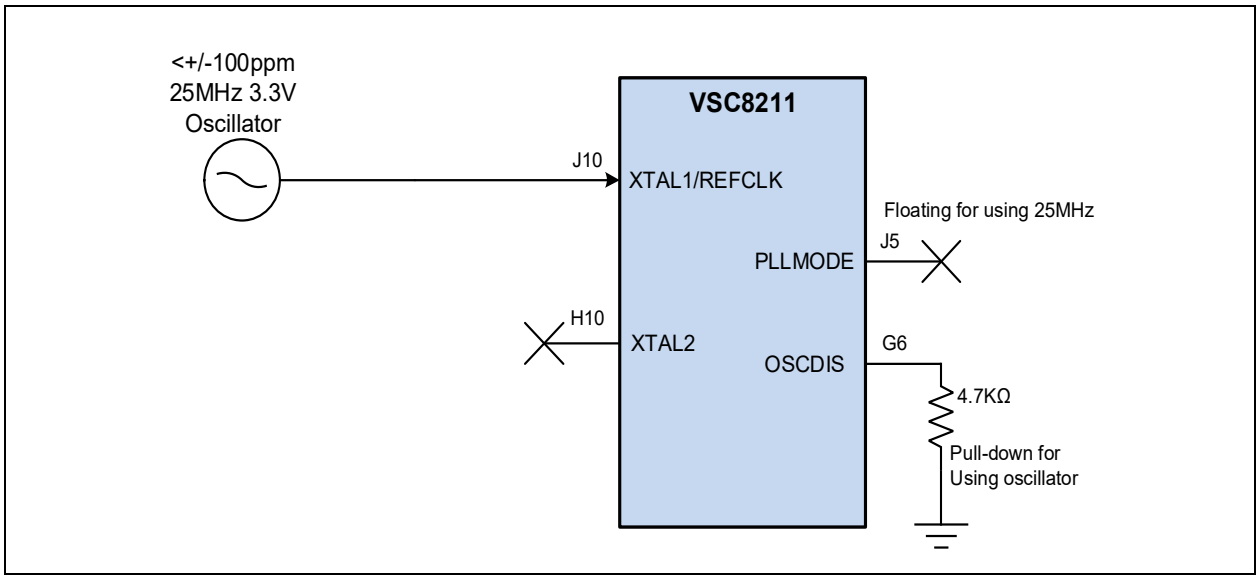
FIGURE 7-1: 25 MHZ CRYSTAL CIRCUIT AND CONFIGURATION



7.3 25 MHz Oscillator Circuit

To use a single-ended reference clock from a 25 MHz oscillator, refer to the configurations for a single-ended **REFCLK** in Figure 7-2. The **PLLMODE** pin should be left floating (or pulled low) on Reset for using 25 MHz clock frequency. The ***OSCDIS*** pin should have an external pull-down resistor for using an oscillator.

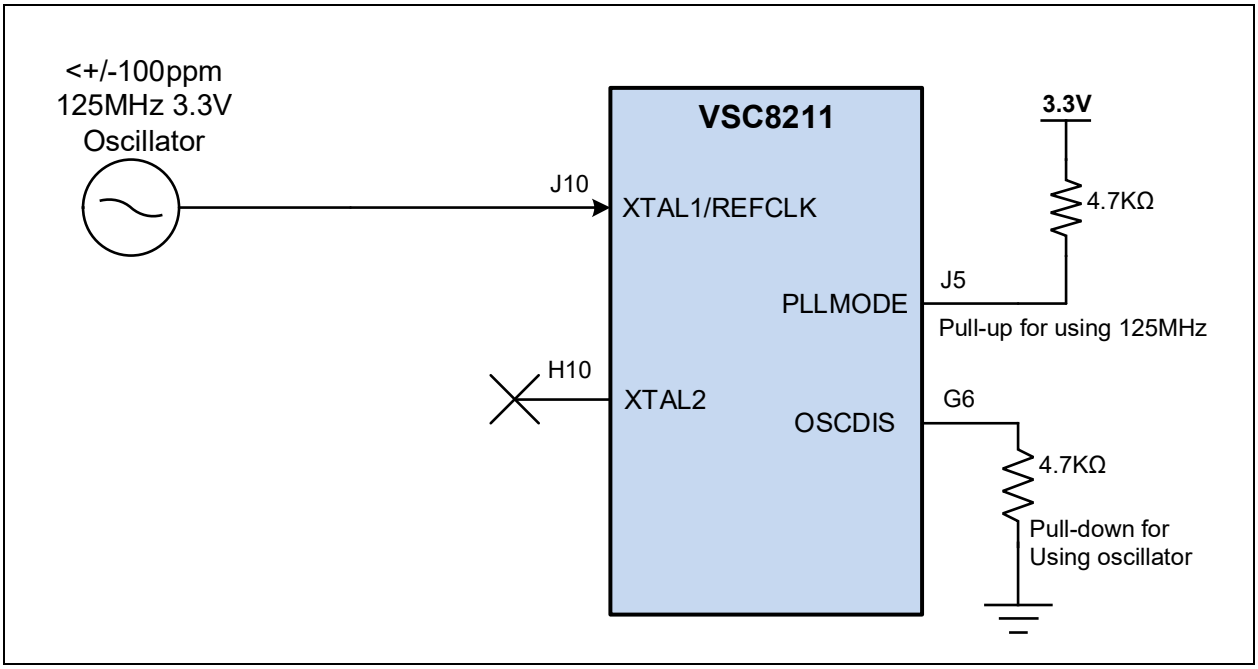
FIGURE 7-2: 25 MHZ OSCILLATOR CIRCUIT AND CONFIGURATION



7.4 125 MHz Oscillator Circuit

To use a single-ended reference clock from a 125 MHz oscillator, refer to the configurations for a single-ended **REFCLK** in Figure 7-3. The **PLLMODE** pin should be high with a pull-up resistor on Reset for using 125 MHz clock frequency. The ***OSCDIS*** pin should have an external pull-down resistor for using an oscillator.

FIGURE 7-3: 125 MHZ OSCILLATOR CIRCUIT AND CONFIGURATION



8.0 HARDWARE CONFIGURATION USING CMODE PINS

8.1 CMODE Pin Description

- Each of the four **CMODE** pins (CMODE [3:0]) is used to latch a four-bit value at PHY Reset. A total of 16 CMODE configuration bits are set at Reset based on pull-down and pull-up resistors values. Each CMODE bit represents the default value of a particular PHY register bit and therefore sets a default PHY operating condition at startup. See Table 8-1 for pin details.

TABLE 8-1: CMODE PINS

Pin Name	Pin Number	Type	Description
CMODE0	F11	I	Pull up/down different resistor values to get a different CMODE0[3:0] value
CMODE1	G11	I	Pull up/down different resistor values to get a different CMODE1[3:0] value
CMODE2	E11	I	Pull up/down different resistor values to get a different CMODE2[3:0] value
CMODE3	E12	I	Pull up/down different resistor values to get a different CMODE3[3:0] value
CMODE4	E13	I	Pull up/down different resistor values to get a different CMODE4[3:0] value
CMODE5	D13	I	Pull up/down different resistor values to get a different CMODE5[3:0] value
CMODE6	D12	I	Pull up/down different resistor values to get a different CMODE6[3:0] value
CMODE7	D1	I	Pull up/down different resistor values to get a different CMODE7[3:0] value

8.2 Select Mode Pins Pull-Up and Pull-Down Resistor Value for System Design

- The CMODE bits are set by connecting each **CMODE** pin to either **VDD33A** or **VSS** (ground) through an external 1% resistor. The four-bit value latched by the PHY on each **CMODE** pin depends upon the value of the resistor used to pull up or pull down the **CMODE** pin. CMODE resistor values and connections are defined in Table 8-2.

TABLE 8-2: CMODE PIN PULL-UP /PULL-DOWN RESISTOR VALUE VS. CMODE BIT VALUES

CMODE Pin Pull-Down Resistor Values (kΩ)	CMODE Pin Pull-Up Resistor Values (kΩ)	CMODEx [3:0] Values (X = 0,1,2... 7)	CMODE [7:0] Pins Bit [3]	CMODE [7:0] Pins Bit [2]	CMODE [7:0] Pins Bit [1]	CMODE [7:0] Pins Bit [0]
0	—	0000	0	0	0	0
2.26	—	0001	0	0	0	1
4.02	—	0010	0	0	1	0
5.90	—	0011	0	0	1	1
8.25	—	0100	0	1	0	0
12.1	—	0101	0	1	0	1
16.9	—	0110	0	1	1	0
22.6	—	0111	0	1	1	1
—	0	1000	1	0	0	0
—	2.26	1001	1	0	0	1
—	4.02	1010	1	0	1	0
—	5.90	1011	1	0	1	1
—	8.25	1100	1	1	0	0
—	12.1	1101	1	1	0	1
—	16.9	1110	1	1	1	0
—	22.6	1111	1	1	1	1

8.3 CMODE Bits

Table 8-3 outlines the mapping of each CMODE bit to a PHY operating condition parameter. Each of the PHY operating condition parameters is described in detail in Table 8-3 and Table 8-4.

TABLE 8-3: CMODE PINS AND BIT OPERATION CONDITION PARAMETER DESCRIPTIONS

CMODE Pin Name	Description for Every Bit of each CMODE Pin			
	Bit [3]	**Bit [2]**	**Bit [1]**	**Bit [0]**
CMODE0	PHY Address [3]	PHY Address [2]	PHY Address [1]	PHY Address [0]
CMODE1	SFP Mode Disable 0: See Table 8-4 for details. 1: See Table 8-4 for details.	PHY Address [4]	SIGDET pin direction 0: Input 1: Output	SerDes line impedance 0: 50Ω 1: 75Ω
CMODE2	PHY Operating Mode [3]	PHY Operating Mode [2]	PHY Operating Mode [1]	PHY Operating Mode [0]
CMODE3	LED Control [1] See Table 8-4 for LED Control [1:0].	SQE Enable 0: SQE Disable (default) 1: SQE Enable (10BT Half-Duplex mode only)	10Base-T-Echo On 0: Disabled 1: Enabled	Auto-Negotiation Advertisement Control [1] See Table 8-4 for details on Auto-Negotiation Advertisement Control [1:0].
CMODE4	LED Control [0] See Table 8-4 for detail of LED Control [1:0]	Pulsing Enable 0: LED pulsing disabled 1: Enable 5 KHz, 20% duty cycle LED pulsing for power savings	Auto-negotiation Advertisement Control [0] See Table 8-4 for Auto-Negotiation Advertisement Control [1:0] details	MII Register View 0: For 1000Base-T device 1: For 1000Base-X device
CMODE5	RGMII/RTBI Transmit Path Timing compensation [1]	RGMII/RTBI transmit path Timing compensation [0]	RGMII/RTBI Receive path Timing compensation [1]	RGMII/RTBI Receive path Timing compensation [0]
	CMODE5 [3:2] 00: 2.0 ns 01: 2.5 ns 10: 0.0 ns (No delay/skew) 11: 1.5 ns		CMODE5 [1:0] 00: 2.0 ns 01: 2.5 ns 10: 0.0 ns (No delay/skew) 11: 1.5 ns	
CMODE6	PICMG Miser Mode Enable 0: Disabled 1: Enabled	SIGDET pin Polarity 0: Active High 1: Active Low	Enhanced ActiPHY™ Enable 0: Disabled 1: Enabled	CLKOUTMICRO Frequency 0: 4 MHz 1: 125 MHz
CMODE7	Linkxxxx/Act Behavior 1: Link function indicated link status only. 0: All link function blinks or flashes when activity is present.	Link Speed Auto-Downshift Enable 0: Disabled 1: Enabled	Flow Control [1]	Flow Control [0]
			Flow Control [1:0]: 00: Asymmetric Pause capable 01: Symmetric Pause capable 10:100BASE-TX FDX capable 11:100BASE-TX HDX capable	

TABLE 8-4: OTHER OPERATION CONDITION PARAMETER DESCRIPTIONS

Name	CMODE Pin Name and Bit Position	CMODE Bit Value	Description
PHY Address [4:0]	CMODE1[2] + CMODE0 [3:0]	31-0	Sets the PHY Address used to access PHY Registers when the PHY's SMI is in IEEE mode.
PHY Operating Mode [3:0]	CMODE2 [3:0]	The value latched is reflected in the MII Register 23. 15:12 + 2:1.	
		0000	802.3z SerDes to CAT5 Media, MAC interface Clause 37 auto-negotiation auto-sense enabled
		0001	RGMII with Copper/Fiber Auto Media Sense (Fiber Preference)
		0010	GMII to Fiber
		0011	GMII/MII with Copper/Fiber Auto Media Sense (Fiber Preference)
		0100	802.3z SerDes to CAT5 Media, Clause 37 disabled
		0101	SGMII to CAT5 Media, SCLK enabled
		0110	RGMII to CAT5 Media
		0111	RGMII to Fiber Media
		1000	GMII/MII to CAT5 Media
		1001	TBI to CAT5 Media, Clause 37 auto-negotiation auto-sense enabled
		1010	802.3z SerDes to CAT5 Media, Media Converter mode
		1011	TBI to Fiber Media
		1100	RTBI to CAT5 Media, Clause 37 auto-negotiation auto-sense enabled
		1101	Serial MAC to Fiber Media, SCLK enabled
		1110	802.3z SerDes to CAT5 Media, Clause 37 enabled
		1111	SGMII to CAT5 Media, SCLK disabled

TABLE 8-4: OTHER OPERATION CONDITION PARAMETER DESCRIPTIONS (CONTINUED)

Name	CMODE Pin Name and Bit Position	CMODE Bit Value	Description
SFP Mode Disable	CMODE1[3]	This CMODE bit sets the default value of MII Register 21E.15.	
		0	This sets MII Register 21E.15 = 1. Sets the following PHY defaults: a) **TXDIS/$\overline{\text{SRESET}}$** is active-high and behaves like **TXDIS**. b) **MODDEF0/CLKOUT** pin functions like **MODDEF0**. This pin is asserted low by the PHY once the EEPROM interface is released for access through the SMI. c) **RXLOS/SIGDET** pin functions like the **RXLOS**. d) The SMI interface is set in MSA mode.
		1	This sets MII Register 21E.15 = 0. Sets the following PHY defaults: a) **TXDIS/$\overline{\text{SRESET}}$** is active-low and behaves like **$\overline{\text{SRESET}}$**. b) **MODDEF0/CLKOUT** pin functions like **CLKOUT** and drives out a 125 MHz clock. c) **RXLOS/SIGDET** pin functions like the **SIGDET**. d) The SMI interface is set in IEEE mode.
LED Control [1:0]	CMODE3[3], CMODE4[3]	This sets the default behavior of LED pins LED [2:0] by setting the startup values of MII Register Bit Register 27 (1Bh) – LED Control Register.	
		00	LED [4:0] = {Duplex/Collision, Link/Activity, Link10/Activity, Link100/Activity, Link1000/Activity} (MII Reg 27 = 0000h)
		01	LED [4:0] = {Activity, Duplex/Collision, Duplex/Collision, Link10/100/Activity, Link/Activity} (MII Reg 27 = 5540h)
		10	LED [4:0] = {Link Fault, Fiber Media Selected, Link/Activity, Link/Activity, Fault} (MII Reg 27 = AA80h)
		11	LED [4:0] = {Tx, Rx, Tx, Link100/1000/Activity, Rx} (MII Reg 27 =FFC0h)
Auto-Negotiation Advertisement Control [1:0]]	CMODE3[0], CMODE4[1]	These CMODE bits set the default auto-negotiation advertisement by setting the initial values of MII Registers 4 and 9.	
		00	10/100/1000BASE-T HDX, 10/100/1000BASE-T FDX
		01	10/100BASE-T HDX, 10/100/1000BASE-T FDX
		10	10/100BASE-T HDX, 10/100BASE-T FDX
		11	1000BASE-T FDX

9.0 DIGITAL INTERFACE

9.1 Dual-Mode Serial Management Interface (SMI)

- The Serial Management Interface provides access to the PHY registers for device configuration and status information. It also provides access to the EEPROM connected to the **EEDAT** and **EECLK** pins (EEPROM interface) of the PHY. For details on EEPROM access through the SMI, refer to Table 9-1. There are dual modes of MSA and IEEE by setting the MII register 21E.15 at startup. For MSA mode-related and IEEE mode-related pins and settings, see Table 9-2 and Table 9-3.
- The **MODDEF1/MDC**, **MODDEF2/MDIO**, and **MDINT** pins comprise the SMI. See Table 9-1 for details on SMI pin descriptions.

TABLE 9-1: SMI PINS

Pin Name	Pin Number	Type	Description
MODDEF1/ MDC	H3	I	The functionality of this pin is determined by the value of MII register 21E.15 'SFP MODE' set at startup using CMODE hardware configuration or via the EEPROM interface.
MODDEF2/ MDIO	G4	I/O	The functionality of this pin is determined by the value of MII register 21E.15 'SFP MODE' set at startup using CMODE hardware configuration or via the EEPROM interface.
MDINT	H4	OD	**Management Data Interrupt** **MDINT** is asserted whenever there is a change in the operating status of the device. This open-drain signal indicates a change in the PHY's link operating conditions for which a station manager must interrogate to determine further information.

9.1.1 PHY REGISTER ACCESS WITH SMI IN MSA MODE

- In this mode, the PHY registers are accessed using the standard MSA-compliant protocol. This protocol is generally used for reading and writing to Microchip's AT24 series-compatible EEPROMs.
- In this SMI in MSA mode, the SMI pin functions are described in Table 9-2. Refer to the table for the pin numbers and additional information on SMI MSA mode.

TABLE 9-2: SMI PINS FOR MSA MODE

Pin Name	Pin Number	Type	Description
MODDEF1	H3	I	**MODDEF1 – Serial MSA Clock (Set CMODE1[3]=0 in SFP Mode or set MII Register 21E.15=1)** **MODDEF1** is the clock input of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM interface using the protocol specified in the MSA specification. Although typically operated at 100 kHz, MODDEF1 can be operated at a maximum of 1 MHz.
MODDEF2	G4	I/O	**MODDEF2 – Serial I/O Data (Set CMODE1[3]=0 in SFP Mode or set MII Register 21E.15=1)** **MODDEF2** is the data line of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM interface using the protocol specified in the MSA specification. This pin normally requires a 1.5 kΩ to 4.7 kΩ pull-up resistor to **VDDIOMICRO** at the station manager. The value of the pull-up resistor depends on the MODDEF1 frequency and the capacitive load on the MODDEF2 line.

TABLE 9-2: SMI PINS FOR MSA MODE (CONTINUED)

Pin Name	Pin Number	Type	Description
MDINT	H4	OD	**Management Data Interrupt** The assertion polarity of **MDINT** is determined by the presence of a pull-up or pulldown on the **MDINT** pin. If the **MDINT** pin is pulled up to **VDDIOMICRO** using a 4.7 kΩ to 10 kΩ resistor, it becomes an active-low signal. If the **MDINT** pin is pulled down using a 4.7 kΩ to 10 kΩ resistor, then it becomes an active-high signal.

9.1.2 PHY REGISTER ACCESS WITH SMI IN IEEE MODE

- In IEEE mode, the SMI is fully compliant with the IEEE 802.3-2000 MII specifications.
- In this SMI with IEEE mode, the SMI pin functions are described as follows. Refer to Table 9-3 for the pin numbers and more information in SMI IEEE mode.

TABLE 9-3: SMI PINS FOR IEEE MODE

Pin Name	Pin Number	Type	Description
MDC	H3	I	**MDC – Management Data Clock (Set CMODE1 [3]=1 in IEEE Mode or set MII Register 21E.15=0)** **MDC** is the clock input of the two wires serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM interface using the Serial Management Interface protocol specified in the IEEE 802.3 specification. Although typically operated at less than 100 kHz due to frequency limitations of the EEPROM used with the PHY, the PHY registers can be accessed at a maximum frequency of 1 MHz.
MDIO	G4	I/O	**MDIO – Serial I/O Data (Set CMODE1[3]=1 in IEEE Mode or set MII Register 21E.15=0)** **MDIO** is the data line of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM interface using the Serial Management Interface protocol specified in the IEEE 802.3 specification. This pin usually requires a 1.5 kΩ to 4.7 kΩ pull-up resistor to **VDDIOMICRO** at the station manager. The value of the pull-up resistor depends on the MDC frequency and the capacitive load on the MDIO line.
MDINT	H4	OD	**Management Data Interrupt** The assertion polarity of **MDINT** is determined by the presence of a pull-up or pull-down on the **MDINT** pin. If the **MDINT** pin is pulled up to **VDDIOMICRO** using a 4.7 kΩ to 10 kΩ resistor, it becomes an active-low signal. If the **MDINT** pin is pulled down using a 4.7 kΩ to 10 kΩ resistor, then it becomes an active-high signal.

9.2 EEPROM Interface

- The EEPROM interface consists of the **EEDAT** and **EECLK** pins of the PHY. If this interface is used, these pins should connect to the **SDA** and **SCL** pins, respectively, of a serial EEPROM that is compatible with the AT24 series of Microchip EEPROMs. The EEPROM interface on the VSC8211 serves the following purposes:
  - It provides the PHY with the ability to configure its self-internal registers.
  - The system manager can access the EEPROM to obtain information pertaining to the system or module configuration.
  - A single EEPROM can be shared among multiple PHYs for their custom configuration.
- The PHY detects the EEPROM based on the presence of a pull-up on the **EEDAT** pin. It is initialized using the configuration EEPROM (if present) under the three conditions: (1) **RESET** deassertion, (2) **TXDIS/*SRESET*** deassertion, and (3) S/W Reset (MII Register 0.15 is asserted). See Table 9-4 for detailed EEPROM interface pin descriptions.

TABLE 9-4: EEPROM INTERFACE PINS

Pin Name	Pin Number	Type	Description
EECLK/PLLMODE	J5	Ozc/Ipd	**EECLK – EEPROM Clock Output** This output is the clock line of the two-wire, MSA-compliant serial EEPROM interface. This pin should be connected to the **SCL** input pin of the AT24 series of Microchip EEPROMs. **PLLMODE – PLL Mode Select Input** **PLLMODE** is sampled during the device power-up sequence or on Reset. When **PLLMODE** pin is high, the PHY expects a 125 MHz clock input as the PHY's reference clock. When default with internal pull-down, 25 MHz is expected at **REFCLK** pin from either an external crystal or oscillator.
EEDAT	H5	Ozc/Ipd	**EEPROM Serial I/O Data** This bidirectional signal is the data line of the two-wire, MSA-compliant serial EEPROM interface. This pin should be connected to the SDA pin of the AT24 series of Microchip EEPROMs. The PHY determines that an external EEPROM is present by monitoring the **EEDAT** pin at power-up or when **RESET** is deasserted. If **EEDAT** has a 4.7 kΩ to 10 kΩ external pull-up resistor (to **VDDIOMICRO**), it assumes that an EEPROM is present. The **EEDAT** pin can be left floating or grounded to indicate no EEPROM.

9.3 JTAG Interface

- If **JTAG** is not used, **TRST** should be pulled low by a pull-down resistor. Refer to Table 9-5 for details on **JTAG** pin information.

TABLE 9-5: JTAG PINS

Pin Name	Pin Number	Type	Description
TCK	C9	I, PU	**JTAG Test Clock** This input pin is the master clock source used to control all JTAG test logic in the device. This pin should be pulled down with a 2 kΩ pull-down resistor in designs that require JTAG functionality. This pin should be tied low in designs that do not require JTAG functionality.
TDI	A11	I, PU	**JTAG Test Data Serial Input Data** Serial test pattern data is scanned into the device on this input pin, which is sampled with respect to the rising edge of **TCK**. This pin should be tied high to **VDDIOCTRL** in designs that do not require JTAG functionality.
TDO	B11	O	**JTAG Test Data Serial Output Data** Serial test data from the PHY is driven out of the device on the falling edge of **TCK**. This pin should be left floating during normal chip operation.
TMS	B10	I, PU	**JTAG Test Mode Select** This input pin sampled on the rising edge of **TCK**, controls the TAP (Test Access Port) controller's 16-state, instruction state machine. This pin should be tied high to **VDDIOCTRL** in designs that do not require JTAG functionality.
$\overline{\text{TRST}}$	C8	I, PU	**JTAG Reset** This active-low input pin serves as an asynchronous Reset to the JTAG TAP controller's state machine. As required by the JTAG standard, this pin includes an integrated on-chip pull-up (to **VDDIOCTRL**) resistor. Because of the internal pull-up, if the JTAG controller on the printed circuit board does not utilize the $\overline{\text{TRST}}$ signal, then the device will still function correctly when the $\overline{\textbf{\textit{TRST}}}$ pin is floating. If the JTAG port of the PHY is not used on the printed circuit board, then this pin should be pulled down with a 2 kΩ pull-down resistor to ground.

10.0 MISCELLANEOUS

10.1 Reset

- The VSC8211 must be reset at power-up. One option is to hold $\overline{RESET}$ low for a minimum 2 ms after all power rails are up, control pins are stable, and clocks are active. Another option is to pulse $\overline{RESET}$ low for a minimum of 2 ms after power-up. $\overline{RESET}$ is typically driven by a voltage monitor device or by the management processor or FPGA Reset circuit. See Table 10-1 for more information on this pin.

TABLE 10-1: RESET PIN

Pin Name	Pin Number	Type	Description
$\overline{RESET}$	A12	I	Device Reset. Active-low input that powers down the device and sets all register bits to their default state.

10.2 LED Pins

- The PHY has dedicated **LED** pins [4:0] to drive 3 LEDs directly. For power savings, all LED outputs can be configured to pulse at 5 kHz with a 20% duty cycle. All LED outputs are active-low and driven with 3.3V from the **VDD33A** power supply when deasserted.
- Because the 100BASE-FX mode uses 100BASE-T resources, its indications are those of the 100BASE-T mode.
- Four different functions have been assigned to each **LED** pin. Selection is done through CMODE hardware configuration or through MII Register 27 (1Bh) – LED Control Register. Refer to Table 10-2 for **LED** pin information.

TABLE 10-2: LED PINS AND BASIC DEFAULT FUNCTION

Pin Name	Pin Number	Type	Description
LED0	A13	O	**LED – Direct-Drive LED Outputs** After Reset, these pins serve as the direct drive, low EMI, LED driver output pins. All **LED** pins are active-low and driven at a 3.3V logic-high through the **VDD33A** analog power supply. The function of each **LED** can be set by using hardware configuration **CMODE3** pins and CMODE3[3] value. See Table 8-3 and Table 8-4 for more details on LED modes. Refer to MII Register 27 LED configuration bits.
LED1	B12	O	
LED2	B13	O	
LED3	C12	O	
LED4	C13	O	

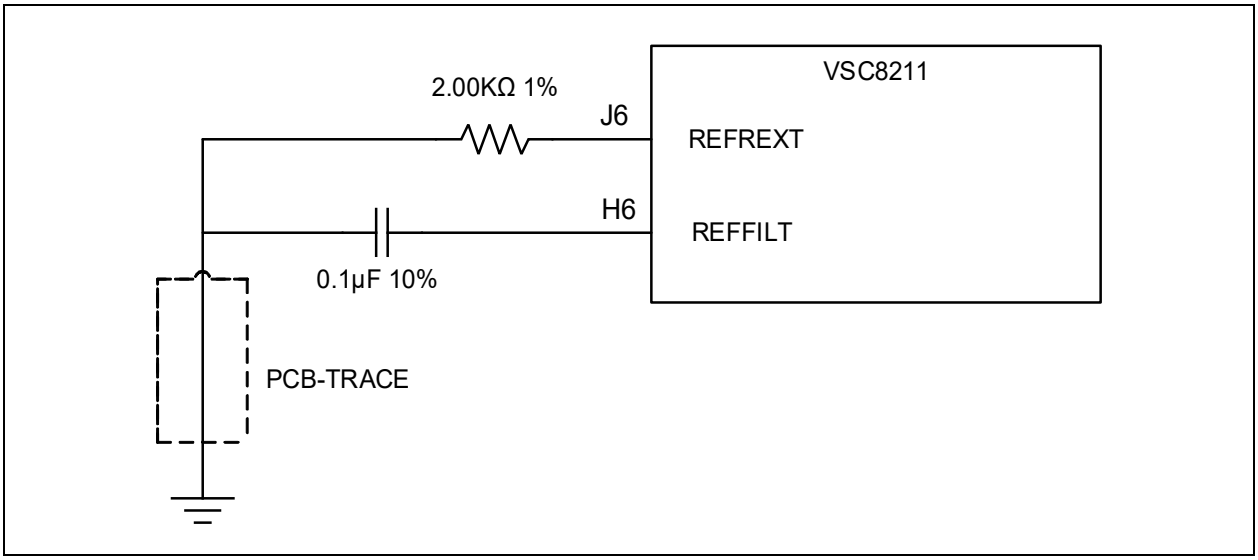
10.3 Analog Bias Pins for Voltage Reference

- The **REFREXT** pin (pin J6) on the VSC8211 should connect to the system ground through a 2 kΩ resistor with a tolerance of 1.0% and minimum 1/16W. This pin is used to set up critical bias currents for the Ethernet physical device.
- The **REFILT** pin (pin H6) on the VSC8211 should connect to the system ground through a 0.1 µF capacitor with 10% tolerance, NPO, X7R, or X5R ceramic materials are all acceptable.
- For best performance, special consideration of the ground connection of the voltage reference circuit is necessary to prevent bus drops that would cause reference voltage inaccuracy. The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace (rather than being connected individually to a common ground plane) as shown in Figure 10-1. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8211.
- Refer to Table 10-3 for details on pin description. See Figure 10-1 for the analog bias pin connections.

TABLE 10-3: BIASING PIN DETAILS

Pin Name	Pin Number	Type	Description
REFREXT	J6	ABIAS	**REFREXT – Reference External Resistor** Bias pin connects through external 2 kΩ (1%) resistor to system ground.
REFFILT	H6	ABIAS	**REFFILT – Reference Filter** Filters internal reference through an external 0.1 µF (10%) capacitor to system ground

FIGURE 10-1: VOLTAGE REFERENCE SCHEMATIC



10.4 MODDEF0/CLKOUT Pin

- This pin is used as either a PHY ready indicator output or a 125 MHz clock output. See Table 10-4 for more information on this pin.

TABLE 10-4: MODDEF0/CLKOUT PIN DETAILS

Pin Name	Pin Number	Type	Description
MODDEF0/ CLKOUT	A10	O	**MODDEF0 – Active Low PHY Ready indicator Output** Use the **CMODE** configuration pin to set CMODE1[3] =0 or set the MII Register 21E.15=1 to SFP mode. **CLKOUT – 125 MHz Clock Output** Use the **CMODE** configuration pin to set CMODE1[3] =1 or set MII Register 21E.15=0 to IEEE mode. The PHY drives a 125 MHz clock output after the PHY startup sequence has completed. This clock can be disabled by clearing MII Register 18.0. The voltage levels of this clock are determined by the VDDIO power supply.

10.5 TXDIS/$\overline{\text{SRESET}}$ Pin

- When this pin is asserted, it places the PHY in a Low-Power state, which includes disabling the SerDes interface. Although the device is powered down, non-volatile Serial Management Interface registers retain their values. See Table 10-5 for more information on this pin.

TABLE 10-5: TXDIS/$\overline{\text{SRESET}}$ PIN

Pin Name	Pin Number	Type	Description
TXDIS/ $\overline{SRESET}$	G5	IPU	**TXDIS – Transmit Disable** Use the **CMODE** configuration pin to set CMODE1[3] =0 or set MII Register 21E.15=1 to SFP mode. When **TXDIS/*SRESET*** is active-high, the pin behaves like **TXDIS**. ***$\overline{SRESET}$*** **–Software Reset** Use the **CMODE** configuration pin to set CMODE1[3] =1 or set MII Register 21E.15=0 to IEEE mode. When **TXDIS/*SRESET*** is active-low, the pin behaves like ***$\overline{SRESET}$***.

10.6 Unused and No-Connection Pins

- The **NC** pins (pins E3, H8, and J8) are unconnected and must be left floating.

10.7 General External Pull-Up and Pull-Down Resistors

- If no pull-up resistor value is specified, it is recommended to use a 4.7 kΩ resistor.
- If no pull-down resistor value is specified, it is recommended to use a 1 kΩ or 4.7 kΩ resistor.

NOTES:

11.0 HARDWARE CHECKLIST SUMMARY

TABLE 11-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify if the digital ground and the analog ground are tied together. Check if there is a chassis ground for the line-side ground.		
Section 3.0, "Power"	Section 3.1, "Current and Power Requirements"	Refer to Table 3-1 to ensure that the power pins are correct. Select the correct power components with at least about 25% to 30% margin based on system configuration. Select one of Table 3-2 or Table 3-3 as a reference for the system power design.		
	Section 3.2, "Power Supply Planes"	When creating a PCB layout, refer to this section for power supply planes design.		
	Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering"	Refer to Figure 3-1 to check the power circuit connection, decoupling capacitors, bulk capacitors, and filtering.		
	Section 3.4, "Bulk Decoupling Capacitors"	If doing a PCB layout, check this section for the bulk decoupling capacitors required.		
Section 4.0, "Twisted Pair Media Interface (CAT5)"	Section 4.1, "10/100/1000 Mbps Interface Connection"	Verify all analog I/O pin connections for the Ethernet port circuit design based on product design requirements. Select the design based on Figure 4-1 and Figure 4-2.		
	Section 4.2, "10/100/1000 Magnetics and RJ45 Connector Connection"	Verify the magnetics and the common-mode capacitor connections based on Figure 4-1 and Figure 4-2.		
	Section 4.3, "PCB Layout Considerations"	Use this section for PCB layout design reference, and check if the Gigabit copper port PCB layout request is met.		
	Section 4.4, "100 MBPS Fiber Support Over Copper Media Interface"	Read this section and refer to Figure 4-3 for the copper media interface to connect to one 100Base-FX SFP module.		
Section 5.0, "SGMII/SerDes MAC Interface"	Section 5.1, "SGMII/SerDes MAC Pins and Connection"	Refer to Figure 5-1 to make sure you are using the correct pins for the SGMII/SerDes MAC interface in design.		
	Section 5.2, "SGMII/SerDes MAC"	Read this section and refer to Figure 5-1 for SGMII/SerDes MAC interface to connect to an external SGMII or SerDes MAC in design.		
	Section 5.3, "SerDes MAC Interface to SFP"	Read this section and refer to Table 5-2 and Figure 5-2 for SerDes MAC interface to connect to one 1000Base-X SFP or connect to one 1000Base-T SFP in design.		
	Section 5.4, "SGMII/SerDes MAC Interface Design Rules"	Read this section for SGMII/SerDes MAC interface PCB design reference.		

TABLE 11-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 6.0, "Parallel MAC Interface"	Section 6.1, "GMII/RGMII/MII Interface Pins"	Refer to Table 6-1 to verify if the correct pins are used for the GMII/RGMII/MII interfaces in the design.		
	Section 6.1.1, "GMII Interface"	Read this section and refer to Figure 6-1 for the correct GMII connection between VSC8211 and other-end MAC GMII interface.		
	Section 6.1.2, "MII Interface"	Read this section and refer to Figure 6-2 for the correct MII connection between VSC8211 and other-end MAC MII interface.		
	Section 6.1.3, "RGMII Interface Connections"	Read this section and refer to Figure 6-3 for the correct RGMII connection between VSC8211 and other-end MAC RGMII interface.		
	Section 6.1.4, "Timing Considerations for Design with RGMII Interface"	Read this section and refer to Table 6-2 to select correct strap pin CMODE5 setting or the register setting for data to clock input/output skew/delay based on other-end RGMII data to clock input/output skew/delay.		
	Section 6.2, "TBI/RTBI Interface Pins"	Refer to Table 6-3 to verify if the correct pins are used for the TBI/RTBI interfaces in design.		
	Section 6.2.1, "TBI Interface"	Read this section and refer to Figure 6-4 for the correct TBI connection between VSC8211 and other-end MAC TBI interface.		
	Section 6.2.2, "RTBI Interface Connections"	Read this section and refer to Figure 6-5 or Figure 6-6 for the correct RTBI connection between VSC8211 and other-end MAC RTBI interface.		
	Section 6.2.3, "Timing Considerations for Design with RTBI Interface"	Read this section and refer to Table 6-4 to select the correct strap pin CMODE5 setting or the register setting for data to clock input/output skew/delay based on other-end RTBI data to clock input/output skew/delay.		
	Section 6.3, "GMII/RGMII/MII and TBI/RTBI Interface Series Terminations"	Read this section and use the series termination resistors at other-end drive pins only for GMII/RGMII/MII and TBI/RTBI interfaces.		

TABLE 11-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 7.0, "Device Clocks"	Section 7.1, "Reference Clock"	Refer to Table 7-1 to select the reference clock circuit-related pins in the design.		
	Section 7.2, "25 MHz Crystal Circuit"	Refer to Figure 7-1 for 25 MHz crystal clock circuit design and make sure to use the correct strapping for **PLLMODE** pin and **OSCDIS** pin.		
	Section 7.3, "25 MHz Oscillator Circuit"	Refer to Figure 7-2 for 25 MHz oscillator clock circuit design and make sure to use the correct strapping for **PLLMODE** pin and **OSCDIS** pin. Select correct resistor divider value based on Table 7-1 and selected 25 MHz oscillator.		
	Section 7.4, "125 MHz Oscillator Circuit"	Refer to Figure 7-3 for 125 MHz oscillator clock circuit design and make sure to use the correct strapping for **PLLMODE** pin and **OSCDIS** pin. Select the correct resistor divider value based on Table 7-1 and selected 125 MHz oscillator.		
Section 8.0, "Hardware Configuration Using CMODE Pins"	Section 8.1, "CMODE Pin Description"	Refer to Table 8-1 to make sure that the correct **CMODE** pin numbers in the hardware configuration are used.		
	Section 8.2, "Select Mode Pins Pull-Up and Pull-Down Resistor Value for System Design"	Refer to Table 8-2 to select the correct pull-up and pull-down resistor values for each **CMODE** pin to get the needed 4-bit value for each **CMODE** pin.		
	Section 8.3, "CMODE Bits"	Refer to Table 8-2, Table 8-3, and Table 8-4 to form the hardware configuration based on system design.		
Section 9.0, "Digital Interface"	Section 9.1, "Dual-Mode Serial Management Interface (SMI)"	Refer to Table 9-1 for **SMI** pin description and verify the correct use of pin numbers.		
	Section 9.1.1, "PHY Register Access with SMI in MSA Mode"	Refer to Table 9-2 for **SMI** in MSA mode pin description if **SMI** in MSA mode is selected.		
	Section 9.1.2, "PHY Register Access with SMI in IEEE Mode"	Refer to Table 9-3 for **SMI** in **IEEE** mode pin description if **SMI** in IEEE mode is selected.		
	Section 9.2, "EEPROM Interface"	Refer to Table 9-4 for EEPROM interface pin description. Make sure to use the correct pin numbers and check if there is a pull-up resistor on **EEDAT** pin if using EEPROM.		
	Section 9.3, "JTAG Interface"	Refer to Table 9-5 and the description in this section for all **JTAG** pins in the circuit design.		

TABLE 11-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 10.0, "Miscellaneous"	Section 10.1, "Reset"	Refer to Table 10-1 for using the correct **RESET** pin and see if the designed Reset circuit meets the Reset time requirement.		
	Section 10.2, "LED Pins"	Check if the correct **LED** pins are used based on Table 10-2 and refer to Table 8-4 for CMODE3[3] settings based on LED function required in the system design.		
	Section 10.3, "Analog Bias Pins for Voltage Reference"	Check if the correct pull-down resistor value is used for the **REFREXT** pin and if the correct pull-down capacitor value is used for **REFFILT** pin based on Table 10-3 and Figure 10-1.		
	Section 10.4, "MODDEF0/CLKOUT Pin"	Refer Table 10-4 to see if this pin is used correctly in the design.		
	Section 10.5, "TXDIS/SRESET Pin"	Refer Table 10-5 to see if this pin is used correctly in the design.		
	Section 10.6, "Unused and No-Connection Pins"	Verify if all unused pins and **NC** pins are unconnected.		
	Section 10.7, "General External Pull-Up and Pull-Down Resistors"	Generally, it is recommended to use 4.7 kΩ pull-up resistor and 1 kΩ pull-down resistor.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004531A (05-05-22)	Initial release	

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