

# dsPIC33EPXXXMC50X to dsPIC33CK256MP508 Migration and Performance Enhancement Guide

## INTRODUCTION

**Note:** This migration document details the transition to the dsPIC33CK256MP508 devices. Please note that some features may not be available. Refer to the device-specific data sheet for more details. The device data sheets and errata are available for download from the Microchip Worldwide Website at: <http://www.microchip.com>.

The dsPIC33CK256MP508 device family includes many new features and changes from the dsPIC33EPXXXMC50X device family. The code developed for the dsPIC33EPXXXMC50X family devices can be ported to the dsPIC33CK256MP508 family devices after making the appropriate changes, as described in this document. The dsPIC33CK256MP508 family devices feature many improvements and new capabilities, such as:

- Higher Speed (100 MIPS) CPU with Additional Instructions for Improved Control Loop Execution
- Flash Program Memory up to 256 Kbytes
- RAM up to 24 Kbytes
- New High-Resolution PWM (250 ps) with Additional Features
- Higher Speed ADC (3.5 Msps) with Additional Channels (up to 24)
- New High-Speed Analog Comparator with Slope Compensation DAC
- Three Dedicated Operational Amplifiers
- New Controller Area Network (CAN FD) modules
- Current Bias Generators (CBG) with Advanced Controls
- New SPI with Audio Codec Support
- New UART with Advanced Protocol Support
- Additional Instances of UART, SPI and I<sup>2</sup>C
- New Capture/Compare/PWM/Timer (MCCP/SCCP) Asynchronous Modules that are able to Operate at Higher Clock Speeds than the CPU Clock
- Improved Oscillator System with Flexible Auxiliary PLL
- Additional Functional Safety Features:
  - New dual WDT
  - RAM Built-In Self-Test (MBIST)
  - Backup FRC oscillator
  - Capacitorless voltage regulator
  - ECC with new Fault Injection and Status registers

## MIGRATION OVERVIEW

This migration and performance enhancement guide discusses several enhancements, changes and application migration considerations related to the dsPIC33CK256MP508 family devices. The following are the key migration considerations:

- Pinouts of all packages have changed
- SFR addresses have changed
- Peripheral Pin Select (PPS) mappings have changed
- Interrupt Vector Tables (IVTs) have changed
- I/O Port Change Notification Control registers have changed
- New peripherals:
  - High-Resolution PWM
  - CAN FD
  - Multiprotocol UART
  - DAC/Comparators
  - Dual WDT
  - Deadman Timer
  - Configurable Logic Cell (CLC)
  - Parallel Master Port (PMP)
  - Single-Edge Nibble Transmission (SENT)
- Clocking options and assignments for peripherals have changed
- Device Configuration registers have changed

**Note:** CTMU peripheral is not present on dsPIC33CK256MP508 family devices.

Each section of this document describes one peripheral or major feature of the dsPIC33CK256MP508 device family.

For more information on new or modified modules, refer to the “dsPIC33CK256MP508 Family Data Sheet” (DS70005349).

### Topics Covered Include:

|                                                                       |   |
|-----------------------------------------------------------------------|---|
| CPU.....                                                              | 2 |
| High-Speed, 12-Bit Analog-to-Digital Converter (ADC).....             | 2 |
| High-Resolution PWM with Fine Edge Placement.....                     | 2 |
| High-Speed Analog Comparator with Slope Compensation DAC .....        | 2 |
| Controller Area Network Flexible Data-Rate (CAN FD) Module.....       | 3 |
| Operational Amplifiers .....                                          | 3 |
| Multiprotocol Universal Asynchronous Receiver Transmitter (UART)..... | 3 |
| Serial Peripheral Interface (SPI) .....                               | 3 |
| Capture/Compare/PWM/Timer Modules (MCCP and SCCP).....                | 4 |
| Oscillator Configuration.....                                         | 6 |
| DMA Controller.....                                                   | 6 |
| Capacitorless Regulator .....                                         | 6 |
| I/O Ports .....                                                       | 6 |

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## CPU

The CPU on dsPIC33CK256MP508 family devices is essentially the same as the dsPIC33EPXXXMC50X CPU, but has a few additional instructions and can be operated at higher speeds. The CPU and Flash support higher instruction rates, up to 100 MIPS.

All instructions from the dsPIC33EPXXXMC50X devices will execute on the dsPIC33CK256MP508 family. Additional instructions have been added to offload software calculations in tight control loops. The new instructions are:

- BFINT
- BFINS
- DIVF2
- DIV2.S and DIV2.U
- Extensions to the DO instruction
- FLIM and FLIM.V
- MAX and MAX.V
- MIN and MIN.V
- NORM
- LAC.D
- SAC.D

The DSP Accumulator registers, ACCA and ACCB, have been added to the shadow register set for context save/restore of DSP operations.

For more information, refer to **Section 3.0 “CPU”** in the “dsPIC33CK256MP508 Family Data Sheet” (DS70005349). For additional instruction set information, see the “16-Bit MCU and DSC Programmer’s Reference Manual” (DS70000157).

## HIGH-SPEED, 12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

The dsPIC33CK256MP508 family’s ADC has increased capabilities and features compared to the dsPIC33EPXXXMC50X family ADC. The main difference is the number of ADC cores. The dsPIC33EPXXXMC50X family implements one ADC core that has up to four Sample-and-Hold circuits to support 10-bit simultaneous sampling. The dsPIC33CK256MP508 family implements three 12-bit ADC cores. Additional differences are:

- The dsPIC33CK256MP508 devices have additional input channels, up to 24
- The dsPIC33CK256MP508 family ADC can operate faster, up to 3.5 Msps
- The dsPIC33CK256MP508 devices include four digital comparators
- The dsPIC33CK256MP508 devices include four oversampling filters

The register interface is significantly different and includes many new registers for the oversampling filters and digital comparators. There are also separate instances for a control register for each of the ADC cores.

## HIGH-RESOLUTION PWM WITH FINE EDGE PLACEMENT

The dsPIC33CK256MP508 family has a new PWM module with increased resolution, up to 250 ps, and additional features and functions. The register interface is similar for the basic functions, but has many additions for new features. The synchronization and triggering methods have been changed and expanded to support more applications. The Fault inputs have been replaced with four highly configurable PWM Control Input (PCI) interfaces, per PWM generator instance, to allow for complex signal conditioning. Some of the new features include advanced data buffering, combinational triggers, combinational logic output and PWM event outputs. These features allow offloading the CPU when performing complex control algorithms.

For more detailed information, see **Section 12.0 “High-Resolution PWM with Fine Edge Placement”** in the “dsPIC33CK256MP508 Family Data Sheet” (DS70005349).

## HIGH-SPEED ANALOG COMPARATOR WITH SLOPE COMPENSATION DAC

The dsPIC33CK256MP508 family uses new comparator/DAC modules that feature a high-speed slope compensation DAC. The DAC supports high-speed ramping profiles that can be used in many control loops. The dsPIC33CK256MP508 devices have three instances of comparator/DACs, and the DACs are based on a Pulse Density Modulation (PDM) technique that allows fast changes in the DAC output voltage. Due to this design, the dsPIC33CK256MP508 devices do not have an external EXTREF1/2 reference. The PDM DAC supports Static DC, Slope, Hysteresis and Triangle Ramp modes. The comparator/DAC is tightly coupled with the ADC and PWM.

For more detailed information, see **Section 14.0 “High-Speed Analog Comparator with Slope Compensation DAC”** in the “dsPIC33CK256MP508 Family Data Sheet” (DS70005349).

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## CONTROLLER AREA NETWORK FLEXIBLE DATA-RATE (CAN FD) MODULE

The dsPIC33CK256MP508 family has two instances of a new CAN module that supports CAN FD. The CAN FD protocol supports a larger data field and faster speeds to allow for higher bandwidth.

The new CAN FD module also supports older CAN versions, including Version 2.0, which the dsPIC33EPXXXMC50X devices support. The register interface has changed significantly and no longer uses the DMA for data transfer, as used on the dsPIC33EPXXXMC50X devices. Instead of using the DMA, the dsPIC33CK256MP508 family allows the CAN to access RAM directly. The CAN FD module has seven configurable FIFOs that can be used for either transmit or receive, with the data stored in RAM itself.

For more detailed information, see **Section 11.0 “Controller Area Network (CAN FD) Module”** in the “*dsPIC33CK256MP508 Family Data Sheet*” (DS70005349).

## OPERATIONAL AMPLIFIERS

The op amp/comparators on the dsPIC33EPXXXMC50X devices have been replaced with dedicated operational amplifiers and separate comparators (see the “**High-Speed Analog Comparator with Slope Compensation DAC**” section) on the dsPIC33CK256MP508 devices.

The dsPIC33CK256MP508 family provides up to three instances of op amp depending on the package pin count.

The op amps are controlled by two SFR registers: AMPCON1L and AMPCON1H, and remain in a low-power state until the AMPON bit is set. Each op amp can then be enabled independently by setting the corresponding AMPENx bit (x = 1, 2, 3).

For more detailed information, see **Section 27.0 “Operational Amplifier”** in the “*dsPIC33CK256MP508 Family Data Sheet*” (DS70005349).

## MULTIPROTOCOL UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

The dsPIC33CK256MP508 family devices have new UART modules with protocol support. Some of the supported protocols are LIN, DMX and smart card. The register interface has many differences to support the new features, including three multiple use data SFRs (UxP1, UxP2, UxP3) for the protocol modes. The UART features a new fractional Baud Rate Generator mode that improves target accuracy to common UART speeds.

In LIN mode, the UART supports a new optional built-in checksum generation and verification. Two SFRs, UxTXCHK and UxRXCHK, provide access to the checksum values.

The UART has an additional ‘Event’ interrupt (UxEVT) in addition to the transmit, receive and error interrupts. The ‘Event’ interrupt will trigger on auto-baud, Break, wake from Sleep and smart card events.

For more detailed information, see **Section 16.0 “Universal Asynchronous Receiver Transmitter (UART)”** in the “*dsPIC33CK256MP508 Family Data Sheet*” (DS70005349).

## SERIAL PERIPHERAL INTERFACE (SPI)

The dsPIC33CK256MP508 family devices feature an additional instance of SPI modules with increased capabilities, including audio codec support. The dsPIC33CK256MP508 family’s SPI has the following additional features:

- Configurable Data Width up to 32 Bits
- Separate TX and RX Buffers
- Deeper Data Buffers up to 32 Deep
- Dedicated Interrupts for TX and RX
- Configurable Clocking Options Including REFO

In addition to basic framed SPI protocol, the modules also support four different Audio modes including:

- I<sup>2</sup>S mode
- Left Justified mode
- Right Justified mode
- PCM/DSP mode

The register interface has signification changes to support the new features. On dsPIC33CK256MP508 family 48, 64 and 80-pin devices, the SPI instance of SPI2 can operate up to 50 MHz speed when selected as a non-PPS (dedicated) pin. The election is done using the SPI2PIN bit (FDEVOP[13]).

For more detailed information, see **Section 17.0 “Serial Peripheral Interface (SPI)”** in the “*dsPIC33CK256MP508 Family Data Sheet*” (DS70005349).

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## CAPTURE/COMPARE/PWM/TIMER MODULES (MCCP AND SCCP)

This section provides a brief summary of the new MCCP/SCCP modules in the dsPIC33CK256MP508 family devices. In addition to Timer1 on the dsPIC33CK256MP508 family devices, the dsPIC33CK256MP508 family devices include several universal Capture/Compare/PWM/Timer modules, which provide the functionality of three different peripherals of the earlier dsPIC33 devices. These modules can operate in one of three major modes:

- General Purpose Timer (TMR)
- Output Compare/PWM (OC)
- Input Capture (IC)

The module is provided in two different forms, distinguished by the number of PWM outputs that the module can generate. Single output modules (SCCPs) provide only one PWM output. Multiple output modules (MCCPs) can provide up to six outputs and an extended range of power control features depending on the pin count of the particular device. All other features of the modules are identical.

The dsPIC33CK256MP508 devices have one MCCP module and eight SSCP modules. [Table 1](#) shows the possible maximum number of timers, input capture and output compare peripherals available on the dsPIC33CK256MP508 family devices.

**TABLE 1: MAXIMUM NUMBER OF PERIPHERALS FOR dsPIC33EPXXXMC50X AND dsPIC33CK256MP508 FAMILIES**

| Peripheral     | dsPIC33EPXXXMC50X | dsPIC33CK256MP508       |
|----------------|-------------------|-------------------------|
| Input Capture  | 4                 | 9 (MCCP/SCCP)           |
| Output Compare | 4                 | 9 (MCCP/SCCP)           |
| 16-Bit Timer   | 5                 | 1 (TMR) + 9 (MCCP/SCCP) |

## General Purpose Timer (TMR)

The MCCP/SCCP can be used as a 32-bit general purpose timer or two 16-bit timers. Both 16-bit timers can generate an interrupt and one timer can also provide a trigger to other peripherals.

Setting the T32 bit configures the MCCP/SCCP module as a single 32-bit timer. [Table 2](#) shows the features comparison between previous TMR modules and the new MCCP/SCCP module in Timer mode.

**TABLE 2: COMPARISON BETWEEN DEDICATED TMR MODULE AND MCCP/SCCP IN TIMER MODE**

| Feature                                  | TMR Module                                                     | MCCP/SCCP Module                                                                                              |
|------------------------------------------|----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|
| Number of 16-Bit Timers per Module       | 1                                                              | 2                                                                                                             |
| Number of 32-Bit Timers per Module       | Two modules are required                                       | 1                                                                                                             |
| Trigger to Other Module                  | Matches the timer rollover                                     | Can be configured at a different time than the timer rollover                                                 |
| Clock Synchronization                    | Synchronous only (except Timer1)                               | Asynchronous or synchronous                                                                                   |
| Clock Source and Maximum Clock Frequency | Clocked from CPU clock only; frequency is limited by CPU clock | If the module is clocked from REFO, then it can be any clock source and frequency is not limited by CPU clock |

## Output Compare/PWM (OC)

The MCCP/SCCP offers new features, such as 32-bit operation and a variety of output modes. [Table 3](#) shows the features comparison between the previous OC module and the new MCCP/SCCP module in PWM mode.

**TABLE 3: COMPARISON BETWEEN DEDICATED OC MODULE AND MCCP/SCCP MODULE IN PWM MODE**

| Feature                                  | OC Module                                                      | MCCP/SCCP Module                                                                                                                       |
|------------------------------------------|----------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| Number of PWM Outputs                    | One                                                            | One for SCCP and up to six for MCCP                                                                                                    |
| Motor Control and Switching Applications | Not supported                                                  | Supported (DC, BLDC motors, half and full-bridge switches)                                                                             |
| Output Modes                             | Single Output mode                                             | Single Output mode, Brush DC Motor Output mode (forward and reverse), Half-Bridge Output mode, Push-Pull Output mode, Output Scan mode |
| Dead-Time Control                        | Not supported                                                  | Supported                                                                                                                              |
| Number of Modules for 32-Bit Operation   | Two modules are required                                       | One                                                                                                                                    |
| Clock Source and Maximum Clock Frequency | Clocked from CPU clock only; frequency is limited by CPU clock | If module is clocked from REFO, then it can be any clock source and frequency is not limited by CPU clock                              |

## Input Capture (IC)

The MCCP/SCCP module can also be used as an input capture module in 16-bit or 32-bit mode. It is different from the previous dedicated peripheral, where two IC modules were required for 32-bit operation. In Input Capture mode, the MCCP/SCCP module can be asynchronous and work from any clock source if it is used with the REFO module.

For more information, refer to **Section 22.0 “Capture/Compare/PWM/Timer Modules (SCCP/MCCP)”** in the *“dsPIC33CK256MP508 Family Data Sheet”* (DS70005349).

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## OSCILLATOR CONFIGURATION

The dsPIC33EPXXXMC50X and dsPIC33CK256MP508 families have a similar oscillator system with a few differences:

- New high-speed PLL
- Configurable auxiliary PLL
- Dedicated CAN clock output

### PLL

The dsPIC33CK256MP508 features a new high-speed PLL that has some additional features and available output options. The PLL in the dsPIC33CK256MP508 devices can operate up to 1.6 GHz and has dual post-scalers for additional frequency division resolution. The PLL subsystem also has some fixed dividers that directly feed some of the high-speed peripherals, such as the ADC, PWM and comparator/DAC. The register interfaces are very similar, however, there is an additional register, PLLDIV, that controls a pair of postscalers.

### Auxiliary PLL Module

The dsPIC33EPXXXMC50X devices implement only one PLL that is shared by both the CPU and peripherals. The dsPIC33CK256MP508 family has a 2nd PLL instance that can be independently configured to allow peripherals to run at different speeds, such as the PWM, ADC or DAC. Like the dsPIC33CK256MP508 family's main PLL, the auxiliary PLL features a configurable feedback divider, and pre- and post-dividers for maximum flexibility. The auxiliary PLL has its own SFRs to configure: ACLKCON1, APLLFBD1 and APLLDIV1.

### CAN Clock Control

The dsPIC33CK256MP508 family implements a new CAN-specific Clocking Control register, CANCLKCON. It allows a discrete clock for the CAN FD module and has many clock input sources and a configurable post-divider for maximum flexibility.

For more detailed information, see **Section 9.0 “Oscillator with High-Frequency PLL Configuration”** in the *“dsPIC33CK256MP508 Family Data Sheet”* (DS70005349).

## DMA CONTROLLER

The dsPIC33CK256MP508 family implements a different DMA controller than the dsPIC33EPXXXMC50X devices. The architecture is similar, but the register interface is completely different. Both device families implement four unidirectional channels between a peripheral and RAM, with triggering based on inter-

rupts. The dsPIC33EPXXXMC50X devices' DMA was limited to a set number of peripherals that were DMA capable. However, the dsPIC33CK256MP508 family's DMA is based on addresses and can support any peripheral address, and includes data bus collision detection to prevent CPU Stalls.

For more detailed information, see **Section 10.0 “Direct Memory Access (DMA) Controller”** in the *“dsPIC33CK256MP508 Family Data Sheet”* (DS70005349).

## CAPACITORLESS REGULATOR

The dsPIC33CK256MP508 family features a new capacitorless voltage regulator. The dsPIC33CK256MP508 family does not require a large capacitor for the core voltage and removes the potential of shorting the core voltage to other voltages. The dsPIC33CK256MP508 family features three regulators; two regulators power the core and one regulator powers the PLLs. Regulator control during Sleep has changed slightly with the VREGSF bit (RCON[11]) being replaced with the LPWREN bit (VREGCON[15]). The VREGCON register also has controls for placing the three regulators in lower power modes.

For more information, refer to **Section 30.4 “On-Chip Voltage Regulators”** within **Section 30.0 “Special Features”** in the *“dsPIC33CK256MP508 Family Data Sheet”* (DS70005349).

## I/O PORTS

The dsPIC33EPXXXMC50X and dsPIC33CK256MP508 families are not pin compatible and have different pin-outs on all packages. Refer to the **“Pin Diagrams”** section in the *“dsPIC33CK256MP508 Family Data Sheet”* (DS70005349) for details.

The dsPIC33CK256MP508 devices also implement enhanced Change Notification (CN), including some additional SFRs. The enhanced functionality includes:

- Port Change or Edge Detection modes
- Individual port CN enables
- Individual port CN status bits
- Individual port CN interrupt enables and flags

The individual controls and status bits allow user software to know which port instance (0-15), within the port, has had an event without having to read the port SFR to determine which has changed.

For more detailed information, see **Section 8.0 “I/O Ports”** in the *“dsPIC33CK256MP508 Family Data Sheet”* (DS70005349).

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## **APPENDIX A: REVISION HISTORY**

### **Revision A (April 2019)**

This is the initial version of this document.

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**NOTES:**

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**Note the following details of the code protection feature on Microchip devices:**

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