Silicon Errata and Data Sheet Clarifications

ATxmega128A1U/64A1U

Introduction

The ATxmega128A1U/64A1U devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002058), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATxmega128A1U/64A1U devices.

Note:

- This document summarizes all the silicon errata issues from all silicon revisions, previous and current

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1. Silicon Issue Summary

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. L[1]
Device	2.2.1. Register ANAINIT in MCUR Will Always Read as Zero	X
	2.2.2. Internal 1V Reference has Noise at Low Temperature	X
System Clock	2.3.1. Enabling DFLL With Illegal Reference Oscillator Will Lock the Clock System	X
	2.3.2. XOSCPWR Configuration is Non-Functional	X
AWeX	2.4.1. AWeX PWM Output After Fault Restarted With Wrong Values	X
	2.4.2. Configuration of PGM and CWCM is not as Described in XMEGA AU Manual	X
RTC	2.5.1. RTC Counter Value not Correctly Read After Sleep	X
	2.5.2. RTC Clock Output Option is Non-Functional	X
USB	2.6.1. USB, When Receiving 1023 Byte Length Isochronous Frame, it Will Corrupt the 1024th SRAM Location	X
	2.6.2. USB Endpoint Table is 16-byte Alignment	X
	2.6.3. USB Auto ZLP Feature is Non-Functional	X
TWI	2.7.1. TWI, SDAHOLD Configuration in the TWI CTRL Register is one bit	X
USART	2.8.1. Disabling the USART Transmitter Does not Automatically set the TxD Pin Direction to Input	X
ADC	2.9.1. ADC has Increased INL Error in When Used in SE Unsigned Mode at Low Temperatures	X
	2.9.2. ADC is Non-Functional in SE Unsigned Mode With VREF Below 1.8V	X
	2.9.3. ADC has Increased Linearity Error When Using the Gain Stage Above 500 ksps	X
DAC	2.10.1. DAC Offset Calibration Range too Small When Using AVCC as Reference	X
	2.10.2. DAC Clock Noise	X

Note:

1. This revision is the initial release of the silicon.

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2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Register ANAINIT in MCUR Will Always Read as Zero

The ANAINIT register in the MCUR module will always be read as zero, even if written to a value. The actual content of the register is correct.

Work Around

Do not use software that reads these registers to get the Analog Initialization configuration.

Affected Silicon Revisions

Rev. L
X

2.2.2 Internal 1V Reference has Noise at Low Temperature

The internal 1.0V reference for the ADC and DAC has increased noise at low temperatures. The noise can result in INL numbers up to +/-20 LSB at temperatures below 0°C.

Work Around

For the ADC, use oversampling to reduce noise. For the DAC, use external filter to reduce the noise.

Affected Silicon Revisions

Rev. L
X

2.3 System Clock and Clock Options

2.3.1 Enabling DFLL With Illegal Reference Oscillator Will Lock the Clock System

If selecting an external crystal as a reference for DFLL, but no crystal is connected, and DFLL is enabled, the DFLL will be locked until a reset is issued.

Work Around

Do not enable DFLL before the reference clock is present, enabled and ready.

Affected Silicon Revisions

Rev. L
X

2.3.2 XOSCPWR Configuration is Non-Functional

The Crystal oscillator drive (XOSCPWR) option in the XOSC Control register is non-functional.

Work Around

None.

Affected Silicon Revisions

Rev. L
X

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2.4 AWeX – Advanced Waveform eXtension

2.4.1 AWeX PWM Output After Fault Restarted With Wrong Values

When recovering from the fault state, the PWM output will drive wrong values to the port for up to two CLK_{PER} + one CLK_{PER4} cycles.

Work Around

The following sequence can be used in Latched mode:

1. Disable DTI outputs (Write DTICCxEN to 0).
2. Clear fault flag.
3. Wait for overflow.
4. Re-enable DTI (Write DTICCxEN to 1).
5. Set pin direction to output.

The above will remove the glitch, but the following period will be shorter. Follow the same procedure in a Cycle-by-cycle mode as long as the Pattern Generation Mode is not enabled.

For Pattern Generation Mode, there is no work around.

Affected Silicon Revisions

Rev. L
X

2.4.2 Configuration of PGM and CWCM is not as Described in XMEGA AU Manual

The configuration of a mutual waveform channel mode (CWCM) and pattern generation mode (PGM) is not as described in the *XMEGA AU manual*.

Work Around

Configure PWM and CWCM according to the following table.

Table 2-1. PWM and CWCM Configuration

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

Affected Silicon Revisions

Rev. L
X

2.5 RTC - 16-bit Real-Time Counter

2.5.1 RTC Counter Value not Correctly Read After Sleep

If a real-time counter (RTC) interrupt is used to wake up the device from sleep, and bit 0 of the RTC count register (CNT) has the same value as when the device entered a sleep mode, CNT will not be read correctly during the first prescaled RTC clock cycle after wakeup. The read value will be the same as the value in the register when entering sleep.

Work Around

Wait at least one prescaled RTC clock cycle before reading CNT.

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Affected Silicon Revisions

Rev. L
X

2.5.2 RTC Clock Output Option is Non-Functional

The real-time counter (RTC) as a clock output option is non-functional, and setting the RTCOUT bit in the clock and event out register (CLKEVOUT) will have no effect.

Work Around

None.

Affected Silicon Revisions

Rev. L
X

2.6 USB – Universal Serial Bus Interface

2.6.1 USB, When Receiving 1023 Byte Length Isochronous Frame, it Will Corrupt the 1024th SRAM Location

When USB is configured for isochronous operation and 1023 bytes data payload size, the 1024th RAM location directly after the endpoint RAM buffer will be corrupted.

Work Around

Allocate 1024 bytes RAM buffer when using a 1023 isochronous endpoint. This workaround is implemented in all USB software and source code from Microchip in the AVR Software Framework.

Affected Silicon Revisions

Rev. L
X

2.6.2 USB Endpoint Table is 16-byte Alignment

The USB endpoint table uses 16-byte alignment instead of 16-bit alignment.

Work Around

Align the endpoint configuration table pointer in SRAM to a 16-byte. This workaround is implemented in all USB software and source code from Microchip in the AVR Software Framework.

Affected Silicon Revisions

Rev. L
X

2.6.3 USB Auto ZLP Feature is Non-Functional

The Auto ZLP feature is non-functional and can not be used.

Work Around

None.

Affected Silicon Revisions

Rev. L
X

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2.7 TWI – Two-Wire Interface

2.7.1 TWI, SDAHOLD Configuration in the TWI CTRL Register is one bit

The SDAHOLD configuration in the TWI Control (CTRL) register is one bit. Due to this, the SDA hold time can be configured for a maximum of ~50 ns when enabled. Configuring for a longer hold time will have no effect.

Work Around

It must be handled in software if a longer SDA hold time than 50 ns is required.

Affected Silicon Revisions

Rev. L
X

2.8 USART – Universal Synchronous and Asynchronous Receiver and Transmitter

2.8.1 Disabling the USART Transmitter Does not Automatically set the TxD Pin Direction to Input

If the USART transmitter is idle with no frames to transmit, setting TXEN to zero will not automatically set the TxD pin direction to input.

Work Around

The TxD pin direction can be set to input using the Port pin direction to input using the port Direction (DIR) register. When the port pin direction is input, it will be immediate and ongoing transmissions will be truncated.

Affected Silicon Revisions

Rev. L
X

2.9 ADC – 12-bit Analog to Digital Converter

2.9.1 ADC has Increased INL Error in When Used in SE Unsigned Mode at Low Temperatures

When using the ADC on Single-Ended (SE) unsigned mode, INL error increases up to +/- 5LSB in temperatures below -20°C.

Work Around

Use the ADC in single ended-signed mode.

Affected Silicon Revisions

Rev. L
X

2.9.2 ADC is Non-Functional in SE Unsigned Mode With VREF Below 1.8V

When using the ADC on single-ended unsigned mode, and V_{REF} is below 1.8V, INL and DNL error is increased above +/- 10 LSB, i.e., the ADC has missing codes under this condition.

Work Around

Use the ADC in single ended-signed mode.

Affected Silicon Revisions

Rev. L
X

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2.9.3 ADC has Increased Linearity Error When Using the Gain Stage Above 500 ksps

The INL error for the gain stage is increased to above 20 LSB for a sampling speed exceeding 500 ksps.

Work Around

None.

Affected Silicon Revisions

Rev. L
X

2.10 DAC – 12-bit Digital to Analog Converter

2.10.1 DAC Offset Calibration Range too Small When Using AVCC as Reference

If using AVCC as a reference, the DAC offset calibration will not remove the offset error. Offset could be up to 100 LSB after calibration.

Work Around

Offset adjustment must be partly handled in software.

Affected Silicon Revisions

Rev. L
X

2.10.2 DAC Clock Noise

The system clock is visible as clock noise on the output of the DAC. Peak-to-peak noise is in the 0.7-1.6 mV at 2 MHz and 0.05-0.1 mV at 32 MHz range. If the external clock is used as a system clock, the noise is up to three times higher.

Work Around

Add an external low-pass filter to remove the noise.

Affected Silicon Revisions

Rev. L
X

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3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002058).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Errata Section in Data Sheet is no Longer Valid

A clarification for the Errata section in the device data sheet has been made.

The errata content has been moved to a separate document, *ATxmega128A1U/64A1U Silicon Errata and Data Sheet Clarifications* (this document).

See the *Silicon Errata Issues* section of this document for the latest errata.

3.2 Ordering Information

3.2.1 Ordering Information

A clarification has been made to the table **Package Type** for all devices with 100C1 package.

Ordering Code	Flash (bytes)	EEPROM (bytes)	SRAM (bytes)	Speed (MHz)	Power Supply	Package (1)(2)(3)	Temp.
ATxmega128A1U-AU	128K + 8K	2K	8K	32	1.6 - 3.6V	100A	-40°C - 85°C
ATxmega128A1U-AUR(4)	128K + 8K	2K	8K				
ATxmega64A1U-AU	64K + 4K	2K	4K				
ATxmega64A1U-AUR(4)	64K + 4K	2K	4K				
ATxmega128A1U-CU	128K + 8K	2K	8K			100C1(5)	
ATxmega128A1U-CUR(4)	128K + 8K	2K	8K				
ATxmega64A1U-CU	64K + 4K	2K	4K				
ATxmega64A1U-CUR(4)	64K + 4K	2K	4K				
ATxmega128A1U-C7U	128K + 8K	2K	8K			100C2	
ATxmega128A1U-C7UR(4)	128K + 8K	2K	8K				
ATxmega64A1U-C7U	64K + 4K	2K	4K				
ATxmega64A1U-C7UR(4)	64K + 4K	2K	4K				
ATxmega128A1U-AN	128K + 8K	2K	8K	32	1.6 - 3.6V	100A	-40°C - 105°C
ATxmega128A1U-ANR(4)	128K + 8K	2K	8K				
ATxmega128A1U-CN	128K + 8K	2K	8K			100C1(5)	
ATxmega128A1U-CNR(4)	128K + 8K	2K	8K				

Notes:

1. This device can also be supplied in wafer form. Contact your local Microchip sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see "**Packaging information**".
4. Tape and Reel.
5. This package is no longer available.
   - Refer to the End of Life (EOL) PCN for more details: www.microchip.com/product-change-notifications/#/19129/ASER-31SUSF550

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Package Type	
100A	100-lead, 14 x 14 x 1.0 mm, 0.50 mm lead pitch, thin profile plastic quad flat package (TQFP)
100C1	**100-ball, Thin Fine Pitch Ball Grid Array (B2B) - 9 x 9 x 1.2 mm Body (TFBGA)**
100C2	100-ball, 7 x 7 x 1.0 mm body, ball pitch 0.65 mm, very thin fine-pitch ball grid array (VFBGA)

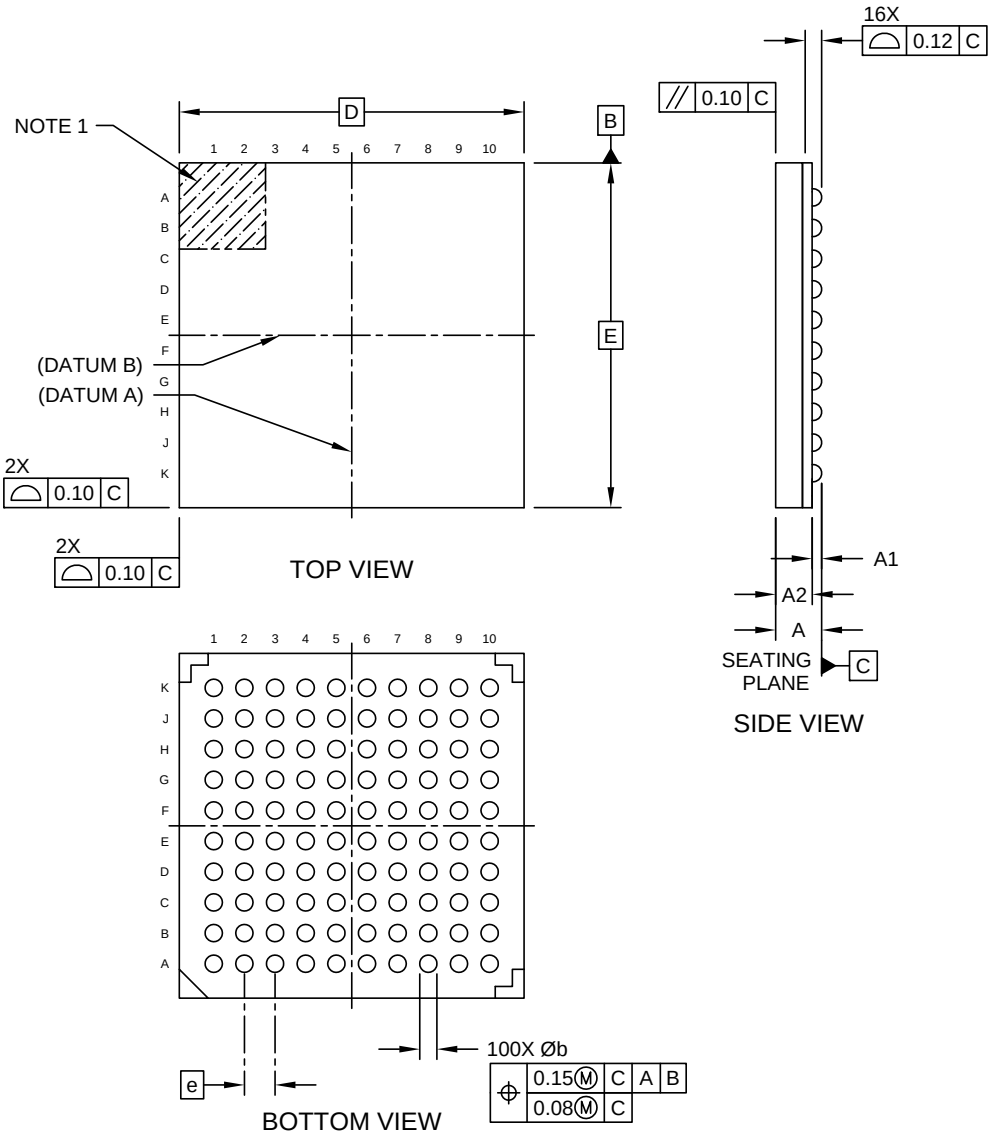
3.3 Packaging Information

3.3.1 100C1

A clarification has been made to section **100C1**, providing the correct package outline drawing.

100-Ball Thin Fine Pitch Ball Grid Array (B2B) - 9x9x1.2 mm Body [TFBGA]
Atmel Legacy Global Package Code CPR

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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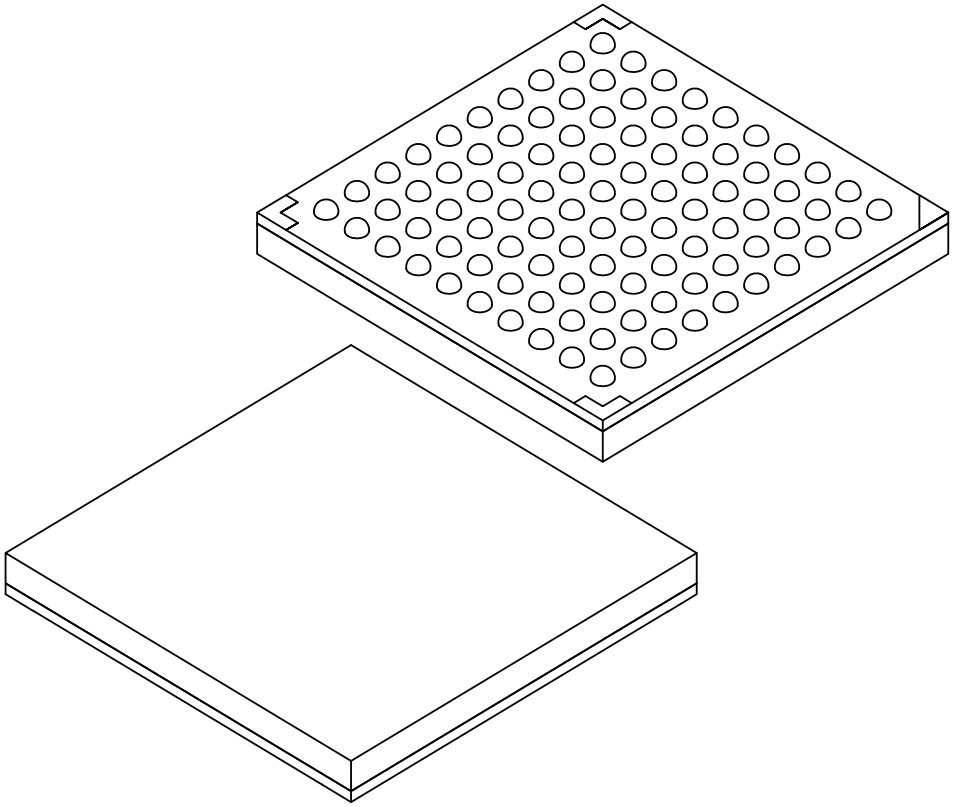
100-Ball Thin Fine Pitch Ball Grid Array (B2B) - 9x9x1.2 mm Body [TFBGA]
Atmel Legacy Global Package Code CPR

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		100	
Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Ball Height	A1	0.20	-	-
Molded Plastic Thickness	A2	0.65	-	-
Overall Length	D		9.00 BSC	
Overall Width	E		9.00 BSC	
Terminal Diameter	b	0.40	0.45	0.50

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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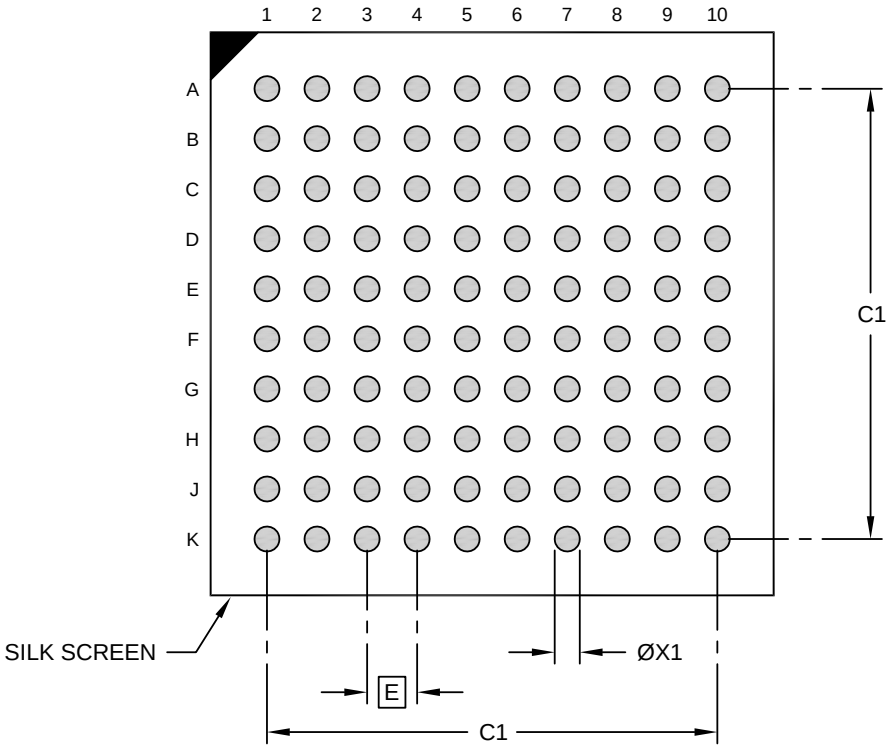
100-Ball Thin Fine Pitch Ball Grid Array (B2B) - 9x9x1.2 mm Body [TFBGA]
Atmel Legacy Global Package Code CPR

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		7.20	
Contact Pad Spacing	C2		7.20	
Contact Pad Width (X20)	X1			0.40

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
A	07/2023	Initial document release • Errata content moved from the data sheet and restructured to the new document template • Data sheet clarifications added: – Packaging Information: 3.3.1. 100C1

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