
PLC Hardware Design Guidelines

Introduction

This application note provides some guidelines to help the customer to use, implement and modify the different reference designs for the PLC-related circuitry in their own equipment, giving recommendations about the parts and the PCB layout.

The reference designs are fully available (Schematics, BOM, Gerber files, etc.) in the webpage of any of the PLC modems.

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1. PLC Coupling Circuitry Description

All the PLC coupling reference designs used with Microchip PLC modems are developed with the same design goals: high performance, low cost and simplicity.

With these objectives in mind, Microchip has a wide range of PLC couplings, covering frequencies up to 472 kHz and compliant with different applicable regulations. See [1.2. PLC Coupling Reference Designs](#).

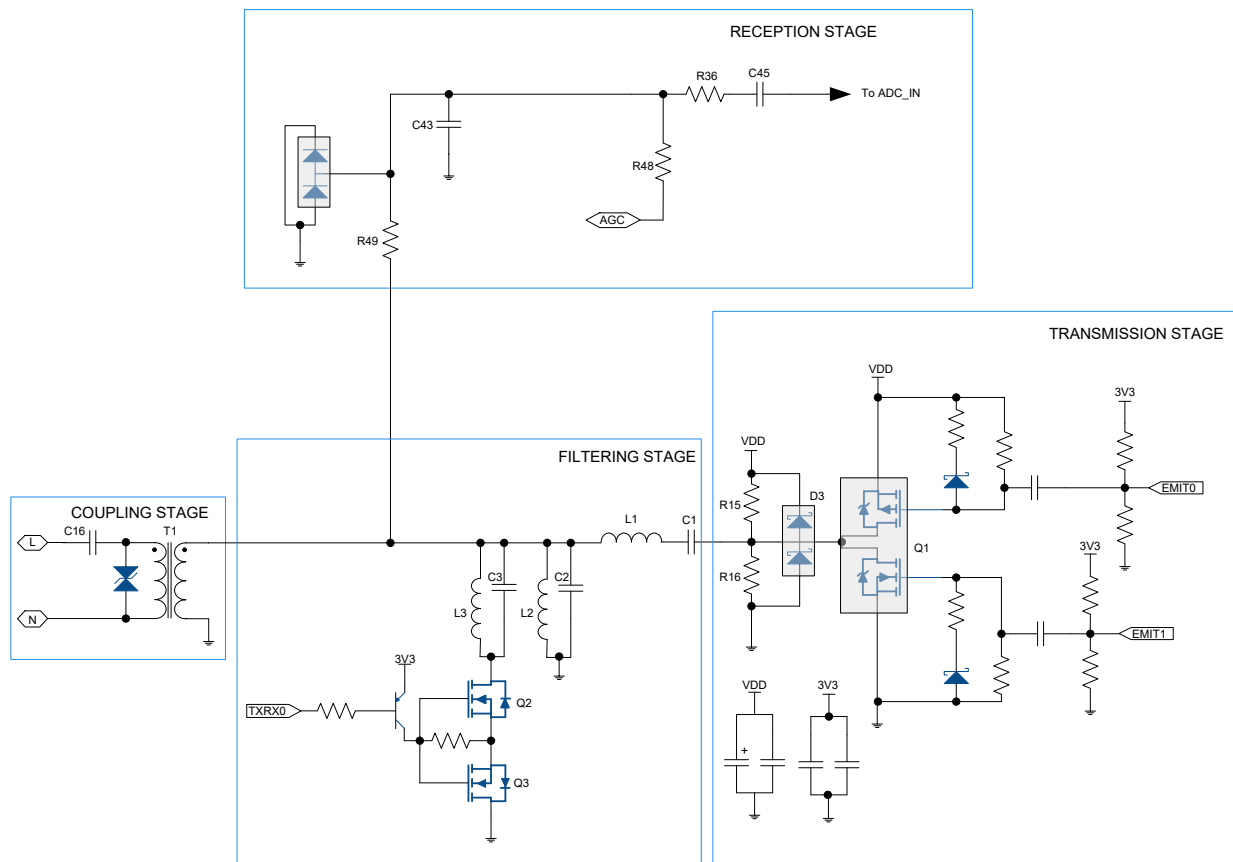
Microchip PLC technology is purely digital and does not require an external DAC/ADC, thus simplifying the required external circuitry. The Microchip PLC coupling reference designs use a few passive components added to an optional class-D amplification stage for transmission.

1.1 PLC Coupling Sub-circuits

All PLC coupling reference designs are generally composed by the same sub-circuits:

- Transmission Stage
- Reception Stage
- Filtering Stage
- Coupling Stage

Figure 1-1. PLC Coupling Sub-circuits Example



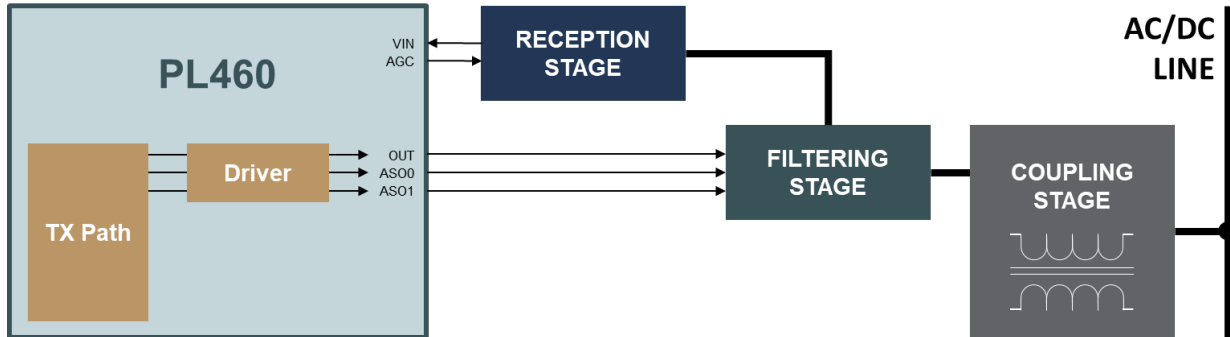
A particular Reference Design may contain more than one sub-circuit of the same kind (i.e., couplings with two transmission and filtering stages).

The reception stage is common to all the reference designs.

1.1.1 Transmission Stage

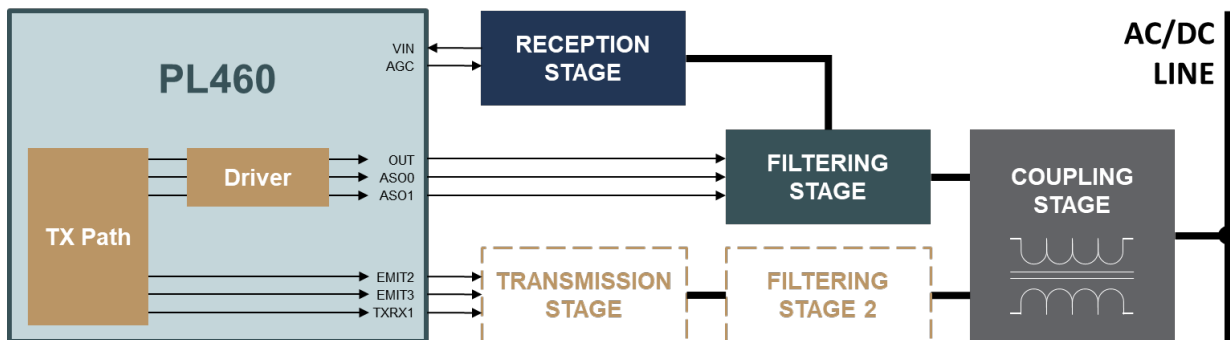
In the PL460, the main transmission stage is embedded in the PLC modem and uses the class-D line-driver included in the device, which optimizes performance in terms of efficiency and EMC compliance while reducing BOM cost and PCB complexity.

Figure 1-2. Main Transmission Path Block Diagram of the PL460



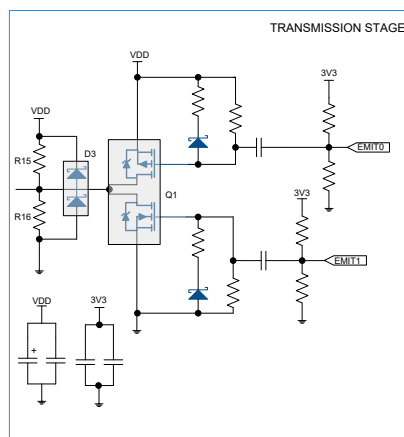
If using the auxiliary transmission branch, it requires an external transmission stage and works in the same way as a PL360 modem.

Figure 1-3. Transmission Path Block Diagram of a Multiband Coupling Using the Auxiliary Branch of the PL460



In the PL360 modem, the transmission stage adapts the EMIT signals and amplifies them.

Figure 1-4. Transmission stage of the PL360



The transmission stage is composed by:

- Driver. A group of resistors and capacitors that adapt the EMIT signals to control the Class-D amplifier
- Amplifier. A Class-D amplifier (Q1)

- Bias and protection. A couple of resistors (R15 and R16) and a couple of Schottky barrier diodes (D3) provide a DC component and provide protection from received disturbances

For optimal transmission performance, Microchip only supports the use of one of the following part numbers for the class-D amplifier (Q1):

- On Semiconductor® (P/N: FDC6420C)
- Diodes Incorporated™ (P/N: DMG6601LVT)
- IcarusTek (P/N: RM3003S6)
- Alpha & Omega Semiconductor (P/N: AO6601)¹
- Niko Semiconductor (P/N: P6002OAG)¹

Note:

1. This part number is only valid for CENELEC A-band design.

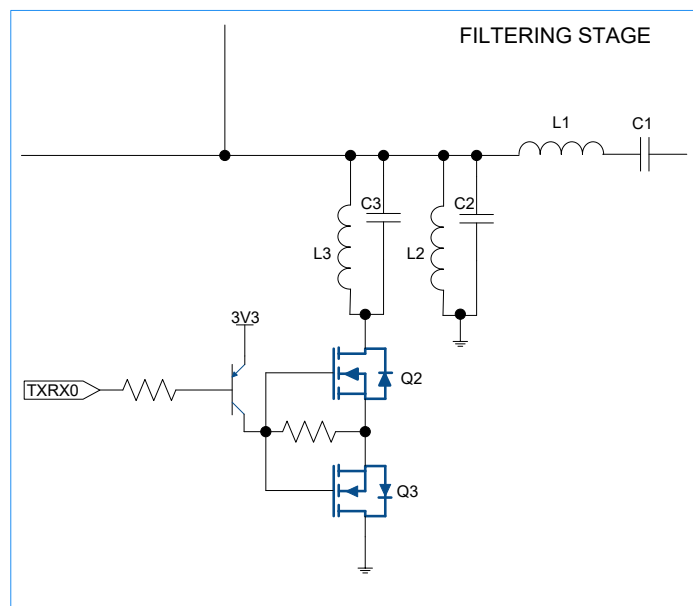
Transmission stage is always followed by a dedicated filtering stage.

1.1.2 Filtering Stage

The filtering stage contains band-pass filters that were designed to achieve high performance in the field but complying, at the same time, with the applicable normative and standards.

The in-band flat response filtering stage does not distort the injected signal, reduces spurious emission below the limits set by the corresponding regulation and blocks potential interferences from other transmission channels.

Figure 1-5. Filtering Stage of the PL360



The filtering stage has three aims:

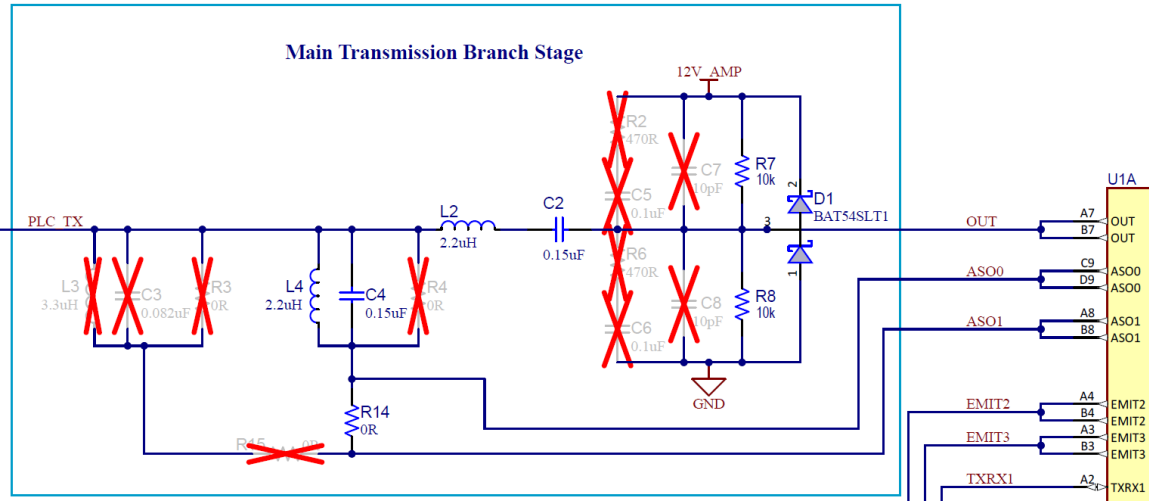
- Band-pass filtering of high frequency components of the square waveform generated by the Transmission Stage (L1, C1, L2, C2, L3 and C3)
- Adapt Input/Output impedance for optimal reception/transmission. This is controlled by the TXRX signal
- And, band-pass filtering for received signals (L2 and C2)

In the PL360 filtering stage, for optimal transmission performance, both Q2 and Q3 must be one of the following three part numbers:

- Diodes Incorporated™ (P/N: DMN2056U-7)
- Diodes Incorporated™ (P/N: DMN3404L-7)
- On Semiconductor® (P/N: FDN337N)

When the main transmission path of the PL460 is used, the circuitry related to the adaptation of the impedance controlled by the TXRX is embedded in the device and the ASOx lines are used to control the connection of the parallel filter to ground. If using only one parallel filter, both ASO0 and ASO1 must be connected together.

Figure 1-6. Main Transmission Path of the PL460-EK



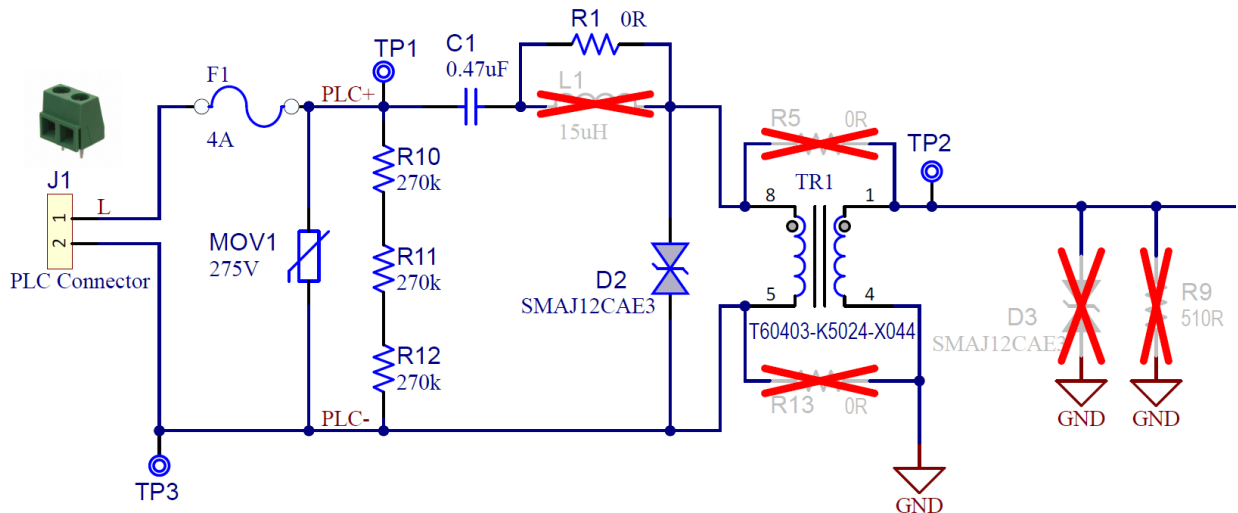
If connecting the system to a physical channel with high voltage or not electrically referenced to the same point than the filtering stage, the filtering stage must always be followed by a coupling stage to isolate the circuitry.

1.1.3 Coupling Stage

The coupling stage has the following objectives:

- To block the low frequency of the mains 50 / 60 Hz line to/from where the signal is injected/received. This is carried out by a voltage capacitor of type X2.
- Add the required protections (fuse, varistor, resistor to discharge the capacitor X2, ...)
- If electrical isolation is required, a transformer 1:1

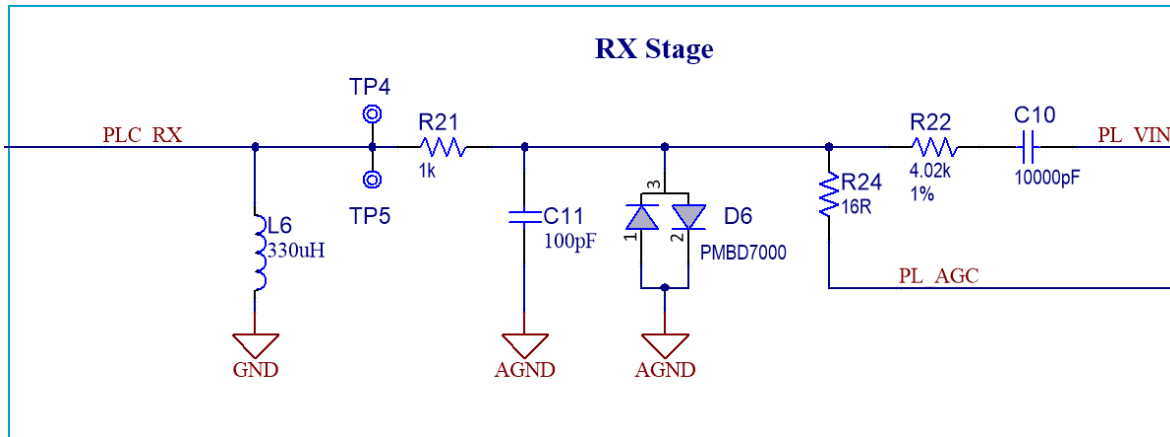
Figure 1-7. Coupling Stage of the PL460-EK



1.1.4 Reception Stage

The reception stage adapts the received analog signal to be properly captured by the internal reception chain. The reception circuit is independent of the PLC band in use.

Figure 1-8. Reception Stage of the PL460-EK



It basically consists of:

- Anti aliasing filter (In the figure RC Filter R21 and C11)
- Automatic Gain Control (AGC) divisor circuit (in the figure R24)
- High-Pass Filter (in the figure R22 and C10)

The AGC circuit avoids distortion on the received signal that may arise when the input signal is high enough to polarize the protective diodes in the forward region.

The High-Pass Filter provides a DC component and adapts the received signal to be properly converted by the internal reception chain.

1.2 PLC Coupling Reference Designs

The following tables summarize the main characteristics of the currently available PLC coupling reference designs:

Table 1-1. ATPLCOUP Boards for PL360-EK

Board Name	PLC Standard	Frequency Band (kHz)	Branch	External Driver	Electrical Isolation	PRIME Channel	G3-PLC Band	Applicable Regulation
ATPLCOUP002	PRIME	206-417	Double	✓	✓	4, 5, 6, 7	—	ARIB [STD-T84 Ver 1.0]
	G3-PLC					—	ARIB	
ATPLCOUP006	PRIME	151-472	Double	✓	✓	3, 4, 5, 6, 7, 8	—	FCC [part 15 - 91905] KN60 [Appendix 11]
	G3-PLC					—	FCC	
ATPLCOUP007	PRIME	35-91	Single	✓	✓	1	—	CEN-A [EN50065]
	G3-PLC					—	CEN-A	
ATPLCOUP008	PRIME	35-91	Single	✓	✗	1	—	CEN-A [EN50065]
	G3-PLC					—	CEN-A	
PLCOUP012	G3-PLC	95-125	Single	✗	Both	—	CEN-B	CEN-B [EN50065]
PLCOUP014	G3-PLC	95-125	Single	✓	Both	—	CEN-B	CEN-B [EN50065]

Table 1-2. Coupling Variants for PL460-EK

Variant Name	Transmission branch	Frequency Band (kHz)	G3-PLC	PRIME Channel	Applicable Regulation
Multiband FCC default & CEN-A	Main	151-472	FCC	3, 4, 5, 6, 7, 8	FCC [part 15 - 91905]
	Auxiliary	35-91	CENELEC-A	1	CEN-A [EN50065]
Multiband FCC default & CEN-B	Main	151-472	FCC	3, 4, 5, 6, 7, 8	FCC [part 15 - 91905]
	Auxiliary	95-125	CENELEC-B	—	CEN-B [EN50065]
Multiband FCC high-attenuation & CEN-A	Main	151-472	FCC	3, 4, 5, 6, 7, 8	FCC [part 15 - 91905]
	Auxiliary	35-91	CENELEC-A	1	CEN-A [EN50065]
Multiband FCC high-attenuation & CEN-B	Main	151-472	FCC	3, 4, 5, 6, 7, 8	FCC [part 15 - 91905]
	Auxiliary	95-125	CENELEC-B	—	CEN-B [EN50065]
CEN-A	Main	35-91	CENELEC-A	1	CEN-A [EN50065]
	Auxiliary	—	—	—	
CEN-B	Main	95-125	CENELEC-B	—	CEN-B [EN50065]
	Auxiliary	—	—	—	
FCC default	Main	151-472	FCC	3, 4, 5, 6, 7, 8	FCC [part 15 - 91905]
	Auxiliary	—	—	—	
FCC high-attenuation	Main	151-472	FCC	3, 4, 5, 6, 7, 8	FCC [part 15 - 91905]
	Auxiliary	—	—	—	
Multiband A	Main	95-125 151-472	CENELEC-A / FCC	1, 3, 4, 5, 6, 7, 8	FCC [part 15 - 91905] CEN-A [EN50065]
	Auxiliary	—	—	—	

Note: All the PL460-EK reference designs are isolated, but they can be easily modified to make them non-isolated. Refer to [3.2.4.2. Non-Isolated Coupling Stage](#) for more information.

2. Safety Recommendations and Disclaimer

These coupling circuits must only be used by expert technicians. They are connected to hazardous voltage (85-265 V_{AC}). To avoid personal damages, this hardware must be handled considering all applicable security protocols.



Microchip does not assume any responsibility for the consequences arising from any improper use of this design.

3. Design Recommendations

The following sections describe some design recommendations that help to get the best performance in the PLC communication and avoid issues specially related to electronic compatibility.

3.1 Layout Recommendations

3.1.1 Power Planes

Two aspects must be considered when designing the power supply layout for the discrete/digital elements of a Power Line Communications application based on Microchip platforms: ESD protection and noise emission. Both topics are covered in detail in the [AVR040](#) application note, and only a brief description is included in this document.



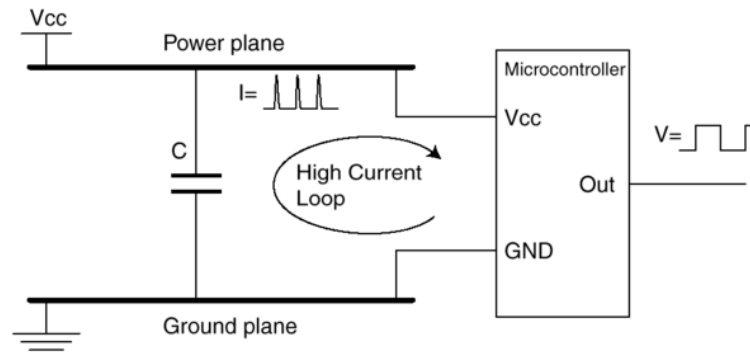
Important: Refer to PL360-EK or PL460-EK design files to be used as reference.

3.1.1.1 Digital Supply

The current provided by the power supply is drawn in very short spikes on the clock edges; if I/O lines are switching, the spikes are even higher. The current pulses on the power supply lines can reach several hundred mA if all I/O lines of an I/O port change their value at the same time. If the I/O lines are not loaded, the pulse is only of a few ns.

This kind of current spike cannot be delivered over long power supply lines; the main source is (or is recommended to be) a decoupling capacitor.

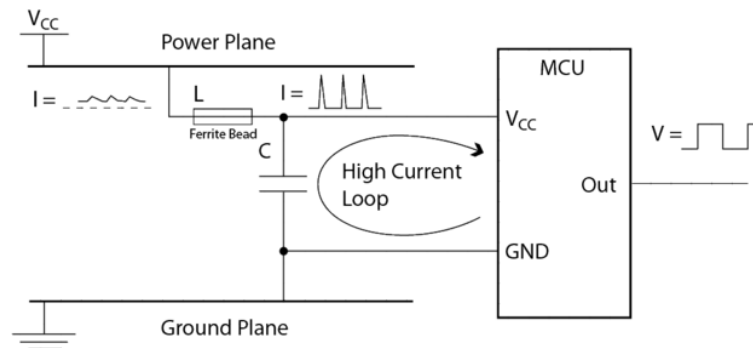
Figure 3-1. Incorrect Decoupling



The previous figure shows an example of insufficient decoupling. The capacitor is placed too far away from the microcontroller, creating a large high current loop. In this case, the power and ground planes are also part of the high current loop. As a result of it, the noise is spread more easily to other devices on the board and radiated emission from the board is increased even further. The whole ground plane acts as an antenna for the noise instead of only the high current loop. This example is the case when the power and ground pins are connected directly to the planes (typically, in hole-mounted components), and the decoupling capacitor is connected the same way. The same effect may be seen in boards with surface-mount components when the integrated circuits are placed on one side of the board and the decoupling capacitors are placed on the other.

The following figure shows a better placement of the decoupling capacitor. The lines of the high current loop are not part of the power or ground planes, avoiding the spread of a lot of noise. Further, the figure shows another improvement of the decoupling: a series ferrite bead inserted to reduce the switching noise on the power plane, ensuring that there are no significant DC voltage drops caused by series resistance.

Figure 3-2. Decoupling with Series Inductor



For devices with multiple pairs of power and ground pins, it is essential that every pair of pins get its own decoupling capacitor.

It is recommended that the main supply also have a ceramic capacitor of some μF to stabilize it.

3.1.1.2 Analog Supply

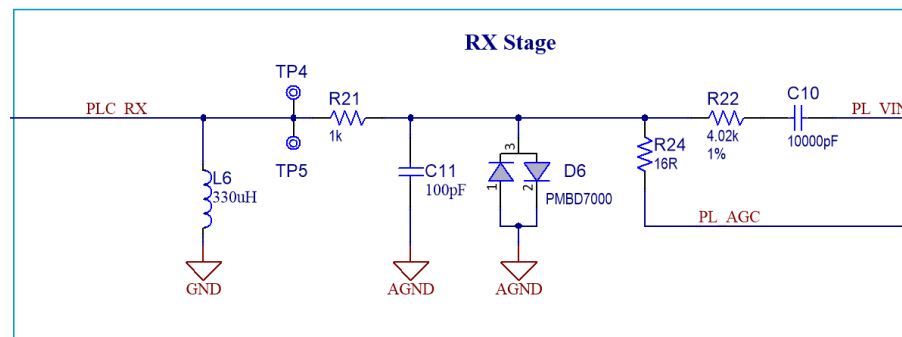
Microchip PLC devices have specific analog supply voltage pins, $V_{\text{DDIN_AN}}$. This separate voltage supply is provided to make the analog circuits less prone to the digital noise originated from the switching of the digital circuits.

In order to obtain good accuracy and performance with the internal reception chain, the analog supply voltage must be decoupled separately in the same manner as the digital supply voltage. Separating the analog ground from the digital ground is recommended so that the analog and digital grounds are only connected at one single point.

3.1.2 Analog Ground Plane

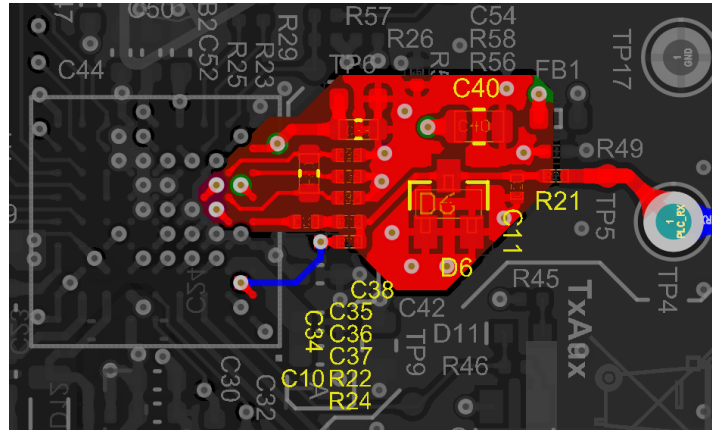
The reception stage from the low pass filter (R21 and C11 in the following figure) to VIN input of the PLC modem is considered the analog path, and routing it over the analog ground plane (AGND) is recommended.

Figure 3-3. Reception Stage



Avoiding cutouts in the ground plane is recommended wherever possible. A cutout is different to a split plane, which is fine as long as the designers keep high-frequency signal tracks over the corresponding continuous plane. Avoiding routing the reception track over a cutout in your analog ground plane is recommended because it causes discontinuity in the return path of the signal leading to reception or EMI issues.

Figure 3-4. Analog GND Plane and Reception Stage in PL460-EK

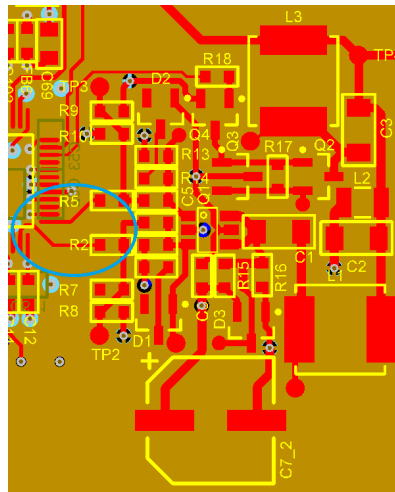


3.1.3 Tracks from EMIT Pins to transistor

The tracks of the transmission stage driver pins (EMITx or OUT outputs) manage high frequency signals. Keeping the high-frequency signal tracks as short as possible is always a good practice.

In the case of the EMITx lines, it is highly recommended to place the resistor as close as possible to the modem

Figure 3-5. Example of Short EMIT Signals



3.1.4 Minimize the Use of Vias

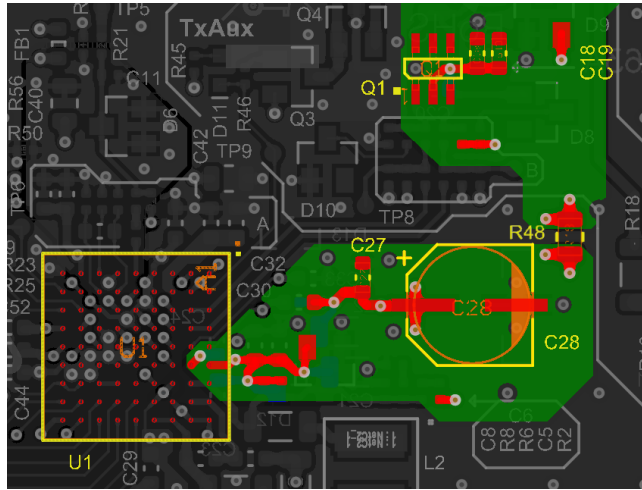
The vias have an inductive behavior, and they modify the features of the tracks that may affect the performance of the transmission and reception paths. Try to avoid any via in PLC-related tracks, especially in the level shift stage of the couplings with the external driver (between the EMIT pads and the transistor).

Vias are acceptable for connecting to power planes.

3.1.5 Capacitors Powering the Amplification Stage

The coupling circuits with external driver require the necessary current for the transistor for a proper performance as well as filtering the DC voltage. Several capacitors are included in the reference designs for this purpose. For example, in the PL460-EK:

Figure 3-6. Capacitors for Powering the Amplifier Stage in PL460-EK



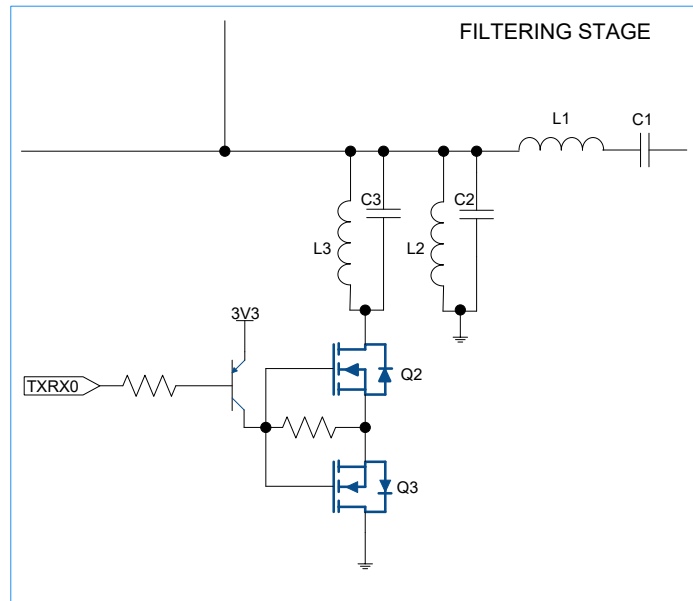
- The ceramic capacitors C18 & C19 must be placed as close as possible to the transistor Q1 to prevent noise issues.
- The low-ESR capacitor C28 must be near the transistor Q1 to avoid voltage drops at high current demands during transmission.
- In the case of the internal driver, C27 and C28 are placed as close as possible to PVDDAMP pins.

The routing of the previous figure (PL460-EK) gives priority to the main transmission branch, placing the capacitor C28 in a better position for this case than the auxiliary transmission branch. In a definitive PCB, the routing could be improved by removing the resistor R28 and modifying the 12V power plane for a better performance in both options, main and auxiliary transmission branches.

3.1.6 Magnetic Coupling of Inductors

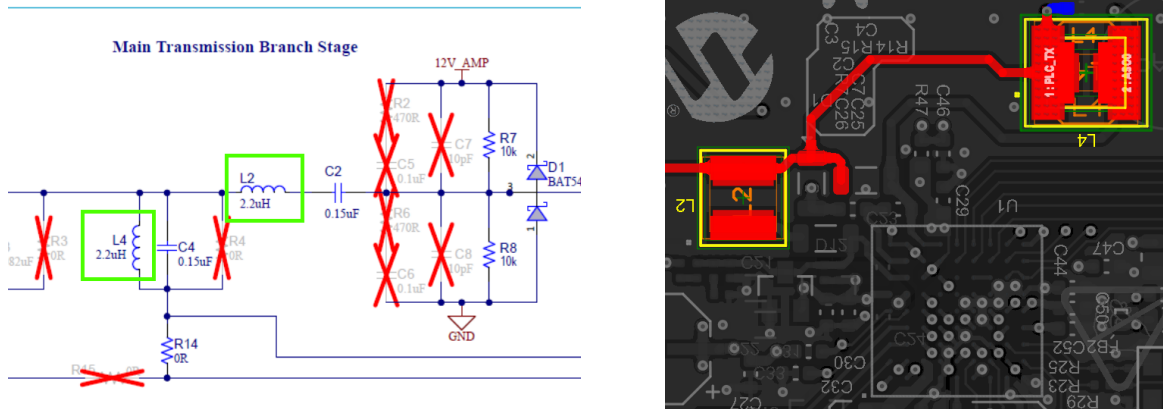
Note that any inductor could be magnetically coupled with each other (i.e., L1, L2 or L3 in the following figure), so avoid placing inductors very close to each other. Otherwise, signals could be coupled from one inductor to another, and that could decrease the performance of the circuitry.

Figure 3-7. Filtering Stage of an External Coupling Circuit



To reduce the magnetic coupling effect, using shielded inductors is recommended; place them orthogonally and as far as possible one from each other..

Figure 3-8. Inductors in Main Transmission Branch of PL460-EK

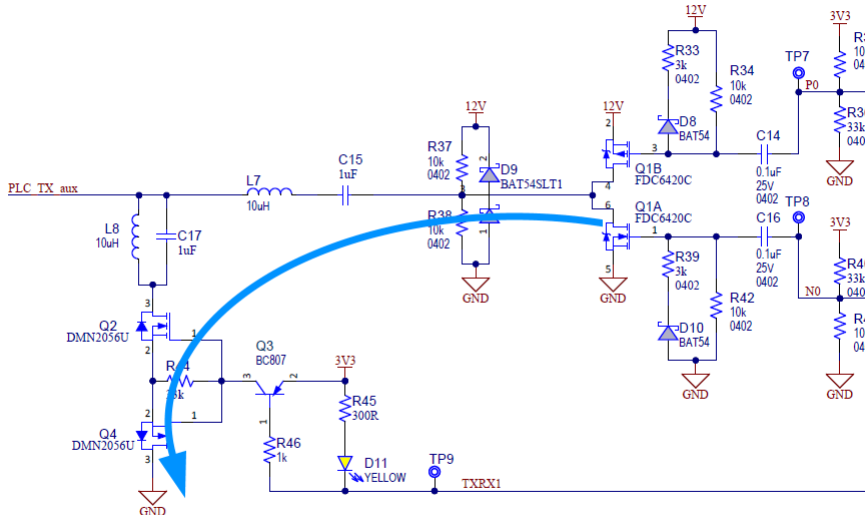


3.1.7 Transmission Stage Loop Through Parallel Filter to Ground

For optimal performance, it is recommended to keep the loop made by the amplifier stage, the filtering stage and ground as short as possible.

During transmission, TXRXx lines make the capacitors and inductors of the parallel filter connect to GND, enabling the parallel filter. The path from those components to GND must be as short as possible to avoid conducted emission issues.

Figure 3-9. Auxiliary Transmission Branch Loop



In the case of the main transmission branch, the amplifier stage is the embedded line-driver, and the ASOx lines are on a direct path to GND (the enabling circuit is also embedded), so ensuring the ASOx lines are as short as possible is recommended to avoid conducted emission issues.

Figure 3-10. Main Transmission Branch Loop (Schematic)

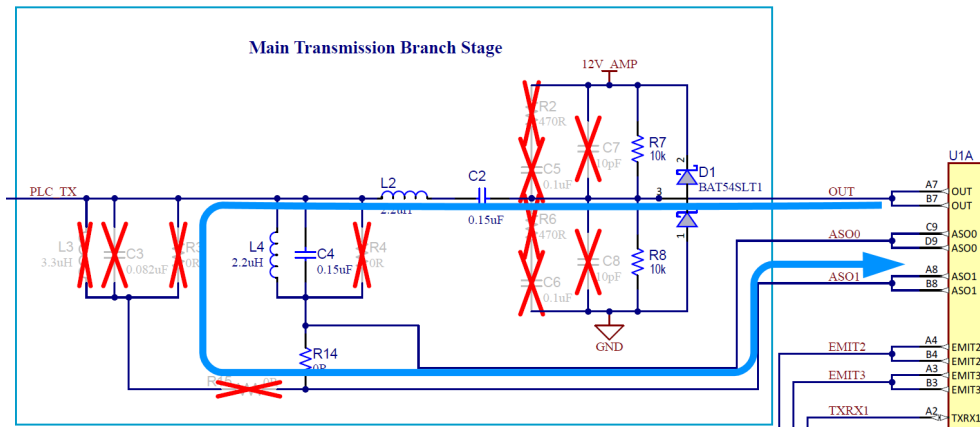
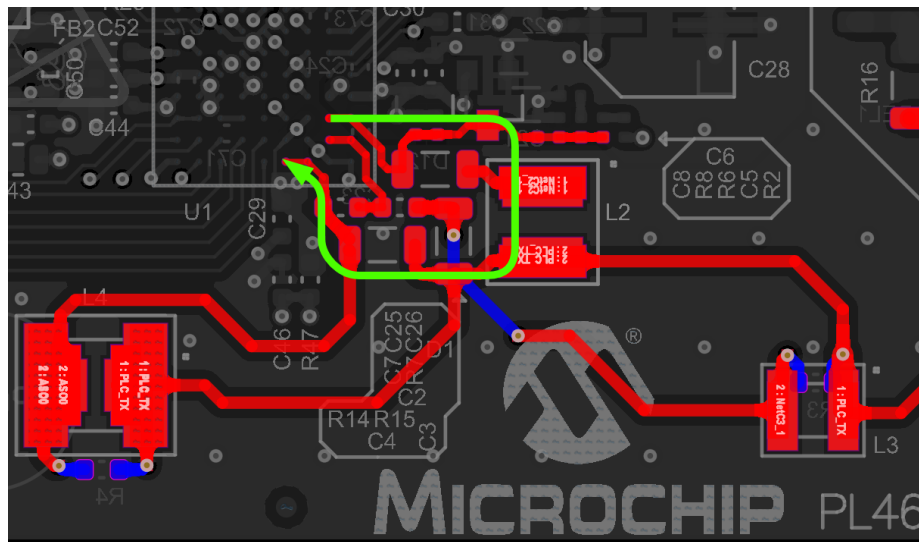


Figure 3-11. Main Transmission Branch Loop (PCB)



Remember: Note that the inductor of the parallel filter can be slightly separated from the capacitor without significant consequences, making it easier to follow the recommendations about distance between inductors in 3.1.6. [Magnetic Coupling of Inductors](#).

3.2 Component Design Recommendations

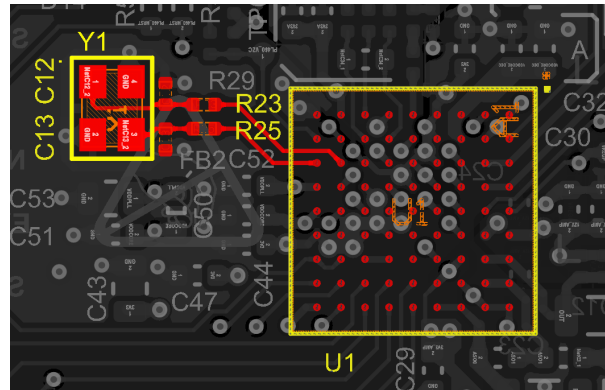
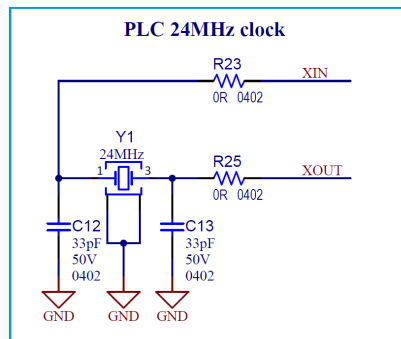
3.2.1 Clocking and Crystal Selection

The clocking topic is widely detailed in the corresponding data sheet. Microchip PLC modems require a 24 MHz crystal oscillator. This clock signal is used as internal reference time of the PLC transceiver.



Important: Refer to the *Crystal Selection Guidelines* application note for detailed guidelines regarding crystal selection and requirements.

Figure 3-12. Clock Circuit of the PLC Modem

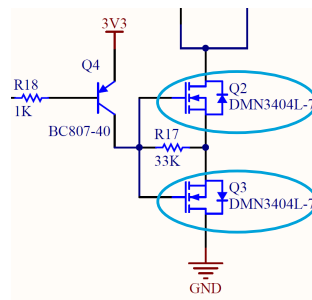


Note: Resistors R23 and R25 in the clock circuitry of the evaluation kit are for testing and debugging purposes. Routing the crystal directly to the PLC modem pins is recommended for a final product.

3.2.2 Adapting Stage

Take into account that the transistors to activate the parallel filter in the stage of the external driver are in opposite rotation.

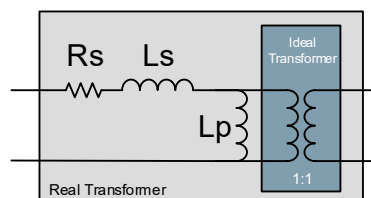
Figure 3-13. Schematic Detail



3.2.3 Isolation Transformer

Microchip recommends the use of the transformer included in the reference designs, but customers are free to use any similar PLC transformer.

Figure 3-14. Real Transformer Model



For any transformer, accomplishing the following features is recommended for optimal performance:

- In-series Parasitic Resistance (R_S) kept as low as possible for minimum losses. In the case of the transformer mounted in the PL460-EK, $R_S = 200 \text{ m}\Omega$.
- In-series Parasitic Inductance (L_S) or "Leakage Inductance" taken into account for calculating the coupling stage resonance frequency (see 3.2.4. [Coupling Stage Filter Design](#)).
Microchip recommends an in-series parasitic inductance as low as possible. L_S lower than $12 \mu\text{H}$ is acceptable (in the case of the transformer mounted in the PL460-EK, $L_S = 0.3 \mu\text{H}$).

Note: For those cases where leakage inductance is very low, an external inductor may be required for completing the coupling stage resonance tank (see 3.2.4. [Coupling Stage Filter Design](#)).

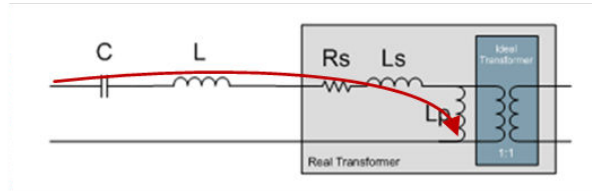
- In-parallel inductance. A typical in-parallel inductance value can be between 750 μH and 1 mH.
- DC Current (I_{DC}). To avoid transformer saturation issues, it is recommended that the transformer be able to manage I_{DC} according to the following inequality:

$$I_{\text{DC}} > 2\pi f_{\text{MAINS}} C_{16} V_{\text{peakMAINS}}$$

Where:

- f_{MAINS} is the frequency of the mains
- C_{16} is the value of the high voltage decoupling capacitor (C16)
- $V_{\text{peak MAINS}}$ is the Peak value of the mains

Figure 3-15. DC Current



3.2.4 Coupling Stage Filter Design

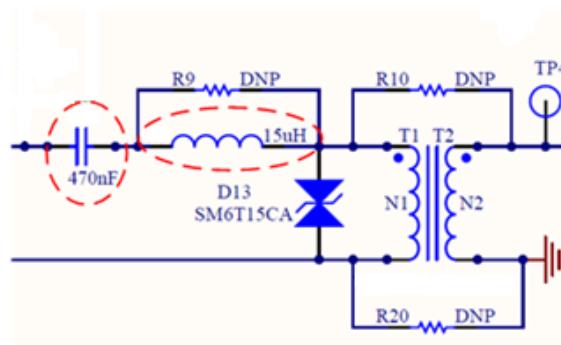
It is recommended that the Coupling Stage circuitry have a resonant frequency as near as possible to the logarithmic center of the transmission band (f_c):

$$f_c = 10^{\left(\frac{\log f_1 + \log f_2}{2}\right)}$$

where f_1 and f_2 are, respectively, initial and final frequencies of the transmission channel.

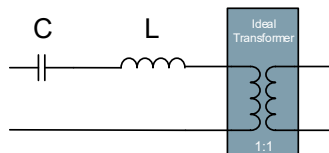
Example: For G3-PLC CENELEC A-band coupling design, $f_1 = 35$ kHz and $f_2 = 91$ kHz.

Figure 3-16. Example of Coupling Stage Composed by C, L and Transformer



3.2.4.1 Isolated Coupling Stage

Figure 3-17. Ideal Isolated Coupling Stage

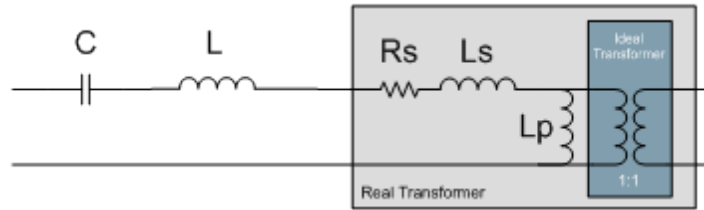


Theoretically, the coupling stage would be composed by just L and C, so the resonant frequency is:

$$f_c = \frac{1}{2\pi\sqrt{LC}}$$

However, a real transformer includes some parasitic components that may affect the behavior of the resonant circuit (mainly L_S , called leakage inductance):

Figure 3-18. Real Isolated Coupling Stage



So the equivalent inductance is L_T :

$$L_T = L + L_S$$

For example, in CENELEC A-band and making use of a capacitor of 470 nF, the inductance for a resonant frequency of 58 kHz is:

$$L_T = \frac{1}{(2\pi f_c)^2 C} = 16\mu\text{H}$$

And so, in case of populating the transformer VAC T60403-K5024-X044 ($L_S \sim 0.3 \mu\text{H}$):

$$L = 16 - L_S \cong 15.7\mu\text{H}$$

In the PL460-EK design files, a 15 μH inductor is used in the primary circuit for the variant of only CENELEC-A, and, when the coupling circuit is double-branch in the secondary circuit, only the CENELEC-A branch is affected.

Figure 3-19. Inductor in Variant CEN-A

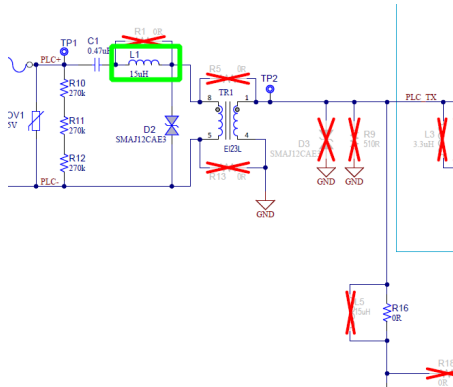
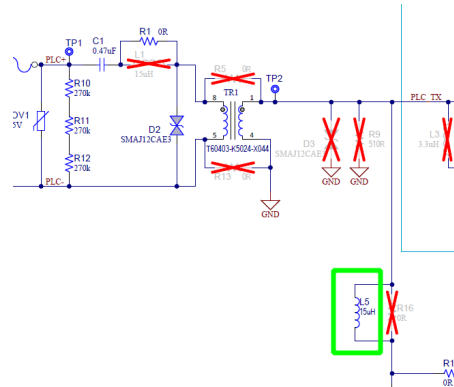


Figure 3-20. Inductor in Variant FCC & CEN-A



3.2.4.2 Non-Isolated Coupling Stage

Removing the PLC transformer ($L_S = 0$) implies that:

$$L_T = L$$

So, the coupling stage is composed by just L and C:

$$f_c = \frac{1}{2\pi\sqrt{LC}}$$

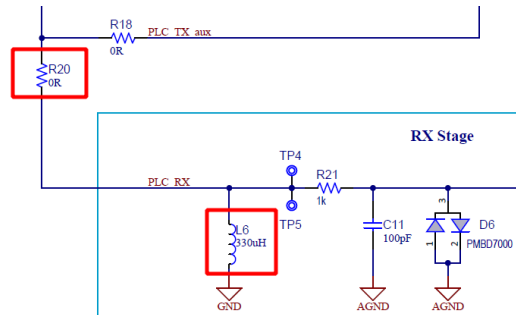
So, selecting the values of the coupling stage filter properly is recommended.

In the case of the PL460-EK, the non-isolated variants must remove the transformer and mount two 0-ohms resistors instead. Due to the low leakage inductance of the transformer VAC T60403-K5024-X044 ($L_S \sim 0.3 \mu\text{H}$), the same

values of the components are used. When one of the branches is going to work in CENELEC-A, two additional modifications are required in the reception stage:

- R20 must increase its value to 10 Ohms
- L6 must be replaced to support a higher saturation current over 200 mA, for example Bourns SRR7045-331

Figure 3-21. Components to Change in a Non-Isolated Variant with CENELEC-A



3.2.5 Path of the DC Current

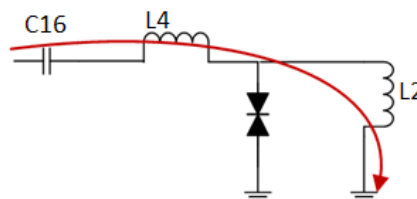
In an isolated coupling, a PLC transformer is populated and the ground path of the DC current goes through the L_p inductance of the transformer, which has a very low DC resistance ($\approx 0,1\Omega$) and supports the required current (see [3.2.3. Isolation Transformer](#)).

Figure 3-22. DC Current



In a non-isolated coupling, removing the transformer implies that the path towards the ground of the DC current is removed, so an inductor is required to let DC current flow to ground: (L2 in the following figure). It is recommended that the inductor be able to support such DC current. For that, a low DC resistance of the inductor is recommended ($< 100\text{ m}\Omega$).

Figure 3-23. DC Current Ground Path in Non-isolated Coupling



To avoid saturation issues, it is recommended that the inductance be able to manage I_{DC} according to the next formula:

$$I_{DC} > 2\pi f_{MAINS} C_{16} V_{peakMAINS}$$

where:

- f_{MAINS} is the frequency of the mains
- C_{16} is the value of the high voltage decoupling capacitor (C16)
- $V_{peakMAINS}$ is the Peak value of the mains

3.3 Switched-Mode Power Supply

3.3.1 Power Requirements

The class-D amplifier of the PLC transmission is powered with a regulated voltage of 12 V_{DC}. When using the embedded driver of the PL460, it is powered through the PVDDAMP pins. The power consumption of the class-D amplifier is not constant, and it creates current peaks during each transmission whose level depends on the load the driver is transmitting to.

Note: Generally, a load of 2Ω is considered the typical impedance seen by the PLC transmitter in a real world scenario.

The PLC modem is powered at 3V3. The 3V3 line is divided in two different paths to power digital and analog parts of the circuitry. This way, noise effects of digital signals are reduced in the analog part of the circuitry.

3.3.2 Switching Frequency

The switching frequency of the Switched-Mode Power Supply (SMPS) must be above the transmission band to avoid performance issues due to the harmonics coming from the power supply.

PRIME channel 1 and G3-PLC CENELEC A-band couplings work with frequencies under 91 kHz, so the switching frequency of the SMPS must not be close to that value. At least, the switching frequency must be greater than 100 kHz to ensure that it does not interfere with the PLC signal.

In the case of higher channels of PRIME (3 to 8) or G3-PLC FCC working band, the switching frequency must be greater than 500 kHz to ensure that it does not interfere with the PLC signal.



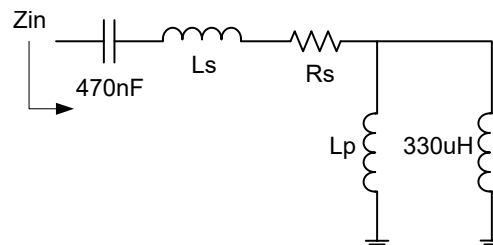
Attention: When using SMPSs with a pulse skipping mode, this functionality modifies the switching frequency of the power supply. It is recommended that the complete range of generated frequencies not interfere with the PLC signal.

3.3.3 Input Impedance

In most cases, the PLC coupling circuit is in parallel with the power supply. In that case, to calculate the value of the input impedance of the final equipment, the PLC input impedance must be taken into account. If the impedance requirements are not satisfied, then an appropriate decoupling filter must be included at the power supply input.

For example, the PLC coupling circuit for CENELEC-A has the following equivalent circuit:

Figure 3-24. Simplified Equivalent Circuit of Coupling for CENELEC-A Band



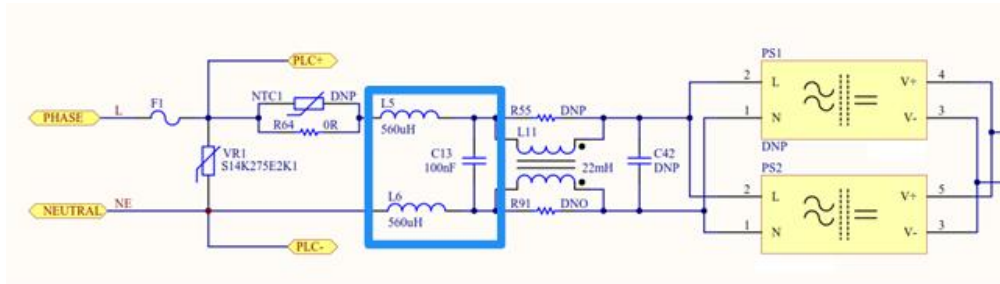
where L_S , R_S and L_P depend on the isolation transformer mounted.

3.3.4 PLC Rejection Filter

To avoid transmitted signal (and also received signals) to be absorbed by the Power Supply, placing a PLC Rejection filter at the input of the Power Supply is recommended. This filter increases the input impedance inside the transmission band, so it helps to achieve the requisites of the previous section, [3.3.3. Input Impedance](#).

It can be composed by two inductance in-series ($L = 560 \mu\text{H}$) and a capacitor in-parallel ($C = 100 \text{ nF}$) as shown in the following picture:

Figure 3-25. PLC Rejection Filter



4. References

- PL360 Data Sheet, 2018
- PL460 Data Sheet, 2020
- Crystal Selection Guidelines for PL360, ATPL230, ATPL250, SAM4CP16B & SAM4CP16C Application Note, 2018
- AVR040 application note, 2016

5. Revision History

5.1 Rev A – 08/2022

Document	Initial document release
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