Application Note

Synchronizing Local Time in Vitesse IEEE 1588v2 PHYs

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first release of this document. It was published in April 2011.

2 Introduction

This document provides a method for synchronizing Vitesse 1588v2 PHYs to a PTP master for ordinary and boundary clock applications, as well as steps for just loading local time without synchronizing to a PTP master.

2.1 References

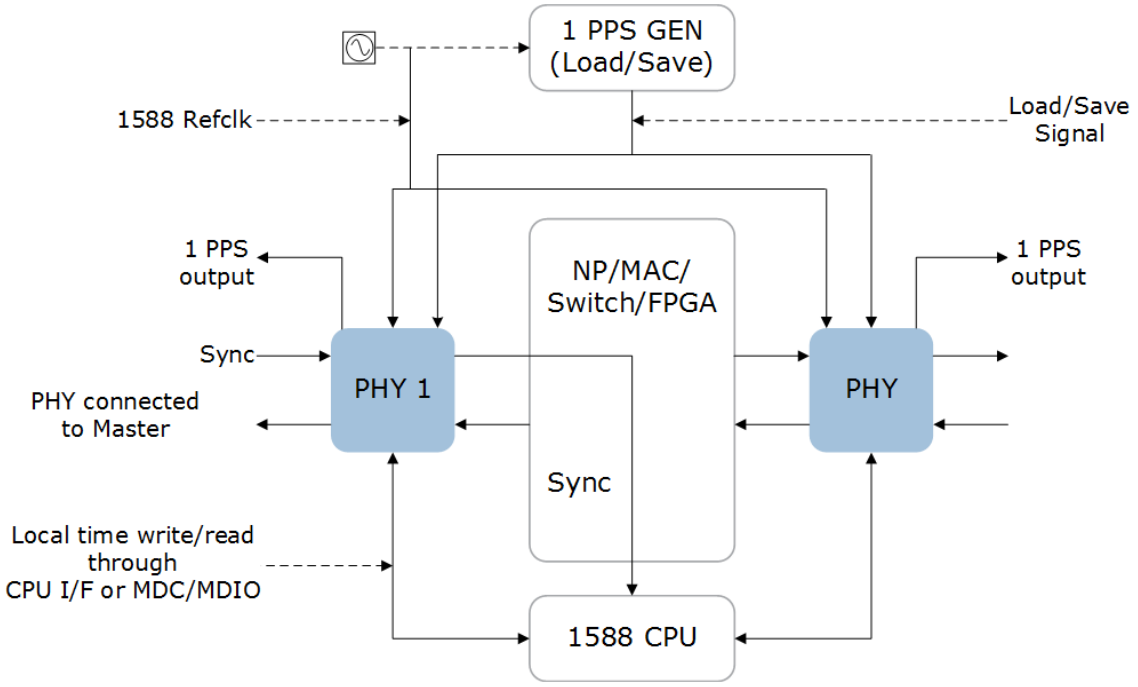
2.1.1 Vitesse Documents

- VSC8492 Dual Channel Universal 10G PHY or 10 GbE PHY with OTN/FEC and IEEE 1588 (http://www.vitesse.com/products/product.php?number=VSC8492)
- VSC8494 Quad Channel Universal 10G PHY or 10 GbE PHY with OTN/FEC and IEEE 1588 (http://www.vitesse.com/products/product.php?number=VSC8494)
- VSC8488-15 Dual Channel WAN/LAN/Backplane XAUI to SFP+/KR Transceiver (http://www.vitesse.com/products/product.php?number=VSC8488)
- VSC8487-15 WAN/LAN/Backplane XAUI to SFP+/KR Transceiver (http://www.vitesse.com/products/product.php?number=VSC8487)

3 Local Time Load and Synchronization

- Local time must be provided to all Microsemi 1588 PHYs through a CPU interface or MDC/MDIO, (see Figure 1). The VSC8492 and VSC8494 use a CPU interface, while all other 1588 PHYs use the MDIO.
- A global load/save signal must be provided to load all PHY counters at the same precise time. The load/save can be a 1 PPS (or low frequency) signal generated from a single timing source, which provides one common signal connected to all PHYs. Generate 1 PPS in hardware with highly accurate time between pulses. This can be done by just dividing down the system reference clock at a central location and distributing the divided down signal (1 PPS) to all 1588 PHYs in the system.
- A global reference clock must be provided to all PHYs so that 1588 counters all progress at the same rate (see the PHY datasheets for frequency requirements). The 1588 reference clock can be an oscillator or derived from a system clock.

Figure 1 • PHY Synchronization Signals



3.1 Synchronizing to a PTP Master

The following steps synchronize and adjust local time in multiple PHYs to a PTP master for ordinary and boundary clock applications (Figure 2 shows the same steps in a flow diagram).

1. The 1588 CPU receives Sync frames time stamped (Rx timestamp) by the ingress PHY1 connected to the PTP master. The CPU then goes through the full IEEE 1588 procedure of exchanging PTP messages (Delay_Req and Delay_Resp) to calculate offset from the master. Normally this procedure of exchanging PTP messages is repeated several times and packet delay variation (PDV) filtering algorithm is applied to filter out delay variation.
2. The 1588 CPU sets the save bit in PHY1, and reads the saved local time (t0). Local time is saved in the LTC registers on the next load/save pulse.
   The local time format is Unsigned 48-bit (s) || Unsigned 32-bit (ns)
3. The CPU calculates expected time (t1) at the next load/save pulse corrected by the offset. The next load/save pulse can be one or more 1 PPS periods (tp).

   t1 = saved local time (t0) + Offset + tp
4. The CPU writes the expected time (t1) into PHY1, and then sets the load bit. Local time is loaded into the local time counter on the next load/save pulse.

5. The CPU checks that the offset is now zero. If not, it adjusts the local time with the ± ns function until the offset is zero.
6. The CPU sets the “save” bit on PHY1 and then reads the local time (t2).
   The CPU then writes all other PHYs with the saved local time t2 + next load pulse (tp) + trace delay (td), and then sets the load bit in each PHY. Local time is loaded into all PHYs on the next pulse on the load/save pin. Td is the known PCB trace delay on the load/save pin for each PHY.
   In most cases the CPU can load all PHYs within one load/save time period (typically one second). If not, this procedure can be done in multiple steps over multiple load/save periods.
7. The CPU sets the save bit in all PHYs, reads back local time values, and checks to make sure all values are the same.
8. The CPU continuously checks the local time drifts compared to the recovered PTP time.

   - It corrects local time by issuing ± ns commands to all PHYs
   - The PHYs can also be programmed to automatically adjust for PPM differences when local time is drifting at a fixed rate compared to the PTP time

   Notes:
   Related registers: LTC_SAVE_ENA in LTC_CTRL and LTC_LOAD_ENA in LTC_CTRL, LTC_SAVED_SEC_H, LTC_SAVED_SEC_L, LTC_SAVED_NS, LTC_LOAD_SEC_H, LTC_LOAD_SEC_L, and LTC_LOAD_NS.

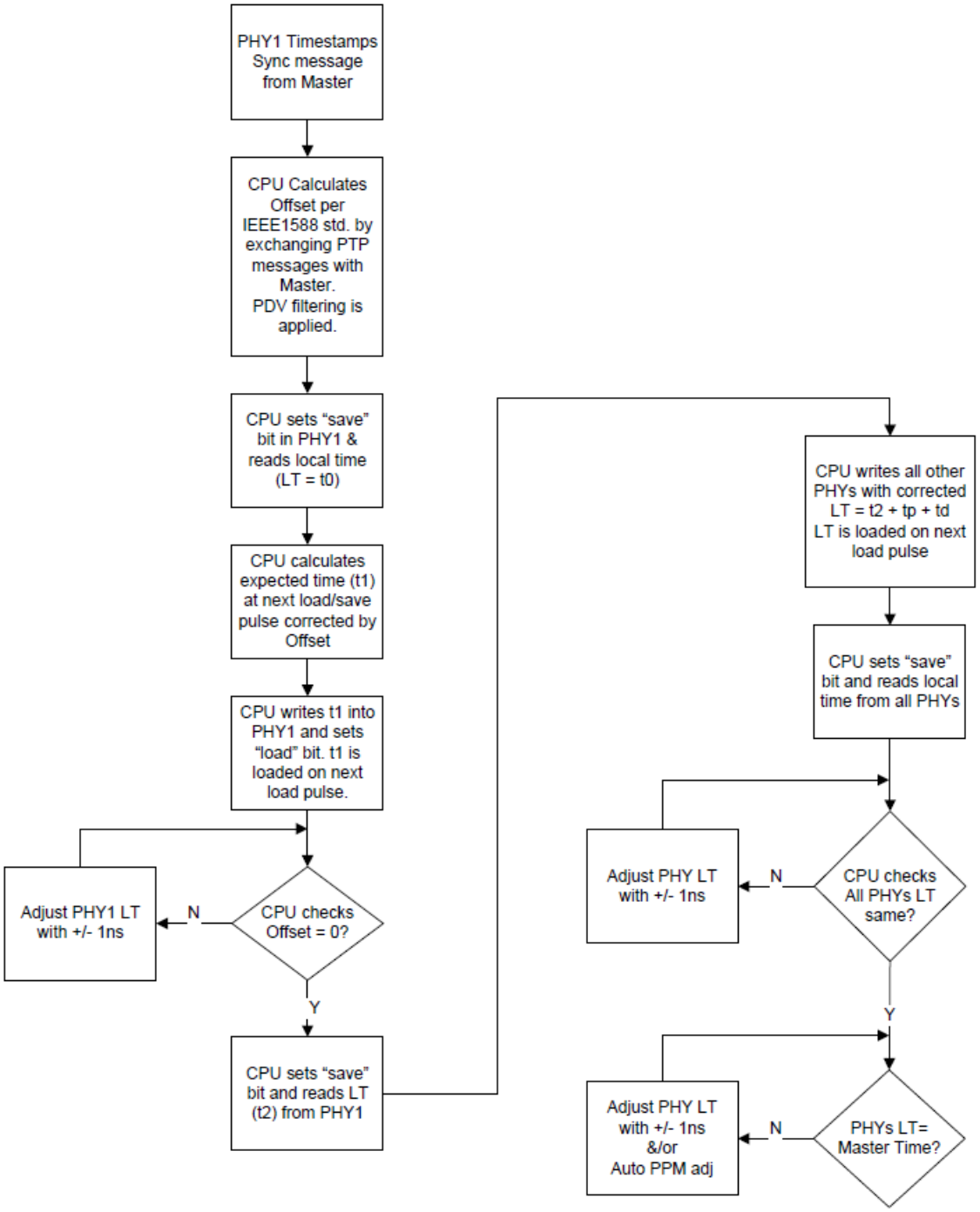
   The PHYs support two methods for local time and/or PPM adjustment: the ±1 ns function with the CPU, and automatic PPM adjustments.

   a. Using the ±1 ns function: To support adjustments on an as needed basis, the CPU issues a ±1 ns command which adds or subtracts 1 ns from the local time counter.
   b. Automatic PPM adjustment: The PPM offset can be used to calculate how many local time clocks it takes to reach an offset of 1 ns. This value along with an add/subtract value can be programmed into the PHY for automatic PPM adjustments.

      For example, automatic adjustment calculation, if the local counter clock is 250 MHz and is off by 100 PPM (0.01%), then the 4 ns period is off by 0.0004 ns every cycle. There needs to be an adjustment every 1 ns/0.0004 ns = 2500 cycles. The programmed value would be set to 2500×4 = 10,000.

The PHYs also have a 1 PPS output pin that provides an equally spaced sync pulse that can be used to measure timing skew between PHYs. It is possible to measure the nominal correction values, which can be incorporated into the systems software, by measuring the skew between the 1 PPS test output from each PHY. Variation due to temperature and system differences should be minimized.

Figure 2 • Set and Adjust PHY Local Time to Master PTP Time



3.2 Loading Local Time Without PTP Master

The following steps load local time in multiple PHYs without synchronizing local time to a master.

1. The CPU writes all PHYs with local time at the **NEXT** Load/Save pulse, then sets the "load" bit in each PHY. This time includes known PCB trace delay on the Load/Save pin for each PHY. Local time is loaded into all PHYs on the next pulse on the Load/Save pin.
   In most cases the CPU can load all PHYs within one load/save time period (typically one second). If not, this procedure can be done in multiple steps over multiple load/save periods.
2. The CPU sets the "save" bit in all PHYs, reads back local time values, and checks to make sure all values are the same. The CPU adjusts each PHY local time using the ± ns function as necessary.

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