AVR32138: How to optimize the ADC usage on AT32UC3A0/1, AT32UC3A3 and AT32UC3B0/1 series

1 Introduction

This application note outlines the steps necessary to optimize analog to digital conversions on AT32UC3A0/1, AT32UC3A3 and AT32UC3B0/1 series. The ADC is useful in measuring output voltages of i.e. analog sensors and converting them to digital values. There are however considerations during design and implementation which impacts the conversion quality.

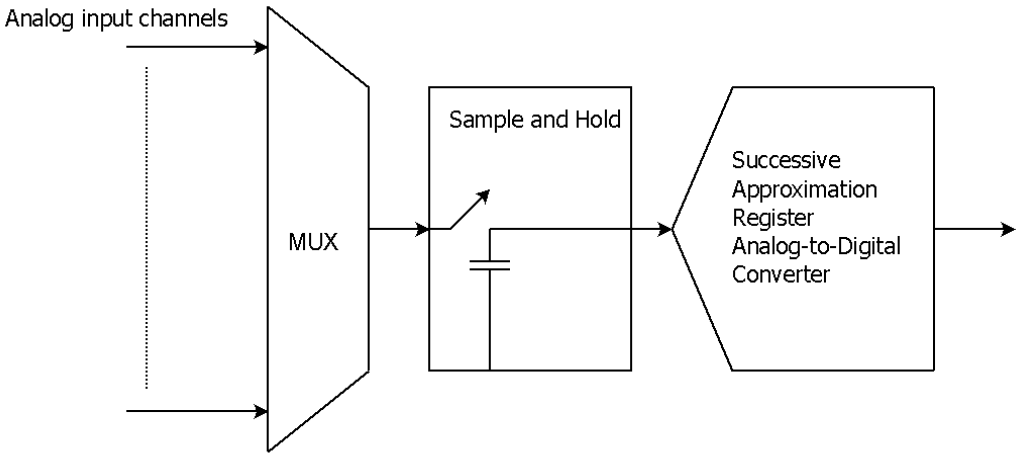
32-bit AVR® Microcontrollers

Application Note

Rev. 32135A-AVR32-11/09

2 System Model

Figure 2-1. ADC controller Schematic



3 Acquisition Time (Sample and Hold)

A number of steps are required during an analog-to-digital conversion. When an analog-to-digital conversion begins, one channel select switch is closed (MUX), allowing the sample and hold capacitor to charge. The channel select switch is then opened. The charge applied to the sample and hold capacitor is then converted into a digital representation by the successive approximation register.

The acquisition time is related to the sample and hold time which is configurable with a dedicated SHTIM bit field in the Mode Register MR. SHTIM can be set from 0x0 to 0xF and consequently change the sample and hold time from the following equation:

Sample & Hold Time = (SHTIM+3) / ADCClock

The ADC Clock frequency is selected in the PRESCAL field of the MR register.

For example: given

SHTIM = 0x0

ADCClock = 5 MHz (Max Freq for 10 bits resolution)

Then the sampling time is:

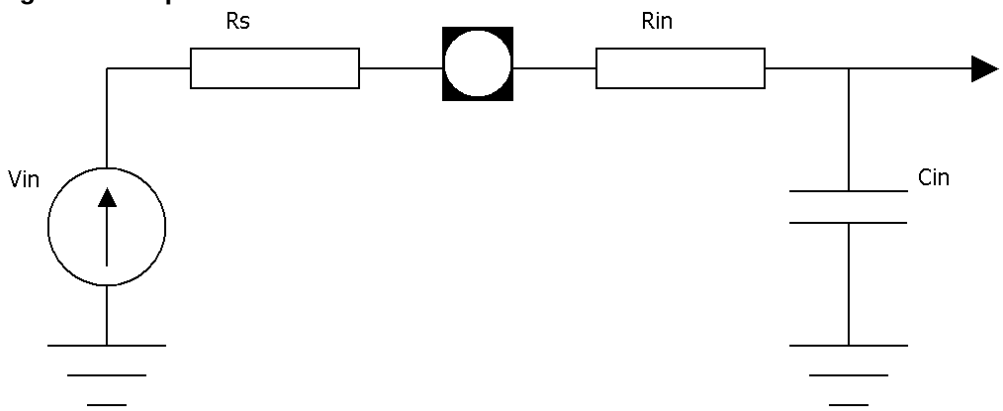
Ts (Sample & Hold Time) = (0+3) / 5 000 0000

= 600 ns

Note that SHTIM will directly impact the conversion rate of the ADC as it comes in addition to the conversion time itself.

4 How to select the Source Impedance

Figure 4-1. Equivalent schematic



The external resistance of the source (Rs) feeding the sample and hold capacitor will determine the charging value. The goal to achieve is to have the sample and hold capacitance charged to a voltage value Vin ± (Vin/Resolution) at the end of the sampling period.

The Worst case appears when Cin is completely discharged and Vin is maximum ADC input voltage. To account for these two worst-case, it is important that the source impedance does not exceed a maximum value.

The capacitor charging time is related to the RC value and the input voltage.

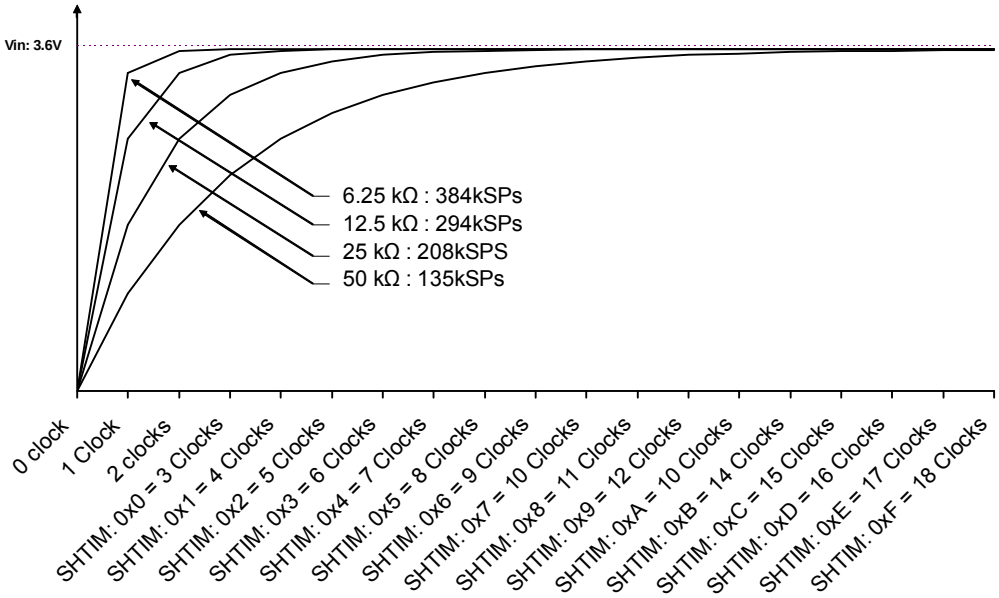
$$VCin = Vin \times (1 - exp(-t / ((Rs+Rin) \times Cin)))$$
$$Ts = (SHTIM+3) / ADCClock$$

We want :

$$VCin > Vin - (Vin / 2^{10})$$
$$Vin \times (1 - exp(-t / ((Rs+Rin) \times Cin))) > Vin - (Vin / 2^{10})$$
$$Vin \times (1 - exp(-t / ((Rs+Rin) \times Cin))) > Vin \times (1- (1 / 2^{10})$$
$$1 - exp(-t / ((Rs+Rin) \times Cin)) > 1- (1 / 2^{10})$$
$$1 / 2^{10} > exp(-Ts / ((Rs+Rin) \times Cin))$$
$$ln (1 / 2^{10}) > -Ts / ((Rs+Rin) \times Cin)$$
$$Ts / C > (Rs+Rin) \times ln (2^{10})$$
$$Rs+Rin < Ts / (C \times ln (2^{10}))$$

Considering the Rin value as negligible (see electrical characteristics section of the datasheet), we see that Rs is directly impacted by the S/H time and vary from ~ 7kΩ (SHTIM= 0) to 43kΩ (SHTIM= 15).

Figure 4-2. Charging Time vs. Rs when ADC clock @5MHz



5 Solutions

To remain compliant with the sampling time constraint, the solutions are:

1. Minimize the total source impedance seen by the analog input channels:
   - The maximum value of the total source impedance should be around 43kOhms in order to reach the Vin-1LSB (given SHTIM set to the maximum 0xF). Nevertheless, the smaller the total source impedance, the faster the acquisition time. Therefore the sensor should be chosen with the lowest output impedance. The figure 4-2 can be used as reference.
   - Adding an impedance adapter interface (operational amplifier …) between the Analog source and the ADC input can be another alternative to lower the total source impedance.
2. Slow down the ADC clock frequency :

   The period time is increased, therefore the sample and hold time is consequently raised, allowing for a more complete charge of the capacitor. Nevertheless in this case the quantity of sample per second is decreased.

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