How to Replace Infineon SABC505C/CA by Atmel T89C51CC01 CAN Microcontroller

CAN Microcontrollers

Application Note

Infineon Technologies® developed a family of C500 core 8051 compatible micro-controllers running with the standard 80C51 12 clocks per cycle. Peripherals such as Controller Area Network (CAN: BOSCH Standard) and capture and compare channels are common blocks on several derivatives.

The Atmel approach on the new C51X2 core used in the T89C51CC01 has been to run all instructions at 6 or 12 clocks per cycle without changing the number of cycles for each instruction. The feature of running 6 or 12 clocks per cycle is a programmable feature.

Infineon implements some features such as: dual data pointer, Watchdog etc. in a way not compatible with the other sources of C51 micro-controllers such as Philips or Atmel. The Infineon and Atmel CAN controllers while both are BOSCH® standard are implemented with different features and the software drivers will be different as well as the Interrupt Service Routines (ISR) to handle the implementation of such protocols as Allen Bradley/Rockwell DeviceNet™ for OSI layers 2 Logical Link Control (LLC) and layers 3 through 7, using the CAN OSI layers 2 Media Access Control (MAC) and layer 1 Physical Layer Signaling (PLS). Explaining how to adapt software to the Atmel T89C51CC01 is the primary objective of this application note.

Finally, Infineon implements some specific features such as eight 8 data pointers for faster and more efficient external code access. These features are not found in standard implementation of the C51 architecture. The standard 8051 uses a single data pointer while both the Atmel and Philips implement an 8051 superset of compatible dual data pointers. The following application note lists these distinctly different features and suggests software workarounds or at the minimum how the nonstandard feature must be deleted to migrate to the Atmel T89C51CC01.

The primary focus of the application note will be the migration of software written for the Infineon SABC505C/CA to the Atmel T89C51CC01 specifically using the on-chip CAN Controller. Secondarily, this application note will suggest the ways to design with the Atmel T89C51CC01 from the start to take advantage of the features of both the X2 Core and the Atmels' CAN controllers' features.

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Features List

The following table lists all features present on SABC505C/SABC505CA and TS89C51CC01.

Table 1. SABC505C/SABC505CA and T89C51CC01 Features

Feature	Description	Infineon C505C	Infineon C505CA	Atmel T89C51CC01
Five I/O ports	Ports 0, 1, 2, 3, 4 (32 + 2 digital I/O)	Y	Y	Y
Three 16 bit timer/counters Timer 2 Capture and compare	Timer 0, 1, 2 Channels of 16 bit capture and compare	Y 4	Y 4	Y 5 PCA
Internal Program Memory	Memory Space Memory Type Boot loader CAN ISP (Usart ISP optional)	16KB ROM NA	32KB OTP NA	32KB FLASH w/ISP 2K Flash (1)
Internal Data Memory	RAM XRAM User available XRAM when using CAN EEPROM (re-programmable data memory)	256 bytes 256 bytes 128 bytes 0	256 bytes 1 kbytes 768 bytes 0	256 bytes 1kbytes 1k bytes 2k bytes
Multiple Data Pointers	DPTR0, DPTR1, …….	8	8	2
Emulation Using Enhanced Hooks	Emulators use production chips on pods	Y	Y	Y
Power Save Modes	Slow Down Mode Idle mode (peripheral operating) Power Down Mode	Y Y Y	Y Y Y	N Y Y
Power Supply	Voltage	5 V	5 V	5 V
Maximum Frequency CAN (min f_{OSC}) X2 Mode Mode Switching X1 or X2 for Peripherals Stretch MOVX	Mode X1 or standard 12 clock cycles per machine cycle With CAN baud = 1000K Baud Max Mode X2 or 6 clock cycles per machine cycle Mode switching after reset Peripherals individual switch-able X1 or X2 mode Stretch the RD and WR cycles for slow peripherals in X2 mode using M0 bit in SFR AUXR	20 MHz 8 MHz w/o prescaler NO NO NO NO	20 MHz 8 MHz w/o prescaler NO NO NO NO	33 MHz 8 MHz X2 20 MHz(2) YES YES YES
Programmable Watchdog	Number of bits for resolution and timing Oscillator Watch dog	15 bits Y	15 bits Y	21 bits N
Full duplex UART	8 bit UART in 3 Full duplex modes Automatic address recognition, Support Framing Error	Y N	Y N	Y Y
Analog to Digital Converter	Channels and number of bits Reference of ADC Minimum conversion time (depends on f_{OSC} and Clk/prescaler)	8 c / 8 bits 5 V 8 µs	8 c / 10 bits 5 V 6 µs	8 c / 10 bits 5-3 V 16 µs
External Interrupt Sources		6	6	2
Interrupt Priority Levels	Priority and levels programmable for each interrupt sources	4 / 12	4 / 12	4 / 14

Table 1. SABC505C/SABC505CA and T89C51CC01 Features (Continued)

Feature	Description	Infineon C505C	Infineon C505CA	Atmel T89C51CC01
Packages	Type available	P-MQFP-44	P-MQFP-44	PLCC-44 TQFP-44 CABGA-64
Temperature	Commercial (0-70); Industrial (-40-85); Extend (-40-110); Auto(-40-125) °C	C,I,Extend, Auto	C,I, Auto	Industrial
CAN Module on chip	CAN Version	2.0B Active	2.0B Active	2.0B Active
	CAN SFR locations and 15 Message objects	128 bits XRAM	128 bits XRAM	direct SFR
	Speed of access to CAN control registers	MOVX slower	MOVX slower	MOV direct faster
	CAN Time stamp Tx and Rcv	NO	NO	YES 16 bits timer
	Time Trigger Communication (TTC) Protocol	NO	NO	YES
	CAN listening mode for writing Auto-baud software	NO	NO	YES
	CAN Buffer mode with assignable channels w/ Interrupt overflow	NO	NO	YES
	Configurable Bit Rate Timing	YES	YES	YES

Notes: 1. Separate from 32K Flash.
2. 40 MHz Equivalent in X2 mode.

Pinout

The following table shows the SABC505C/CA and T89C51CC01 pinout. (NAMEb to indicate active low signal).
The Atmel T89C59CC01 pinout has been optimized for noise immunity and differs from the standard C51 pinout.

Table 2. SABC505C/SABC505CA and T89C51CC01 Pinout

Infin.	Atmel					
MQFP	PLCC44	TQFP44	CA-BGA 68	Signal Name	Difference in Infineon C505C/CA	Description / comment or difference in Atmel T89C51CC01
17	42	36	B5,B6	Vcc	No difference	Positive Supply
16	43	37	A5,A6	Vss		Ground.
4	44	38	D5	RST	Infineon hold high for 1 machine cycle (12 Osc cycles)	Reset. Atmel must have high level for two machine cycles. (12 Osc Cycles X2 and 24 Osc Cycles X1) Need external capacitor to V_{CC} .
14 15	40 41	34 35	A8 A7	XTAL2 XTAL1	No difference	Xtal1 is the input of the oscillator inverter, Xtal2 is the output
26	38	32	C7	PSENb	No difference	Program Store Enable (b to indicate active low)
27	39	33	B8	ALE	ALE disabled by Infineon bit EALE =1 and EA=1	Address Latch Enable. When instructions executed in Flash (Eab = 1) then ALE can be disabled by A0 bit in AUXR. ALE 1/6 Osc period X1 mode 1/3 in X2 mode.
37 36 35 34 33 32 31 30	30 31 32 33 34 35 36 37	24 25 26 27 28 29 30 31	G8 F7 E7 F8 E8 D8 D7 C8	P0.0/AD0 P0.1/AD1 P0.2/AD2 P0.3/AD3 P0.4/AD4 P0.5/AD5 P0.6/AD6 P0.7/AD7	No difference	AD0-7 Port0 is the multiplexed address bus
  40 41 42 43 44 1 2 3	 3 4 5 6 7 8 9 10	 41 42 43 44 1 2 3 4	 A3 B3 A2 B2 A1 B1 C2 C1	Port1 P1.0 P1.1 P1.2 P1.3 P1.4 P1.5 P1.6 P1.7	Port Alternate Function Infineon P1.0 AN0, INT3b, **CC0** P1.1 AN1, INT4, **CC1** P1.2 AN2, INT5, **CC2** P1.3 AN3, INT6, **CC3** P1.4 AN4 P1.5 AN5, **T2EX** P1.6 AN6, **CLKOUT** P1.7 AN7, **T2** Differences use CCU or + 4 external interrupts; CCU vs. PCA Atmel	Port Alternate Function Atmel P1.0 AN0,**T2** I/O Timer/cntr2/Anolog 0 P1.1 AN1,**T2EX** Timer/Counter2 Capture/Reload, Analog channel 1 P1.2 AN2,**ECI** Analog 2, PCA ext Clk input P1.3 AN3,**CEX0** Analog 3, PCA module 0 input or PWM output P1.4 AN4,**CEX1** Analog 4, PCA Module 1 P1.5 AN5, **CEX2** Analog 5, PCA Module 2 P1.6 AN6, **CEX3** Analog 6, PCA Module 3 P1.7 AN7, **CEX4** Analog 7, PCA Module 4
18 19 20 21 22 23 24 25	29 28 27 26 25 24 23 22	23 22 21 20 19 18 17 16	H8 H7 G6 H6 G5 H5 H4 H3	A8 (P2.0) A9 (P2.1) A10 (P2.2) A11 (P2.3) A12 (P2.4) A13 (P2.5) A14 (P2.6) A15 (P2.7)	No difference	A15-A8 (Port2)

Table 2. SABC505C/SABC505CA and T89C51CC01 Pinout (Continued)

Infin.	Atmel					
MQFP	PLCC44	TQFP44	CA-BGA 68	Signal Name	Difference in Infineon C505C/CA	Description / comment or difference in Atmel T89C51CC01
				Port3		Port Alternate Function Atmel
5	12	6	E1	P3.0	No difference	P3.0 RXD0 Serial Port0 input
7	13	7	E2	P3.1	No difference	P3.1 TXD0 Serial Port0 output
8	14	8	F1	P3.2	No difference	P3.2 INT0b External interrupt 0
9	15	9	F2	P3.3	No difference	P3.3 INT1b External interrupt 1
10	16	10	G1	P3.4	No difference	P3.4 T0 Timer0 input
11	17	11	G2	P3.5	No difference	P3.5 T1 Timer1 input
12	18	12	H1	P3.6	No difference	P3.6 WRb External Data Memory Write
13	19	13	H2	P3.7	No difference	P3.7 RDb External Data Memory Read
29	11	5	D1	EAb	No difference	External Access (b to indicate active low)
38	2	40	B4	V_{AREF}	Reference Voltage for A/D	
39	1	39	A4	VA_{GND}	Reference Ground for A/D	
6	20	14	G3	P4.0, TxDC	No difference	Port 4.0 IO or Transmit Data CAN
28	21	15	G4	P4.1, RxDC		Port 4.1 IO or Receive Data CAN

Note. C505C/CA has CAN Tx and Rcv pins on the opposite side of the chip versus the Atmel configuration with the CAN signals on adjacent pins. The Atmel configuration provides the shortest layout to the CAN transceiver thereby minimizing the trace length.

SFR Memory Map

Major differences occur in the Special Function Registers map of the Atmel T89C51CC01 and the Infineon SABC505C/CA due to the Atmel use of the SFRs for the CAN control and message object registers. The following tables will identify the Atmel SFR's, the Infineon SFR's and a difference table. For the CAN specific peripherals' Special Function Registers there will be a mapping comparison with a detailed explanation of the differences for ease of implementation or conversion.

Atmel T89C51CC01

The following table lists the Atmel T89C51CC01 Special Function Registers. The CAN specific Special Function Registers are contained in the SFR table which allows for faster direct addressing for the CAN peripheral software.

Table 3. T89C51CC01 SFR Mapping

ADDR	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	ADDR.
F8h	**IPL1** **XXXX X000**	CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		FFh
F0h	**B** **0000 0000**		ADCLK xx00 0000	ADCON x000 0000	ADDL 0000 0000	ADDH 0000 0000	ADCF 0000 0000	IPH1 xxxx x000	F7h
E8h	**IE1** **xxxx x000**	CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000		EFh
E0h	**ACC** **0000 0000**								E7h
D8h	**CCON** **00xx xx00**	CMOD 00xx x000	CCAPM0 x000 000	CCAPM1 x000 000	CCAPM2 x000 000	CCAPM3 x000 000	CCAPM4 x000 000		DFh
D0h	**PSW** **0000 000**	FCON 0000 0000	EECON xxxx xx00						D7h
C8h	**T2CON** **0000 000**	T2MOD xxx xx00	RCAP2L 0000 000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000	CANEN1 xx00 000	CANEN2 0000 0000	CFh
C0h	**P4** **XXXX XX11**	CANGIE 0000 0000	CANIE1 xx00 0000	CANIE2 0000 0000	CANIDM1 xxxx xxxx	CANIDM2 xxxx xxxxx	CANIDM3 xxxx xxxxx	CANIDM4 xxxx xxxx	C7H
B8h	**IPL0** **x000 000**	SADEN 0000 0000	CANSIT1 0x00 0000	CANSIT2 0000 0000	CANIDT1 xxxx xxxx	CANIDT2 xxxx xxxxx	CANIDT3 xxxx xxxxx	CANIDT4 xxxx xxxxx	BFh
B0h	**P3** **1111 1111**	CANPAGE 0000 0000	CANSTCH xxxx xxxx	CANCONCH xxxx xxxx	CANBT1 xxxx xxxx	CANBT2 xxxx xxxx	CANBT3 xxxx xxxx	IPH0 x000 0000	B7h
A8h	**IE0** **0000 0000**	SADDR 0000 0000	CANGSTA x0x0 000	CANGCON 000 x000	CANTIML 0000 0000	CANTIMH 0000 0000	CANSTMPL 0000 0000	CANSTMPH 0000 0000	AFh
A0h	**P2** **1111 1111**	CANTCON 0000 0000	AUXR1 0000 0000	CANMSG xxxx xxxx	CANTTCL 0000 0000	CANTTCH 0000 0000	WDTRST 1111 1111	WDTPRG xxxx x000	A7h
98h	**SCON** **0000 0000**	SBUF 0000 0000		CANGIT 0x00 0000	CANTEC 0000 0000	CANREC 0000 0000			9Fh
90h	**P1** **1111 1111**								97h
88h	**TCON** **0000 000**	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR 0000 1000	CKCON 0000 0000	8Fh
80h	**P0** **1111 1111**	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 0000 0000	87h

Note: The bold registers are bit addressable. And reset values indicated.

Infineon C505C

Table 4. Infineon C505C SFR Mapping

ADDR	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	ADDR.
F8h					(1)	(1)	(1)		FFh
F0h	B 0000 0000								F7h
E8h	**P4** **XXXX XX11**								EFh
E0h	ACC 0000 0000								E7hh
D8h	**ADCON0** **00X0 0000**	**ADDAT** **0000 000**	**ADST** **XXXX XXXX**		**ADCON1** **01XX X000**				DFh
D0h	PSW 0000 000								D7h
C8h	T2CON 0000 000		**CRCL** **0000 0000**	**CRCH** **0000 000**	**TL2** **0000 0000**	**TH2** **0000 000**			CFh
C0h	**IRCON** **0000 000**	**CCEN** **0000 0000**	**CCL1** **0000 0000**	**CCH1** **0000 0000**	**CCL2** **0000 0000**	**CCH2** **0000 0000**	**CCL3** **0000 0000**	**CCH3** **0000 0000**	C7H
B8h	**IEN1** **0000 0000**	**IP1** **xx00 0000**	**SRELH** **xxxx xx11**						BFh
B0h	P3 1111 1111	**SYSCON** **xx10-0x01**							B7h
A8h	**IEN0** **0000 0000**	**IP0** **0000 0000**	**SRELL** **1101 1001**						Afh
A0h	P2 1111 1111								Afh
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 (1) 1111 1111	**XPAGE** **0000 0000**	**DPSEL** **XXXX X000**						97h
88h	TCON (1) 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000			8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000			**WDTREL** **0000 0000**	**PCON** **0000 0000**	87h

Bold Type denotes the registers in the Infineon C505C/CA that are different than the Atmel T89C51CC01. The XPAGE, DPSEL, and WDTREL are unused SFR's locations for Atmel. The SYSCON, ADDAT, ADSL are slightly different in C505C and C505CA. (see the data sheet)

Note (1) At this address there is a register located in the mapped SFR area (see Below). To access this area the RMAP bit in SYSCON must be set and cleared when necessary.

ADDR	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	ADDR.
F8h					**VR0 C5h**	**VR1 05h**	**VR2 XXh**		FFh
90h	**P1ANA 1111 1111**								97h
88h	**PCON1 0XX0 XXXX**								8Fh

Value in VR0,1,2 are read only and contents in VR2 varies with the silicon step (e.g. 01h for the 1st step).

Differences on SFRs

ADDR	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	ADDR.
B0h		**SYSCON XX10-0001**							B7h

CSWO CAN Controller Switch-off bit3 of SYSCON register cuts off the system clock to the CAN module and the SFR's for CAN are not accessible. Default =0 CAN controller is enabled.

ADDR	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	ADDR.
D8h		**ADDATH 0000 000**	**ADDATL 00xx xxxx**						DFh

C505CA with 10 bit A/D has different registers D9h DAh

The Infineon CAN SFR's are in 256 bytes of XRAM from address F700h-F7FE in the following organization.

Table 5. Infineon C505/CA CAN General SFR's Mapping to XRAM

ADDR	Mnemonic/ Name	7	6	5	4	3	2	1	0
F700h	**CR** CAN Control Register	TEST	CCE	0	0	EIE	SIE	IE	INIT
F701h	**SR** CAN Status Register	BOFF	EWRN	-	RXOK	TXOK	LEC2	LEC1	LEC0
F702h	**IR** CAN Interrupt Register	INTID7	INTID6	INTID5	INTID4	INTID3	INTID2	INTID1	INTID0
F704h	**BTR0** Bit Timing Register Low	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
F705h	**BTR1** Bit Timing Register High	0	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
F706h	**GMS0** Global Mask Short Register Low	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
F707h	**GMS1** Global Mask Short Register High	ID20	ID19	ID18	1	1	1	1	1
F708h	**UGML0** Upper Global Mask Long Register Low	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
F709h	**UGML1** Upper Global Mask Long Register High	ID20	ID19	ID18	ID17	ID16	ID15	ID14	ID13

Table 5. Infineon C505/CA CAN General SFR's Mapping to XRAM (Continued)

ADDR	Mnemonic/ Name	7	6	5	4	3	2	1	0
F70Ah	**LGML0** Lower Global Mask Long Register Low	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5
F70Bh	**LGML1** Lower Global Mask Long Register High	ID4	ID3	ID2	ID1	ID0	0	0	0
F70Ch	**UMLM0** Upper Mask of Last Message Register Low	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
F70Dh	**UMLM1** Upper Mask of Last Message Register High	ID20	ID19	ID18	ID17	ID16	ID15	ID14	ID13
F70Eh	**LMLM0** Lower Mask of Last Message Register Low	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5
F70Fh	**LMLM1** Lower Mask of Last Message Register High	ID4	ID3	ID2	ID1	ID0	0	0	0

Table 6. Infineon C505C/CA CAN Message Object Registers (1-15) SFR's Mapping to XRAM

ADDR	Mnemonic/ Name	7	6	5	4	3	2	1	0
F7n0h	**MCR0** Control Register Low	MSGVAL1	MSGVAL0	TXIE1	TXIE0	RXIE1	RX1E0	INTPND1	INTPND0
F7n1h	**MCR1** Control Register High	RMTPND1	RMTPD0	TXRQ1	TXRQ0	MSGLST CPUUPD1	MSGLST CPUUPD0 s	NEWDAT1	NEWDAT0
F7n2h	**UAR0** Upper Arbitration Register Low	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
F7n3h	**UAR1** Upper Arbitration Register High	ID20	ID19	ID18	ID17	ID16	ID15	ID14	ID13
F7n4h	**LAR0** Lower Arbitration Register Low	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5
F7n5h	**LAR1** Lower Arbitration Register High	ID4	ID3	ID2	ID1	ID0	0	0	0
F7n6h	**MCFG** Message Configuration Register	DLC3	DLC2	DCL1	DCL0	DIR	XTD	0	0
F7n7h	**DB0** Message Data Byte 0	DB0.7	DB0.6	DB0.5	DB0.4	DB0.3	DB0.2	DB0.1	DB0.0
F7n8h	**DB1** Message Data Byte 1	DB1.7	DB1.6	DB1.5	DB1.4	DB1.3	DB1.2	DB1.1	DB1.0
F7n9h	**DB2** Message Data Byte 2	DB2.7	DB2.6	DB2.5	DB2.4	DB2.3	DB2.2	DB2.1	DB2.0
F7nAh	**DB3** Message Data Byte 3	DB3.7	DB3.6	DB3.5	DB3.4	DB3.3	DB3.2	DB3.1	DB3.0
F7nBh	**DB4** Message Data Byte 4	DB4.7	DB4.6	DB4.5	DB4.4	DB4.3	DB4.2	DB4.1	DB4.0
F7nCh	**DB5** Message Data Byte 5	DB5.7	DB5.6	DB5.5	DB5.4	DB5.3	DB5.2	DB5.1	DB5.0
F7nDh	**DB6** Message Data Byte 6	DB6.7	DB6.6	DB6.5	DB6.4	DB6.3	DB6.2	DB6.1	DB6.0
F7nEh	**DB7** Message Data Byte 7	DB7.7	DB7.6	DB7.5	DB7.4	DB7.3	DB7.2	DB7.1	DB7.0

Note: N =1-F for XRAM addresses for CAN Message Objects (Atmel CAN Channels) 1-15

Table 7. Comparison of SFR's Except CAN

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ADDR.	Comment for T89C51CC01
Core C51 SFRs										
ACC									E0h	Same on T89C51CC01
B									F0h	Same on T89C51CC01
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h	Same on T89C51CC01
SP									81h	Same on T89C51CC01
DPL									82h	Same on T89C51CC01
DPH									83h	Same on T89C51CC01
I/O Port SFR's										
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h	Port0 same on T89C51CC01
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h	Same on T89C51CC01
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h	Same on T89C51CC01
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h	Same on T89C51CC01
P4 P4							P4.1 P4.1	P4.0 P4.0	E8h C0h	Infineon C505C/CA T89C51CC01 different addr
Timers SFRs										
WDTREL	WDT PSEL	0	0	0	0	0	0	0	86h	**C505C ONLY** WDTPSEL bit replaced by WDT duration bits S0-2 bits in WDTPRG (A7h**). No register at adr. 86h in T89C51CC01**
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h	Same on T89C51CC01
TMOD	GATE	C/Tb	M1	M0	GATE	C/Tb	M1	M0	89h	Same on T89C51CC01
TL0									8Ah	Same on T89C51CC01
TL1									8Bh	Same on T89C51CC01
TH0									8Ch	Same on T89C51CC01
TH1									8Dh	Same on T89C51CC01
WDTRST									A6h	**T89C51CC01 ONLY**
WDTPRG	-	-	-	-	-	S2	S1	S0	A7h	T89C51CC01 ONLY
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2b	CP/RL2	C8h	Same on T89C51CC01
T2MOD	-	-	-	-	-	-	T2OE	DCEN	C9h	T89C51CC01 ONLY
RCAP2L									CAh h	Same on T89C51CC01
RCAP2H									CBh	Same on T89C51CC01
TL2									CCh	Same on T89C51CC01
TH2									CDh	Same on T89C51CC01

Table 7. Comparison of SFR's Except CAN (Continued)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ADDR.	Comment for T89C51CC01
Serial I/O Ports SFRs										
SCON	FE/SM0 SM0	SM1 SM1	SM2 SM2	REN REN	TB8 TB8	RB8 RB8	TI TI	RI RI	98h 98h	T89C51CC01 C505C/CA FE = Framing error not Supported by Infineon
SBUF									99h	T89C51CC01 same on C505C/CA
SADDR SADDR1									A9h	T89C51CC01 ONLY Slave addr
SADEN									B9h	T89C51CC01 ONLY Mask Byte
SRELH							.9 MSB	.8	BA h	C505C/CA ONLY
SRELL	.7	.6	.5	.4	.3	.2	.1	.0 LSB	AA h	C505C/CA ONLY
Capture and Compare C505C/CA Versus T89C51CC01 PCA SFR's										
CCON	CF	CR		CCF4	CCF3	CCF2	CCF1	CCF0	D8H	T89C51CC01 **only** C50C/CA
CMOD	CIDL	WDTE				CPS1	CPS0	ECF	D9H	T89C51CC01 **only** C505C/CA
CL									E9h	T89C51CC01 **only** C505C/CA
CH									F9h	T89C51CC01 **only** C505C/CA
CCEN	COCAH 3	COCAL3	COCAH 2	COCAL2	COCAH 1	COCAL1	COCAH 0	COCAL0	C1 h	C505C/CA ONLY
CCH1									C3 h	C505C/CA ONLY
CCH2									C5 h	C505C/CA ONLY
CCH3									C7 h	C505C/CA ONLY
CCL1									C2 h	C505C/CA ONLY
CCL2									C4 h	C505C/CA ONLY
CCL3									C6 h	C505C/CA ONLY
CRCH	.7 MSB	.6	.5	.4	.3	.2	.1	.0	CB h	C505C/CA ONLY
CRCL	.7	.6	.5	.4	.3	.2	.1	.0 LSB	CA h	C505C/CA ONLY
CCAPM0 CCAPM1 CCAPM2 CCAPM3 CCAPM4		ECOM0 ECOM1 ECOM2 ECOM3 ECOM4	CCAP0 CCAP1 CCAP2 CCAP3 CCAP4	CAP0 CAP1 CAP2 CAP3 CAP4	MAT0 MAT1 MAT2 MAT3 MAT4	TOG0 TOG1 TOG2 TOG3 TOG4	PWM0 PWM1 PWM2 PWM3 PWM4	ECCF0 ECCF1 ECCF2 ECCF3 ECCF4	DAh DBh DCh DDh DEh	T89C51CC01 T89C51CC01 T89C51CC01 T89C51CC01 T89C51CC01

Table 7. Comparison of SFR's Except CAN (Continued)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ADDR.	Comment for T89C51CC01
CCAP0L CCAP1L CCAP2L CCAP3L CCAP4L	CCAP0L 7 CCAP1L 7 CCAP2L 7 CCAP3L 7 CCAP4L 7	CCAP0L 6 CCAP1L 6 CCAP2L 6 CCAP3L 6 CCAP4L 6	CCAP0L 5 CCAP1L 5 CCAP2L 5 CCAP3L 5 CCAP4L 5	CCAP0L 4 CCAP1L 4 CCAP2L 4 CCAP3L 4 CCAP4L 4	CCAP0L 3 CCAP1L 3 CCAP2L 3 CCAP3L 3 CCAP4L 3	CCAP0L 2 CCAP1L 2 CCAP2L 2 CCAP3L 2 CCAP4L 2	CCAP0L 1 CCAP1L 1 CCAP2L 1 CCAP3L 1 CCAP4L 1	CCAP0L 0 CCAP1L 0 CCAP2L 0 CCAP3L 0 CCAP4L 0	EA h EB h EC h ED h EE h	T89C51CC01 T89C51CC01 T89C51CC01 T89C51CC01 T89C51CC01
CCAP0H CCAP1H CCAP2H CCAP3H CCAP4H	CCAP0 H7 CCAP1 H7 CCAP2 H7 CCAP3 H7 CCAP4 H7	CCAP0 H6 CCAP1 H6 CCAP2 H6 CCAP3 H6 CCAP4 H6	CCAP0 H5 CCAP1 H5 CCAP2 H5 CCAP3 H5 CCAP4 H5	CCAP0 H4 CCAP1 H4 CCAP2 H4 CCAP3 H4 CCAP4 H4	CCAP0 H3 CCAP1 H3 CCAP2 H3 CCAP3 H3 CCAP4 H3	CCAP0 H2 CCAP1 H2 CCAP2 H2 CCAP3 H2 CCAP4 H2	CCAP0 H1 CCAP1 H1 CCAP2 H1 CCAP3 H1 CCAP4 H1	CCAP0 H0 CCAP1 H0 CCAP2 H0 CCAP3 H0 CCAP4 H0	FA h FB h FC h FD h FE h	T89C51CC01 T89C51CC01 T89C51CC01 T89C51CC01 T89C51CC01
Interrupt SFRs										
IE0 IEN0	EA EA	AC WDT	ET2 ET2	ES ES	ET1 ET1	EX1 EX1	ET0 ET0	EX0 EX0	A8h A8h	T89C51CC01 **AC bit** C505C/CA **WDT bit**
IE1 IEN1 IEN1	EXEN2 EXEN2	SWDT SWDT	EX6 EX6	EX5 EX5	EX4 EX4	ETIM EX3 EX3	EADC ECAN -	ECAN EADC EADC	E8h B8h B8 h	T89C51CC01 **Note the position of** C505CA **EADC and ECAN bits** C505C
IPL0 IP0	OWDS	PPC WDTS	PT2 IPO.5	PS IPO.4	PT1 IPO.3	PX1 IPO.2	PT0 IPO.1	PX0 IPO.0	B8h A9 h	T89C51CC01 C505C/CA
IPH0		PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	B7h	T89C51CC01 C505C/CA NONE
IPL1 IP1			IP1.5	IP1.4	1P1.3	POVRL IP1.2	PADCL IP1.1	PCANL IP1.0	F8h B9h	T89C51CC01 C505C/CA
IPH1						POVRH	PADCH	PCANH	F7h	T89C51CC01 C505C/CA NONE
IRCON	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	SWI	IADC	C0h	C505C/CA ONLY SEE NOTE
ADC SFRs										
ADCON ADCON0	BD	PSIDLE CLK	ADEN -	ADEOC BSY	ADSST ADM	SCH2 MX2	SCH1 MX1	SCH0 MX0	F3h D8h	T89C51CC01 C505C/CA
ADCF ADCON1	CH7 ADCL1	CH6 ADCL0	CH5	CH4	CH3	CH2 MX2	CH1 MX1	CH0 MX0	F6h DCh	T89C51CC01 C505C/CA
ADCLK				PRS4	PRS3	PRS2	PRS1	PRS0	F2h	T89C51CC01 C505C/CA see ADCON1 bits ADCL0-1

Table 7. Comparison of SFR's Except CAN (Continued)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ADDR.	Comment for T89C51CC01
ADDH ADDATH	ADAT9 ADDATL .9	ADAT8 ADDATL .8	ADAT7 ADDATL .7	ADAT6 ADDATL .6	ADAT5 ADDATL .5	ADAT4 ADDATL .4	ADAT3 ADDATL .3	ADAT2 ADDATL .2	F5h D9h	T89C51CC01 MSB same C505CA
ADDL ADDATL	ADDATL .1	ADDATL .0					ADAT1	ADAT0	F4h DAh	T89C51CC01 C505CA
P1ANA	EAN7	EAN6	EAN5	EAN4	EAN3	EAN2	EAN1	EAN0	90 h	SABC505C/CA **only** :SYSCON RMAP bit set
The A/D convertor interrupt is controller by the EADC bit (Atmel SFR IE1 addr E8h and for Infineon IEN1 addr B8h and IADC bit IRCON SFR addr C0h)										
Other SFRs										
PCON	SMOD SMOD1	PDS SMOD0	IDLS -	SD POF	GF1 GF1	GF0 GF0	PDE PD	IDLE IDL	87h 87h	SABC505C/CA :SMOD (note 4) T89C51CC01 (note 4)
PCON1	EWPD			WS					88h	SABC505C/CA **only** :SYSCON RMAP bit set
AUXR		M(1)	M0		XRS1	XRS2	EXTRAM	AO	8Eh	**T89C51CC01 ONLY** see note 9 EXTRAM : if 0 (default) internal XRAM access using MOVX, if 1 External data memory access. **Same as the T89C51RD2** AO : ALE Output disable duringinternalcodefetch. AO=0(reset)ALEalwayson AO=1 ALE disable See Note 10 for External Program Mem
AUXR1			ENBOOT		GF3			DPS	A2h	T89C51CC01 ONLY Data Pointer selection see Note 1 above Clear to select DPTR0 (reset) Set to select DPTR1
CKCON	CANX2	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2	8Fh	T89C51CC01 ONLY Clear X2 for 12 clocks per cycle (reset value) Set X2 for 6 clocks per cycle. Each peripheral X2 settable NO X2 mode available C505C/CA
FCON	FPL3	FPL2	FPL1	FPL0	FPS	FMOD1	FMOD0	FBUSY	D1h	T89C51CC01 Flash Control No Flash on C505C/CA
EECON	EEPL3	EEPL2	EEPL1	EEPL0			EEE	EEBUSY	D2h	T89C51CC01 EEPRON Cntrl No EEPROM on C505C/CA
XPAGE	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0	91h	C505C/CA

Table 7. Comparison of SFR's Except CAN (Continued)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ADDR.	Comment for T89C51CC01
DPSEL	-	-	-	-	-	DPSEL.2	DPSEL.1	DPSEL.0	92h	C505C/CA
SYSCON		EALE EALE	RMAP RMAP	CMOD CMOD	- CSWO		XMAP1 XMAP1	XMAP0 XMAP0	B1h	C505C **No Atmel SYSCON** **C505CA/C515C** CAN Switch-off bit See Note 10 for External Program Mem
VR0									FCh	No Atmel VR0 but Manufacturer code and device ID and rev in Flash area read on hardware registers (See Flash Programming Section)
VR1									FDh	No Atmel VR1
VR2									FEh	No Atmel VR2

Note: See reset value for all registers on T89C51CC01

Functionality

Multiple Data Pointers Implementations for 8051 Compatible Faster External Access of Code

Atmel T89C51CC01 two 16 bit data pointers (DPTR0 and DPTR1) are mapped at the same SFR addresses 82h for DPL and 83h DPH. The register AUXR1 (SFR address A2h) contains one single bit DPS. With DPS=0 DPTR0 is selected and DPH + DPL present the value of DPTR0. With DPS=1 DPTR1 is selected and DPH + DPL present the value of DPTR1.

In the Infineon SABC505C/CA the eight 16 bit data pointers (DPTR0 through DPTR7) are mapped to the same SFR addresses 82h for DPL and 83h for DPH. The SFR register Data Pointer Select DPSEL at address 92h has the 3 bits DPSEL.2-0 to define the number of the active data pointer DPTR0-7.

Remark: Atmel implementation of the dual data pointer although not exactly the same as Philips is compatible with Philips.

Watchdog Timer (WDT)

To keep 8051 compatibility the Atmel T89C51CC01 has a divider-by-two circuit inserted between the XTAL1 signal and the main core clock input. This divider can be disabled in software. Therefore the WDT is clocked at the standard 12 Clocks per machine cycle if the CKCON.0 bit X2=0 and therefore in X1 or Standard 8051 mode (CKCON.1-7 have no effect). But if the CKCON.0 bit X2=1 and therefore the CPU is in the X2 mode at 6 clocks per machine cycle then the WDT can be set to either the X1 or X2 mode by the following; CKCON.6 bit WDX2=0 (WD =X2 mode); other wise a set bit is in standard 12 clocks per machine cycle. (note CKCON address = 8Fh)

Infineon does not support the X2 mode for the WDT unit.

The T89C51CC01 has a WDT with a 14 bit counter and a programmable 7 bit counter for a total of 21 bits. The Atmel watchdog time-out period in the T89C51CC01 is programmed by register WDTPRG (address A7h) bit S0 S1 S2, see value on T89C51CC01 datasheet. The time-out is programmable from $(2^{14}-1)*6$ clocks to $(2^{21}-1)*6$ clocks: from 16 ms to 2 seconds @12MHz or 9.82 mS to 1.25 µS @20MHz.

Atmel watchdog is enabled and reset by writing 1Eh then E1h in the WDTRST register (address A6h). Upon time-out, the watchdog generates a reset, the reset is available as an output on the reset pin. The reset pulse is 96 XTAL clock periods.

The WDT does not need to be serviced in the power down mode. It is prudent of the user to service the WDT just prior to entering the power down mode to prevent an overflow at power down. However, in the idle mode where the oscillator is still running the user should set up a timer to periodically exit the idle mode, service the WDT and then re-enter idle mode. Atmel does not support an on-chip oscillator watchdog (OWD).

The Infineon C505C/CA provides both a programmable 15 bit watchdog timer and an on-chip oscillator watchdog (OWD). The OWD monitors the on-chip oscillator and provides the clock for fast on reset.

The Infineon watchdog time-out period is programmed by WDTREL register (address 86h). WDTREL.7 bit WDTPSEL is the watch dog prescaler which if set is a divide by 16 and the 7 bit reload value are bits WDTREL.6-0. The time-out is programmable from: minimum WDTREL=00h from 32.768 ms @ 12 MHz or 24.576 ms @ 16MHz to a maximum when WDTREL = 7Fh of 256 µS @ 12 MHz or 192 µS @ 16 MHz.

The Infineon watchdog timer is controlled by two control flags (WDT and SWDT in the IEN0 and IEN1 registers) and one status flag (WDTS in the IP0 register). The OWD is controlled by the status flag bit OWDS in the IP0 register.

The Infineon watchdog is refreshed by a double instruction sequence of setting to the bits WDT (IEN0) and SWDT (IEN1) consequently*.*

The Infineon double instruction protection mechanism is replaced by a similar mechanism in the Atmel T89C51CC01 as the dual write into WDTRST as described above.

Timer Clock

To keep 8051 compatibility the Atmel T89C51CC01has a divider-by-two circuit inserted between the XTAL1 signal and the main core clock input. This divider can be disabled in software. Therefore timer 0,1,2 are clocked at the standard 12 Clocks per machine cycle if the CKCON.0 bit X2=0 and therefore in X1 or Standard 8051 mode (CKCON.1-7 have no effect). But if the CKCON.0 bit X2=1 and therefore the CPU is in the X2 mode at 6 clocks per machine cycle then each timer 0,1,and 2 can be set to either the X1 or X2 mode by the following; CKCON.1 bit T0X2=0 (timer0=X2 mode); CKCON.2 bit T1X2=0 (timer1=X2 mode); CKCON.3 bit T2X2=0 (timer2=X2 mode) other wise a set bit is in standard 12 clocks per machine cycle. (note CKCON address = 8Fh)

The hardware CPU X2 mode can be read and written via the In Application Programming (IAP) (SetX2Mode, ClearX2Mode, ReadX2Mode) while the application is running with out a reset. See the section on the CAN comparison therefore to change the FCAN from X1 to X2 mode.

Remark: Using Atmel T89C51CC01 to replace a SABC505C/CA, most likely the X2 mode will be selected in the T89C51CC01 to achieve 6 clock per cycles for the CPU. The timers will be selected to run in the X1 mode at 12 clocks per machine cycle. Otherwise their programming must be changed to recover the timing value they had with SABC505C/CA running at 12 clocks per machine cycle.

UART Control

To keep 8051 compatibility the Atmel T89C51CC01has a divider-by-two circuit inserted between the XTAL1 signal and the main core clock input. This divider can be disabled in software. Therefore the serial UART is clocked at the standard 12 Clocks per machine cycle if the CKCON.0 bit X2=0 and therefore in X1 or Standard 8051 mode (KCON.1-7 have no effect). But if the CKCON.0 bit X2=1 and therefore the CPU is in the X2 mode at 6 clocks per machine cycle then the serial UART can be set to either the X1 or X2 mode by the following; CKCON.4 bit S1X2=0 (UART =X2 mode); other wise a set bit is in standard 12 clocks per machine cycle. (note CKCON address = 8Fh)

Atmel T89C51CC01 PCON register (address 87h) contains the SMOD1 and SMOD0 control bit for UART: PCON.7 the SMOD1 bit selects double baud rate in mode 1, 2, 3 and the PCON.6 bit SMOD0 selects access to Framing Error FE bit in SCON (SMOD0=1) or SM0 bit in SCON(SMOD0=0). Infineon does not support the enhanced UART Framing Error or automatic address recognition features found in the Atmel T89C51CC01.

Atmel T89C51CC01 supports an enhanced feature of automatic serial address recognition using the SADDR (A9h) and SADEN (B9h) registers. The SADDR register provides an 8 bit individual address and the SADEN provides a mask byte to address one or more slave addresses.

Atmel also has a Power Off Flag Feature with POF bit included in PCON register. Atmel does not support the Infineon slow down mode,. The Infineon Power down start (PDS), Slow Down start (SD), or Idle start bit (IDLS) must be set as a last instruction before entering that mode.

Infineon SABC505C/CA PCON register (same address as Atmel 87h) contains SMOD selects double baud rate in mode 1, 2, 3 for UART. Infineon does not support the Power Off Flag.

Programmable Counter Array (PCA)

To keep 8051 compatibility the Atmel T89C51CC01has a divider-by-two circuit inserted between the XTAL1 signal and the main core clock input. This divider can be disabled in software. Therefore the PCA is clocked at the standard 12 Clocks per machine cycle if the CKCON.0 bit X2=0 and therefore in X1 or Standard 8051 mode (CKCON.1-7 have no effect). But if the CKCON.0 bit X2=1 and therefore the CPU is in the X2 mode at 6 clocks per machine cycle then the PCA can be set to either the X1 or X2 mode by the following; CKCON.5 bit PCAX2=0 (PCA =X2 mode); other wise a set bit is in standard 12 clocks per machine cycle. (note CKCON address = 8Fh)

The PCA is used to produce pulse width modulated (PWM) output in a different manner than the Capture and Compare (CAPCOM) unit on the Infineon C505C/CA. These units are programmed totally different so that any code programmed for either must be rewritten to support the other device.

Infineon does not support the X2 mode for the CAPCOM unit.

Interrupt

Atmel T89C51CC01 and the SABC505C/CA have a 4 level priority interrupt system. The C505C/CA implements 12 interrupt vectors.

T89C51CC01 includes an additional IPH Interrupt priority register (address B7h) IP together with IPH provide a 2 bit coding to define 4 priority levels for the following interrupts: UART, Timer2, ADC, CAN (software), Timer1, External Interrupt1, Timer0, External Interrupt0, PCA.

See Table 6: Comparison natural interrupt priority assuming all sources have the same priority defined in IP0 and IP1 (SABC505C/CA) or IP and IPH (T89C51CC01)

Note: with IPH reset value being 00h, T89C51CC01 defaults to 2 priority levels and is fully compatible with Philips 2 priority levels.

Table 8. Interrupt Priority

Name If/Atmel	Description Infineon/Atmel	Infineon Level	Atmel Level	Vector	Comment
IE0/INT0	External interrupt 0	1	1	03h	
TF0	Timer 0	2	2	0Bh	
IE1/INT1	External interrupt 1	3	3	13h	
TF1	Timer 1	4	4	1Bh	
RI/TI	TI or RI UART	6	6	23h	
TF2	Timer 2	7	7	2Bh	
	SERIAL CHANNEL INT.	5		23 h	
	PCA (T89C51CC01 only)		5	33h	No 33h on C505C/CA
	CAN (TX Rcv Buf ov; T89C51CC01 only)		8	3Bh	No 3Bh on C505C/CA
IADC	ADC Interrupt	P	9	43h	
	CAN Software Interrupt/ CAN Overflow	P	10	4Bh	Warning Not the same Interrupts
IEX3/INT3	External interrupt3	P	-	53h	C505C/CA only
IEX4/INT4	External interrupt4	P	-	5Bh	C505C/CA only

Table 8. Interrupt Priority

Name If/Atmel	Description Infineon/Atmel	Infineon Level	Atmel Level	Vector	Comment
IEX5/INT5	External interrupt5	P	-	63h	C505C/CA only
IEX6/INT6	External Interrupt 6	P	-	6Bh	C505C/CA only

Note: P= Programmable

Reset and Power-Off Flag

Both Infineon SABC505C/CA and Atmel T89C51CC01 Reset input require an external Capacitor between Reset input and Vcc positive supply is necessary (1µF typical for Atmel and 4.7 – 10 µF for Infineon) because of internal pull –down resistor to Vss.

The Infineon C505C/CA has an internal on-chip oscillator watchdog that subs as the input to the system clock for fast power on reset.

In the Atmel T89C51CC01, at power up, the RC composed with internal resistor and external capacitor (see above) will insure that a proper reset pulse is generated inside the circuit. A Schmitt trigger is built inside the chip in order to maintain a reset pulse long enough in case of slow Vcc ramp-up. The internal oscillator also includes a special mechanism to block the distribution of the clock inside the chip until the oscillator is stabilized with large enough oscillations.

There is no Power Fail Interrupt mechanism in the T89C51CC01 or the Infineon C505C/CA.

Atmel T89C51CC01 includes a Power-Off flag: the POF bit in PCON register is set at power-up. POF bit is cleared when an external or Watchdog reset generates a Reset.

The Infineon C505C/CA does not support the Power off flag in the PCON register (87h).

ADC Conversion

Atmel T89C51CC01 is a 3 volt ADC conversion and Infineon SABC505C/CA is a 5 volt ADC conversion. The SABC505C has an eight channel 8 bit AD and both the T89C51CC01 and the SABC505CA have a 10 bit AD. The Atmel AD has the feature to go into the idle mode during a conversion for the stability and then after the conversion is down go to the power mode. If the idle mode is chosen all interrupts are enabled but they can not be serviced till the end of the conversion. Be careful on choosing the stable conversion by using idle mode to service real time interrupts. The Atmel has different position of the bits of the 10 bit AD result that is optimized for the use of a C shift operation.

Int Variable = ADDH << 2 +ADDL and the values of all unused bits in ADDL are set to zero for this operation.

The sample times are different depending on the system clock, divider and prescaler with a maximum of the 700KHz. At 700KHz the Atmel has a 16 us conversion time channel. For the fastest rate the input clock and prescaler are selected so that the frequency is as close to 700 KHz but not greater than. If the ADC is not enabled then it defaults into standby mode for lower power consumption.

Program/User Code Flash Memory

The Atmel T89C51CC01 implements 32 Kbytes of on-chip program/user code Flash memory. The on-chip 32 K bytes FLASH is located between 0000 and 7FFF hex and an additional 32K bytes of external program memory can be located 8000 – FFFF hex. The T89C51CC01 can further be used in a single chip mode design where by the ALE line is not constantly active, either 1/6 in X1 mode or 1/3 in X2 mode of the OSC frequency, but is only active for a MOVC or MOVX command controlled by the AO (bit0) in the AUXR SFR.

The FLASH program code memory increases the functionality of either EPROM or ROM by providing in-circuit electrical erasure and programming. An internal charge pump provides the high voltage needed to erase FLASH cells and is generated on-chip using the standard V_{DD} voltage. Therefore the FLASH can be programmed using a single operating voltage source by the application software Program (IAP) or by hardware programming mode (parallel technique) using a specific third party programmer tool.

T89C51CC01 features two separate on-chip FLASH memories. The first is FLASH Memory Zero (**FM0**) which contains the 32K bytes of user program code/memory organized into 256 pages of 128 bytes. FM0 supports both serial ISP or parallel programming by third party tool programmers. The second FLASH memory (**FM1**) is a separate 2 K bytes of boot loader and Atmel provided Applications Programming Interfaces (API). These API supports all the READ/WRITE access operations on FALSH memory FM0. (see In System Programming Section of T89C51CC01 Data Sheet) FM1 only supports parallel programming by third party tool programmers. FM1 is mapped between F800 and FFFF hex when the ENBOOT bit is set in the AUXR1 SFR.

FM0 consists of four blocks:

1. Hardware Security Byte (8 bits); the 4 most significant bits are software Read/write able and the 4 least significant bits (Lock Bits 2,1,0) are read/write able only in the parallel programming mode. These lock bits provide security from external reading of the internal code. **The security level is set to level 4 from the factory so that external programming and parallel mode verification are disabled.**
2. Extra Row (XROW) 128 bytes
3. Column Latches 128 bytes; used as the entrance buffer for the 32K bytes user code array, XROW, and hardware security byte.
4. User FLASH Memory Array of 256 pages of 128 bytes (32 K bytes).

For the In Systems Programming (ISP) of the FLASH see section below. For the CAN or UART enabled Boot loader for the T89C51CC01 see the Atmel Applications note of the same title.

At the current time the only program code memory configuration that the Infineon SABC505C/CA offers is the 32 K Bytes of One-Time Programmable memory (OTP) for the C505CA and 16K bytes ROM for the C505C.

External Program Memory Access

For external Program memory access mode the not EA pin will be to ground (for any 8051, C505C/CA, T89C51CC01). For the Infineon C505C/CA the SYSCON SFR (address B1 h) the enable ALE bit 6, EALE will be set for external ALE. For the Atmel T89C51CC01 the AUXR SFR (address 8E h) bit 0 the ALE Output bit, AO = 0 for always on. The ALE line will then be enabled for external access.

CAN Comparison

CAN SFR Comparison

Table 9. CAN SFR Table Comparison

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ADDR.	Comment for T89C51CC01
General CAN CONTROL										
CANGCON CR	ABRQ TEST	OVRQ CCE	TTC 0	SYNCTTC 0	AUTBAUD EIE	TEST SIE	ENA IE	GRES INIT	ABh F700h	T89C51CC01 C505C/CA
CANGSTA SR	BOFF	OVFG EWRN	- -	TBSY RXOK	RBSY TXOK	ENFG LEC2	BOFF LEC1	ERRP LEC0	AAh F701H	T89C51CC01 C505C/CA
CANBT1 BTR0	- SJW1	BRP5 SJW0	BRP4 BRP5	BRP3 BRP4	BRP2 BRP3	BRP1 BRP2	BRP0 BRP1	- BRP0	B4h F704h	T89C51CC01 C505C/CA
CANBT2 BTR1	- 0	SJW1 TSEG22	SJW2 TSEG21	- TSEG20	PRS2 TSEG13	PRS1 TSEG12	PRS0 TSEG11	- TSEG10	B5h F705H	T89C51CC01 C505C/CA
CANBT3		PHS22	PHS21	PHS20	PHS12	PHS11	PHS10	SMP	B6h	T89C51CC01 C505C/CA BTR0/1
CANGIT IR	CANIT INTID7	- INTID6	OVRTIM INTID5	OVRBUF INTID4	SERG INTID3	CERG INTID2	FERG INTID1	AERG INTID0	9Bh F702h	T89C51CC01 C505C/CA
CANEN1		ENCH14	ENCH13	ENCH12	ENCH11	ENCH10	ENCH9	ENCH8	CEh	T89C51CC01 C505C/CA
CANEN2	ENCH7	ENCH6	ENCH5	ENCH4	ENCH3	ENCH2	ENCH1	ENCH0	CFh	T89C51CC01 C505C/CA
CANSIT1	-	SIT14	SIT13	SIT12	SIT11	SIT10	SIT9	SIT8	Bah	T89C51CC01
CANSIT2	SIT7	SIT6	SIT5	SIT4	SIT3	SIT2	SIT1	SIT0	BBh	T89C51CC01
CANTCON	TPRESC 7	TPRESC 6	TPRESC 5	TPRESC 4	TPRESC 3	TPRESC 2	TPRESC 1	TPRESC 0	A1h	T89C51CC01 TIMER CNTL **C505C/CA NONE**
CANTIMH	CANTIM15	CANTIM14	CANTIM13	CANTIM12	CANTIM11	CANTIM10	CANTIM9	CANTIM8	ADh	T89C51CC01 CAN Time High C505CA NONE
CANTIML	CANTIM7	CANTIM6	CANTIM5	CANTIM4	CANTIM3	CANTIM2	CANTIM1	CANTIM0	ACh	T89C51CC01 CAN Time Low C505CA NONE
CANSTMH	TIMSTMP 15	TIMSTMP 14	TIMSTMP 13	TIMSTMP 12	TIMSTMP 11	TIMSTMP 10	TIMSTMP 9	TIMSTMP 8	AF h	T89C51CC01 CAN Time Stmp C505CA NONE
CANSTMPL	TIMSTMP 7	TIMSTMP 6	TIMSTMP 5	TIMSTMP 4	TIMSTMP 3	TIMSTMP 2	TIMSTMP 1	TIMSTMP 0	AE h	T89C51CC01 CAN Time Stmp C505CA NONE
CANTTCH	TIMTTC 15	TIMTTC 14	TIMTTC 13	TIMTTC 12	TIMTTC 11	TIMTTC 10	TIMTTC 9	TIMTTC 8	A5 h	T89C51CC01 CAN TTC C505CA NONE

Table 9. CAN SFR Table Comparison (Continued)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ADDR.	Comment for T89C51CC01
CANTTCL	TIMTTC 7	TIMTTC 6	TIMTTC 5	TIMTTC 4	TIMTTC 3	TIMTTC 2	TIMTTC 1	TIMTTC 0	A4 h	T89C51CC01 CAN TTC C505CA NONE
CANGIE			ENRX	ENTX	ENERCH	ENBUF	ENERG		C0 h	T89C51CC01 **ONLY**
CANIE1	ENCH14	ENCH13	ENCH12	ENCH11	ENCH10	ENCH9	ENCH8	ENCH8	C1 h	T89C51CC01 **ONLY**
CANIE2	ENCH7	ENCH6	ENCH5	ENCH4	ENCH3	ENCH2	ENCH1	ENCH0	C2 h	T89C51CC01 **ONLY**
CANTEC	TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0	9C h	T89C51CC01 **ONLY** Read only
CANREC	REC7	REC6	REC5	REC4	REC3	REC2	REC1	REC0	9D h	T89C51CC01 **ONLY** Read only
CANPAGE	CHNB3	CHNB2	CHNB1	CHNB0	AINCb	INDX2	INDX1	INDX0	B1 h	T89C51CC01 **ONLY**
CANSTCH	DLCW	TXOK	RXOX	BERR	SERR	CERR	FERR	AERR	B2 h	T89C51CC01 **ONLY**
CANCONH	CONCH1	CONCH0	RPLV	IDE	DLC3	DLC2	DLC1	DLC0	B3 h	T89C51CC01 **ONLY**
CANMSG	MSG7	MSG6	MSG5	MSG4	MSG3	MSG2	MSG1	MSG0	A3 h	T89C51CC01 **ONLY**
CANIDM1	IDMSK10	IDMSK9	IDMSK8	IDMSK7	IDMSK6	IDMSK5	IDMSK4	IDMSK3	C4 h	T89C51CC01 **ONLY 11 BIT**
CANIDM2	IDMSK2	IDMSK1	IDMSK0						C5 h	T89C51CC01 **ONLY 11 BIT**
CANIDM3									C6 h	T89C51CC01 **ONLY 11 BIT**
CANIDM4						RTRMSK		IDEMSK	C7 h	T89C51CC01 **ONLY 11 BIT**
CAN Arbitration Registers CAN 2.0 Part A (Standard 11 bit Identifiers)										
CANIDT1 UAR0	IDT10 ID28	IDT9 1D27	IDT8 ID26	IDT7 1D25	IDT6 ID24	IDT5 ID23	IDT4 ID22	IDT3 ID21	BC h F7n2 h	T89C51CC01 C505C/CA N =1-F h
CANIDT2 UAR1	IDT2 ID20	IDT1 ID19	IDT0 ID18	X X	X X	X X	X X	X X	BD h F7n3 H	T89C51CC01 C505C/CA N =1-F h
Note: for Infineon ID 28-18 is the standard identifier bytes 10-0 for 11 bit identifier (ID). All 15 Message objects are available in XRAM (n=1-F hex).										
Note: access to the Atmel CAN Channel (message object) is via the CAN Channel Page register CANPAGE SFR (B1 h).										
CAN Arbitration Registers CAN 2.0 Part B (Extended 29 bit Identifiers)										

Table 9. CAN SFR Table Comparison (Continued)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ADDR.	Comment for T89C51CC01
CANIDT1 UAR0	IDT28 ID28	IDT27 1D27	IDT26 ID26	IDT25 1D25	IDT24 ID24	IDT23 ID23	IDT22 ID22	IDT21 ID21	BC h F7n2 h	T89C51CC01 C505C/CA N =1-F h
CANIDT2 UAR1	IDT20 ID20	IDT19 ID19	IDT18 ID18	IDT17 ID17	IDT16 ID16	IDT15 ID15	IDT14 ID14	IDT13 ID13	BD h F7n3 H	T89C51CC01 C505C/CA N =1-F h
CANIDT3 LAR0	IDT12 1D12	IDT11 ID11	IDT10 ID10	IDT9 ID9	IDT8 ID8	IDT7 ID7	IDT6 ID6	IDT5 ID5	BE h F7n4 h	T89C51CC01 C505C/CA N =1-F h
CANIDT4 LAR1	IDT4 1D4	IDT3 ID3	IDT2 ID2	IDT1 ID1	IDT0 ID0	RTRTAG -	RB1TAG -	RB0TAG -	BF h F7n5 h	T89C51CC01 C505C/CA N =1-F h
Note: for Infineon All 15 Message objects are available in XRAM (n=1-F hex).										
Note: access to the Atmel CAN Channel (message object) is via the CAN Channel Page register CANPAGE SFR (B1 h).										

Atmel and Infineon CAN Implementation Comparison

General

In the Atmel T89C51CC01 a system of pagination allows the management of the 177 registers and 120 (15 x 8) bytes of the CAN data mailbox via 21 direct addressable Special Function Registers (SFR) and 13 indirect general channel window SFR's (CAN message buffers or objects) that are accessible via the **CANPAGE** register (see page 82 figure 65 CAN Controller memory organization ref 1 data sheet). The use of direct addressable SFR's speed up the transfer of data via the assembly MOV command. All actions on the channel window SFR's are reflected in the corresponding channel (message objects) registers. **(Atmel refers to the 15 Infineon CAN message objects registers as CAN channel registers!!! Do not confuse this terminology with the one single CAN transmit and receive channel on the CAN peripheral)** The T89C51CC01 channel window SFR is handled through the PAGE Channel CANPAGE register (B1 h) which is used to select one of the 15 CAN Channels (message objects). Then the Channel Control (CANCONCH) and Channel Status (CANSTCH) registers are available for this selected channel number in the corresponding SFR's. A single CANMSG register is used for the CAN message. The mailbox pointer is managed by the PAGE Channel (CANPAGE) and has auto increment capability with a range of 8. Note that since the CAN message mailbox is pure RAM, dedicated to one channel, without overlap. In most cases it is not necessary to transfer the received message into the standard 8051 memory. The message to be transmitted can be built directly in the mailbox and most calculations or test can be executed in the mailbox area. During T89C51CC01 operation the CAN Enable Channel registers 1 and 2 (CANEN1/2) will give a fast overview of channel availability. CAN messages can be handled by both interrupt or polling methods.

In the Infineon SABC505C/CA a system of 256 bytes of SFR's located in the XRAM portion of the on-chip RAM memory. These SFR's are accessible by the MOVX assembly command because of the XRAM. This will take two machine cycles versus the one cycle for the MOV for direct addressable SFR's. The Infineon C505C/CA is not currently available with the X2 clock mode, or 6 clock cycles per machine cycle, so that increased speed is available only by increasing the Infineon micro-controller oscillator frequency. The 256 bytes of SFR's in XRAM locations F700 through F7FE hex are organized into 15 General CAN registers in the first 16 bytes and then 15 message (channel) objects of

16 bytes containing the message objects (channel) registers. The general CAN control registers are used to set up the CAN control, Bit timing, provides status or received or transmitted messages, interrupts, initialization, and both the global and last message masks for the message objects. Then each individual message object (15 available) have 8 configuration bytes and 8 data bytes available in XRAM at offsets of F7n0 to F7nE hex. Therefore, each message objects registers are readily available via the n (off-set) from 1 to 15 (1 to F hex).

CAN Arbitration Registers

The CAN arbitration registers for both the standard 11 bit identifiers (CAN 2.0 Part A) and the extended 29 bit identifiers (CAN Part 2.0 B) are both supported by Infineon C505C/CA and the Atmel T89C51CC01. The arbitration registers are compared for both 11 and 29 bit identifiers above. In the Infineon CAN architecture all 15 message object (CAN channels) identifiers are available in XRAM with the offset of n=1-F hex for accessing the registers UAR0, UAR1, LAR0, and LAR1. The Atmel architecture permits the access of channel and associated arbitration identifiers through the CANPAGE SFR located at B1 hex.

CAN Bit Timing

CAN bit timing for both the Infineon and Atmel are divided into time quantum (tq) with the minimum resolution of one system clock. They both begin with a Synchronization segment equal to one tq. (nomenclature in Infineon Synchronization Segment ($t_{Syns-Seg}$) and Atmel Time Synchronization (T_{syns}) Both of these are non-programmable and represent the same quantity.

The Infineon Time Quanta ($\mathbf{t_Q}$) is calculated by the following equation:

tQ = (BRP +1) * 2 (1 – CMOD) * CLP
t Syns-Seg = 1 * tQ
t Tseg1 = (TSEG1 +1) * tQ (= minimum of 4 * tQ)
t Tseg2 = (TSEG2 +1) * tQ (= minimum of 3 * tQ)
bit time = t Sync-Seg + t Tseg1 + t Tseg2 (exact sequence of times)

Where TSEG1 (BTR1:0-3), TSEG2 (BTR1:4-6), and BRP (BTR0:0-5) are the programmed values form the respective fields of the bit timing registers BTR0 and BTR1. Note both BTR0 and BTR1 can only be configured if Configuration Change Enable bit (CCE) (CR:6)is set in the CAN Control Register (CR). CMOD (SYSCON:3) is bit 3 in the SYSCON register location B1 hex.

Note that the bit rate time is determined by the C505C/CA clock period (CLP as defined in the AC Characteristics on SABC505C/CA Data Sheet), the six bit Baud Rate Pre-scalar (BRP), and the number of time quanta per bit.

The sample point is at the end of t_{Tseg1} and the transmit point is at the end of $t_{Tseg2.}$ (see bit time calculation above for exact sequence).

Now to compare this bit timing of the Atmel where the Time of Synchronization is equal to the time of the System Clock ($T_{SYNC} = T_{SCL}$). The $T_{SYNS} = T_{SCL} = (BRP +1) / F_{CAN}$; where BRP is a six bit baud rate pre-scalar (CANBT1:6-1) location B4 hex, and F_{CAN} is the frequency of the CAN controller as determined by the FCAN clock (CANX2 bit (CKCON:7) AND X2 bit (CKCON:0)) . Note that the CAN controller bit timing registers can only be accessed if the CAN controller is disable with the ENA bit of the CANGCON register set to zero.

It may also be noted that the FCAN can be changed from the X1 to X2 mode in the application if an auto baud sensing and calculation program is going to be written by the user using this X1 and X2 feature of FCAN. The auto baud and listening modes of T89C51CC01 are used for hot plug attachment of the Bus nodes to a running system with an unknown bit rate.

TSYNS = TSCL (fixed)=(BRP +1) / FCAN = tQ

TPRS = (1 to 8)* TSCL =(PRS[2:0] +1) * TSCL

TPHS1 = (1 to 8)* TSCL =(PHS1[2:0] +1) * TSCL

TPHS2 = (1 to 8)* TSCL =(PHS2[2:0] +1) * TSCL

TSJW = (1 to 4)* TSCL =(SJW[1:0] +1) * TSCL

T_{BIT} = (8 to 25)* T_{SCL} = T_{SYNS} + T_{PRS} +T_{PHS1} + T_{PHS2} ; Where the sample point is at the end of T_{PHS1} and the transmit point is at the end of T_{PHS2} .

Therefore, the Infineon Tseg1 is equal to the Atmel T_{PRS} +T_{PHS1} and the Infineon Tseg2 is equal to the Atmel $T_{PHS2.}$ The analysis of the bit timing would leave you to consider the ability to change the Atmel F_{CAN} from X1 to X2 during an application and the ability to configure the Atmel T_{PRS} +T_{PHS1} segment.

T89C51CC01 Enhancements Features

The following section pertains to the enhancements of the Atmel T89C51CC01 CAN module, FLASH program memory, and data EEPROM memory for applications where time stamps, time triggered protocol, in system programmable (ISP) Flash program memory, EEPROM data memory, and boot-loaders via both the UART and CAN are necessary. These are system level concerns of many embedded CAN designers and are supported by the T89C51CC01 derivative but not supported by the Infineon SABC505C/CA and other CAN micro-controllers.

Data Strings Longer than the 8 Byte CAN Maximum per CAN Message Frame

Special Features for flexibility to ease the transfer of data strings longer than the 8 byte maximum limitation of one CAN frame.

In receive buffer mode: 1 to 15 message objects can participate in a non-consecutive sequence to build up a 120 byte wide data receiver buffer. In this case all concerned ID Tag registers are programmed on the same CAN message identifier. The lowest channel will be served first. This feature enables a large data block to be received with the same CAN message identifier. In this mode the CAN interrupt will be received at 100 percent full and then each additional CAN message will be receive in the normal receiver mode with a CAN interrupt after each received CAN message. This ensures that no CAN message will be lost after the 100 percent full CAN interrupt.

CAN Auto Reply Mode

The CAN auto reply mode feature enables a transmission without software intervention after the reception of the remote frame that has been pre programmed for reception in auto-reply mode.

CAN Time Stamp and Time Trigger Communication Protocol

A 16 bit programmable timer CANTIMER is used to stamp each received and sent CAN message in the CANSTMP register. The timer is started as soon as the CAN controller is enabled by the ENA bit in the CANGCON register (AB h).

The Time Trigger Communication (TTC) protocol is supported by the T89C51CC01.

CAN Auto Baud and Listening Modes

The auto baud and listening modes of T89C51CC01 are used for hot plug attachment of the Bus nodes to a running system with an unknown bit rate. In the Autobaud and Listening mode the CAN controller is only listening to the line without acknowledging the received messages. It also can not send messages. The error flags are updated and the bit timing can be adjusted until no error occurs. The error counters are frozen in this mode.

To activate this mode the AUTOBAUD bit (CANGCON.3) is set in the CAN General Control Register (CANGCON). To go back to the standard mode the AUTOBAUD bit is cleared by software.

Special Section for the Atmel In System Programming of 32K User Code Flash (FM0) and EEPROM Data programming

The code memory architecture and organization on the Atmel T89C51CC01 is describe in note 9 in the Comparison of SFR's section above. The CPU interfaces the 32K bytes of FLASH program/user code memory through the FCON and AUXR1 SFR's. to:

1. Map Memory spaces in addressable space
2. Launch the programming of memory space
3. Get busy/not busy status of memory
4. Select the FLASH memory FM0 or FM1

API Calls listed on of the T89C51CC01 data sheet are available for use by an application program to permit the selective erasing and programming of FLASH pages. All calls are made by functions listed on. The API can be called during the user application without interrupt. The interrupts are disabled by some of the API's for complex operations.

The XROW contains bytes for boot loader management; Boot Vector Address (BVA) location 01 h, Software Security Byte (SSB) location 05 h, Extra Byte (EB) location 06 h, Copy of the Manufacturer Code value 58 h for Atmel location 30 h, Copy of Device ID#1 Family Code value D7 for CANARY location 31 h, Copy of Device Code ID#2 Memory Size and type value F7 for Flash 32 k bytes location 60 h, and copy of Device ID #3 for the Name and Revision value FF at location 61 hex. The first 64 bytes of XROW can be used by the user or ZAPI functions.

EEPROM Data Reading and Programming

The 2 K bytes of on-chip EEPROM memory block is located at address 0000 to 07FF hex of the XRAM program memory and is selected by setting the control bits in the EECON SFR. The EEPROM memory is read using the MOVX instruction. The full 4 step procedure is as follows;

1. Set the bit EEPROM Enable (EEE) of the ECON SFR
2. Set Bit MO of the AUXR SFR to strech the MOVX to accommodate the slow access time of the column latch
3. Load the DPTR with the address to read
4. Execute MOVX A,@DPTR
5. The physical write to the EEPROM is accomplished in two steps;
6. Write data in the column latches
7. Transfer all data latches into EEPROM Memory row/ programming

The number of data written on the page can vary from 1 to 128 bytes (page size). When programming only the data written in the column latch is programmed and a ninth bit is used to obtain this feature. This provides the capability to program the whole memory by bytes, by page, or by a number of bytes in a page. Therefore each ninth bit is set when the corresponding byte in a row is written and the ninth bit is reset after writing a

complete EEPROM row. A detailed procedure to write data in the column latches and the programming is found in the T89C51CC01 data sheet.

References

Atmel References

- T89C51CC01 Data Sheet Rev.A

Infineon References

- SABC505C/CA Data Sheet Rev 9/22/1999
- SABC505/505C Users Manual Dated 8/1997
- SABC505A/505CA Addendum Users Manual Dated 9/1997

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