H.264 Encoder IP User Guide

Introduction (Ask a Question)

H.264 is a popular video compression standard to compress a digital video. It is also known as MPEG-4 Part10 or Advanced Video Coding (MPEG-4 AVC). H.264 uses the block-wise approach for compressing a video where the block size is defined as 16 x 16 and such block is called a macro block. The compression standard supports various profiles that define the compression ratio and complexity of implementation. The video frames to be compressed are treated as I-Frame, P-Frame, and B-Frame. An I-Frame is an intra-coded frame where compression is done by using the information contained within the frame. No other frames are required to decode the I-Frame. A P-Frame is compressed by using the changes with respect to an earlier frame that can be an I-Frame or a P-Frame. The compression of B-Frame is done by using the motion changes with respect to both an earlier frame and an upcoming frame.

The I and P frame compression process has four stages:

- Intra/Inter prediction
- Integer transformation
- Quantization
- Entropy encoding

H.264 supports two types of encoding:

- Context Adaptive Variable Length Coding (CAVLC)
- Context Adaptive Binary Arithmetic Coding (CABAC)

The current version of H.264 Encoder implements baseline profile and uses CAVLC for entropy encoding. Also, the IP supports encoding of I and P frames upto 4K resolution.

Summary

The following table lists a summary of the H.264 Encoder IP characteristics.

Table 1. H.264 Encoder IP Characteristics

Core Version	This document applies to H.264 Encoder IP v2.0.
Supported Device Families	• PolarFire® SoC • PolarFire
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases.
Licensing	H.264 Encoder IP is provided only in encrypted form under license. **Encrypted RTL:** Encrypted RTL source code is license locked, must be purchased separately. You can perform simulation, synthesis, layout, and program the Field Programmable Gate Array (FPGA) silicon using the Libero design suite. Evaluation license is provided for free to check the H.264 Encoder features. The evaluation license expires after an hour's use on the hardware.

Features

H.264 Encoder IP has the following features:

- Supports compression up to Resolution of 4K (3840 × 2160) 60 fps
- Implements compression on YCbCr 420 video format
- Expects the input in YCbCr 422 video format
- Supports 8 bits for each component (Y, Cb, and Cr)
- Supports ITU-T H.264 Annex B Compliant NAL byte stream output
- Standalone Operation, CPU, or Processor Assistance not required
- User Configurable Quality Factor QP during run time
- Supports dynamic configuration for number of P frames per I frame
- Supports user configurable threshold value for skip block
- Computation at the rate of 1 pixel per clock for each slice
- Minimal Latency (252 µs for full HD or 17 horizontal lines)
- Uses video arbiter interface for accessing DDR frame buffers
- Supports up to 4 slices

Unsupported Features

The H.264 Encoder has the following unsupported features in this version:

- B frames are not supported
- Does not support 8 x 8 integer transform
- Horizontal, Vertical, Diagonal, Vertical-Left, Horizontal-Down, Vertical-Right, and Horizontal-Up predictions not supported

Installation Instructions

The IP core must be installed to the IP Catalog of the Libero® SoC software automatically through the IP Catalog update function in Libero SoC software, or it is manually downloaded from the catalog. Once the IP core is installed in Libero SoC software IP Catalog, it is configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Resource Utilization (Ask a Question)

The following tables list the resource utilization of a sample H.264 Encoder IP design made for PolarFire® FPGA (MPF300TS-1FCG1152I package) and generates compressed data by using 4:2:2 sampling of input data.

Table 2. Resource Utilization of the H.264 Encoder IP when 4k_support = 0

Element	P_Frame = 0 (without 16x16 DC Prediction)	P_Frame = 0 (with 16x16 DC Prediction)	P_Frm = 1
4LUTs	16888	20916	72785
DFFs	17033	18974	65346
LSRAM	75	88	207
µSRAM	21	21	31
Math Blocks	19	23	19
Interface 4-input LUTs	3636	4248	8508
Interface DFFs	3636	4248	8508

Table 3. Resource Utilization when I Only Frames without 16x16 DC intra prediction (P_Frm = 0, 4k_support = 1)

Element	1-slice	2-slices	3-slices	4-slices
4LUTs	18440	36541	55306	72646
DFFs	18230	36281	54327	72338

.....continued				
Element	**1-slice**	**2-slices**	**3-slices**	**4-slices**
LSRAM	88	176	264	352
µSRAM	21	42	63	84
Math Blocks	19	39	59	77
Interface 4-input LUTs	4104	8244	12384	16452
Interface DFFs	4104	8244	12384	16452

Table 4. Resource Utilization when I and P Frames (P_Frm = 1, 4k_support = 1)

Element	1-slice	2-slices	3-slices	4-slices
4LUTs	29720	59441	88410	119000
DFFs	35560	71184	106835	142304
LSRAM	146	292	438	584
µSRAM	28	56	84	112
Math Blocks	19	39	59	77
Interface 4-input LUTs	6276	12588	18900	25140
Interface DFFs	6276	12588	18900	25140

Table of Contents

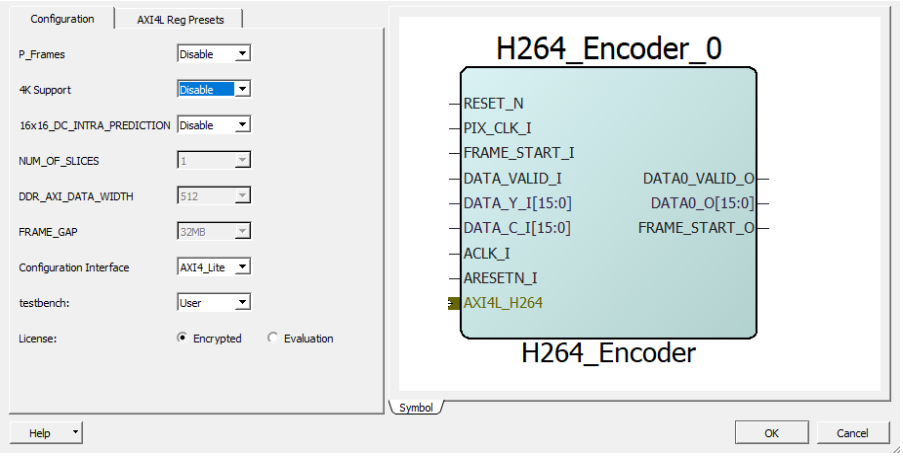
1. H.264 Encoder IP Configurator (Ask a Question)

This section provides an overview of the H.264 Encoder configurator interface and its various components.

The H.264 Encoder configurator provides a graphical interface to set up the H.264 Encoder core for specific requirements. This configurator allows the user to select parameters such as P_Frames, 4K Support, 16x16_DC_INTRA_PREDICTION, NUM_OF_SLICES, DDR_AXI_DATA_WIDTH, FRAME_GAP, Configuration Interface, Testbench, and License. The interface of the H.264 Encoder Configurator consists of various dropdown menus and options. The key configurations are described in Table 3-1.

The following figure provides a detailed view of the H.264 Encoder IP configurator interface.

Figure 1-1. H.264 Encoder IP Configurator



The interface also includes **OK** and **Cancel** buttons for confirming or discarding the configurations made.

2. Hardware Implementation (Ask a Question)

The H.264 Encoder IP supports the configurations as listed:

- I only frames supporting up to 1080P resolution
- I and P frames supporting up to 1080P resolution
- I only frames supporting up to 4K resolution with slices
- I and P frames supporting up to 4K resolution with slices

The following figures show the H.264 Encoder IP block diagram with respective configured frame and resolution.

Figure 2-1. H.264 Encoder Block Diagram (P_Frame = 0, 4K = 0)

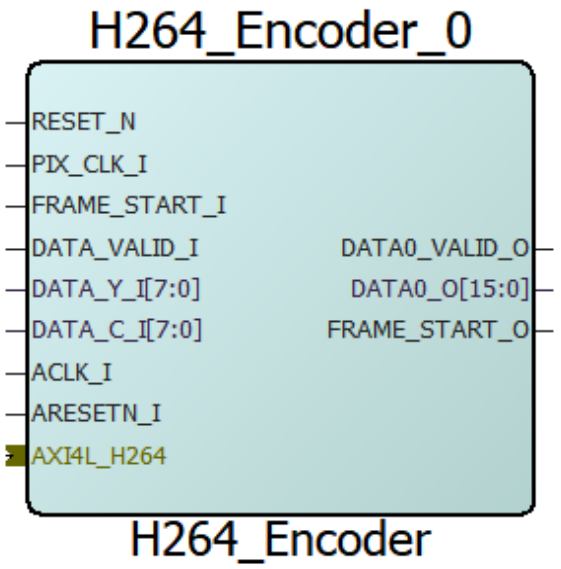


Figure 2-2. H.264 Encoder Block Diagram (P_Frame = 1, 4K = 0)

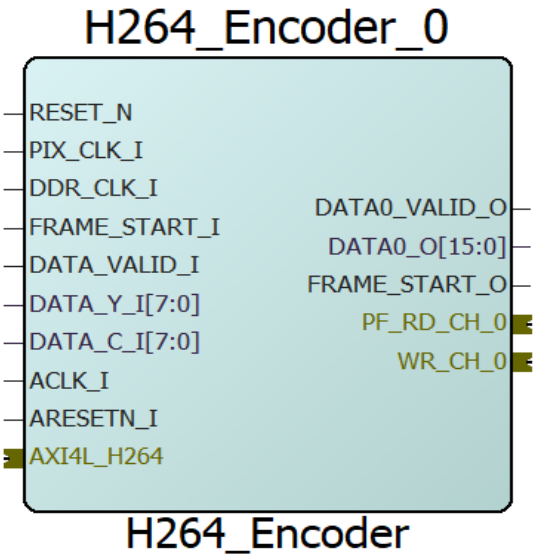


Figure 2-3. H.264 Encoder Block Diagram (P_Frame = 0, 4K = 1)

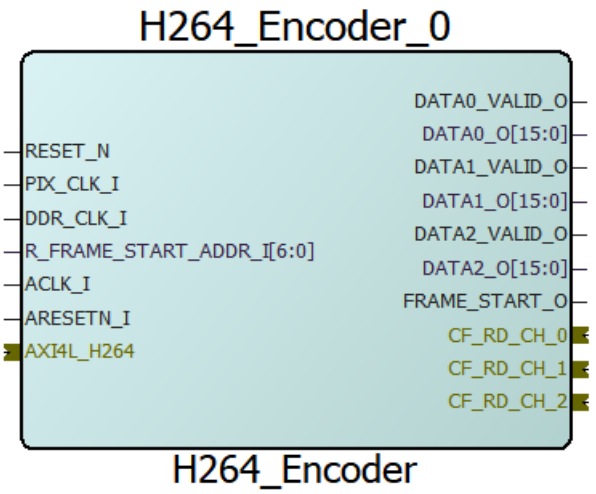
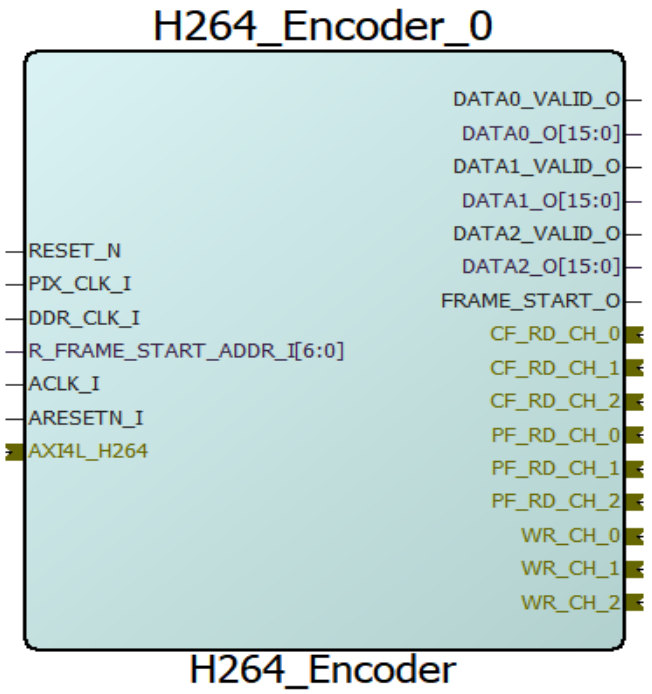


Figure 2-4. H.264 Encoder Block Diagram (P_Frame = 1, 4K = 1)

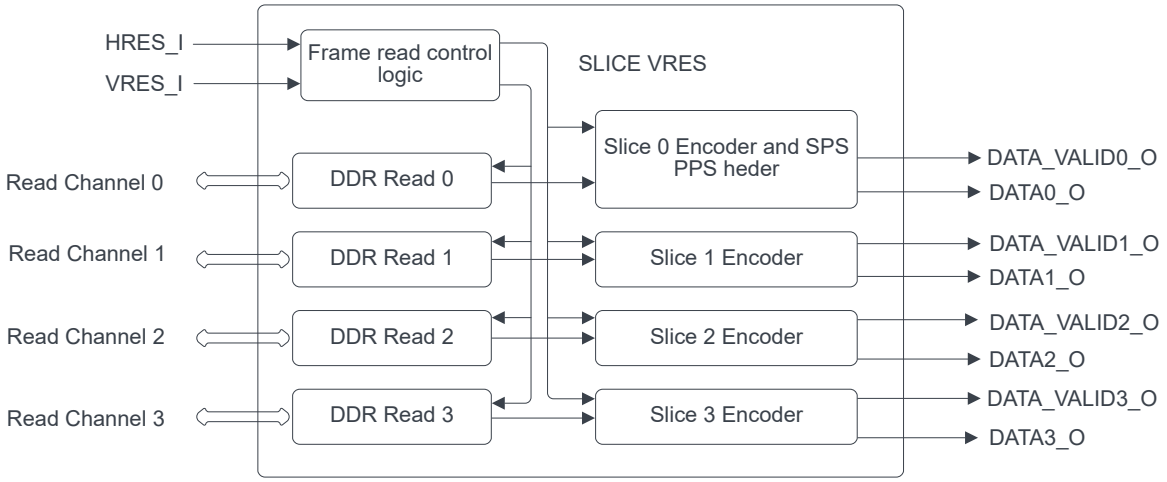


When 4K is disabled, H.264 Encoder IP uses one slice encoder as shown in Figure 2-6. Data input to the H.264 Encoder must be in the form of a raster scan image in the YCbCr 422 format. H.264 Encoder uses 422 formats as input and implements compression in 420 formats.

When 4K is enabled, H.264 Emcoder IP divides each frame into 1 to 4 slices and encodes using the slice encoder. The DDR read logic expects the frame data in DDR memory as YCbCr 422 format. The line gap between every horizontal line of frame in DDR memory must be specified through DDR_LINE_GAP_I input. The Slice0 output also contains the SPS and PPS header. All slices bit stream is provided separately. All slices bit stream combined together becomes the final H.264 bit stream.

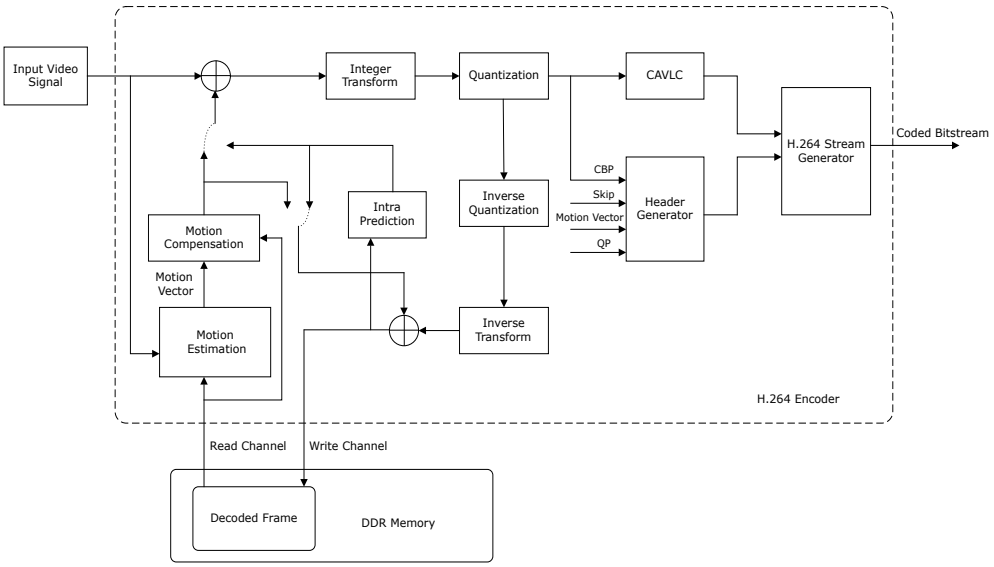
The following figure shows the H.264 Encoder IP block diagram with Slice Encoder and DDR Read channels.

Figure 2-5. Block Diagram



The following figure shows the slice encoder block diagram.

Figure 2-6. Slice Encoder Block Diagram



2.1 Design Description Slice Encoder (Ask a Question)

This section describes the different internal modules of the slice encoder.

2.1.1 Intra Prediction (Ask a Question)

H.264 uses various intra-prediction modes to reduce the information in a 4 x 4 block. The intra-prediction block in the IP uses only DC prediction on 4 x 4 matrix size. The DC component is computed from the adjacent top and left 4 x 4 blocks. Using 4 x 4 prediction at a QP value of more than 35 results in poor quality of video; for better quality, 16 x 16 prediction can be enabled. When P frame is enabled, the QP value for I frames is limited to 35 to improve video quality.

2.1.2 Integer Transform (Ask a Question)

H.264 uses integer discrete cosine transform where the coefficients are distributed across the integer transform matrix and the quantization matrix such that there are no multiplications or divisions in the integer transform. The integer transform stage implements the transformation using shift and add operations.

2.1.3 Quantization (Ask a Question)

The quantization multiplies each output of integer transform with a predetermined quantization value defined by the QP user input value. The range of QP value is from 0 to 51. Any value more than 51 is clamped to 51. A lower QP value denotes lower compression and higher quality and vice versa.

2.1.4 Motion Estimation and Compensation (Ask a Question)

When 4K is disabled, the Motion Estimation searches 8 x 8 block of the current frame in the 16 x 16 block of the previous frame and generates motion vectors.

When 4K is enabled, the Motion Estimation compares 8 x 8 block of the current frame with the 8 x 8 block of the previous frame and generates skip blocks or compensation.

2.1.5 CAVLC (Ask a Question)

H.264 uses two types of entropy encoding:

- Context Adaptive Variable Length Coding (CAVLC)
- Context Adaptive Binary Arithmetic Coding (CABAC)

H.264 Encoder IP uses CAVLC for encoding the quantized output.

2.1.6 Header Generator (Ask a Question)

The header generator block generates the block headers, slice headers, Sequence Parameter Set (SPS), Picture Parameter Set (PPS), and Network Abstraction Layer (NAL) unit depending on the instance of the video frame. Skip block decision logic calculates the Sum of Absolute Difference (SAD) of the current frame 16 x 16 macro block and the previous frame 16 x 16 macro block from the motion vector predicted location. The skip block is decided using the SAD value and the SKIP_THRESHOLD input.

2.1.7 H.264 Stream Generator (Ask a Question)

The H.264 stream generator block combines the CAVLC output along with the headers to create the encoded output as per the H.264 standard format.

2.1.8 DDR Write Channel and Read Channel (Ask a Question)

H.264 Encoder requires the decoded frame to be stored in DDR memory, which is used in the inter prediction. The IP uses DDR write and read channels to connect with the Video Arbiter IP, which interacts with the DDR memory through the DDR controller IP.

3. H.264 Encoder Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the H.264 Encoder GUI configurator and I/O signals.

3.1 Configuration Parameters (Ask a Question)

The following table lists the description of the generic configuration parameters used in the hardware implementation of the H.264 Encoder, which can vary based on the application requirements.

Table 3-1. H.264 Encoder Configuration Parameters

Name	Description
P_Frames	Option to enable P frames support
4K Support	Option to enable 4K resolution support
16x16_DC_INTRA_PREDICTION	Option to enable the 16 x 16 intra dc prediction along with 4 x 4 intra dc prediction. Supports only when P frames is disabled.
NUM_OF_SLICES	Configuration is supported only when 4K is enabled. • Select 1 slice to support 4K at 15 fps when PIX_CLK_I is 135 MHz • Select 2 slices to support 4K at 30 fps when PIX_CLK_I is 135 MHZ • Select 3 slices to support 4K at 60 fps when PIX_CLK_I is 175 MHz • Select 4 slices to support 4K at 60 fps when PIX_CLK_I is 135 MHz
DDR_AXI_DATA_WIDTH	Select the DATA width of read channel, which must be connected to video arbiter IP.
FRAME_GAP	Select the frame buffer size. For 4K select 32 MB.
Configuration Interface	Supports the following interfaces for configuration: • Native: Configuration Interface ports are provided when Native is selected • AXI4_Lite: AXI4 Lite slave interface is provided and AXI4L Reg Presets tab are used to set the reset values of the registers
Testbench	Allows the selection of a testbench environment. Supports the following testbench options: • User • None
License	Specifies the type of license. Provides the following two license options: • Encrypted • Evaluation

3.2 Inputs and Outputs (Ask a Question)

The following table lists the input and output ports of H.264 Encoder IP.

Table 3-2. Input and Output Ports of H.264 Encoder IP

Signal Name	Direction	Width	Description
RESET_N	Input	1	Active-low Asynchronous reset signal to the design.
PIX_CLK_I	Input	1	Input clock with which incoming pixels are sampled.
DDR_CLK_I	Input	1	Clock from DDR memory controller.
Config Interface			
HRES_I	Input	16	Horizontal resolution of input image. It must be multiple of 16, when 4k is disabled. It must be multiple of 64, when 4k is enabled.
VRES_I	Input	16	Vertical resolution of input image. It must be multiple of 16.

.....continued

Signal Name	Direction	Width	Description
QP_I	Input	6	Quality factor for H.264 quantization. The value ranges from 0 to 51 where 0 represents the highest quality and the lowest compression and 51 represents the highest compression.
PCOUNT_I	Input	8	Number of P frames per every I frame 422 format value ranges from 0 to 255.
SKIP_THRESHOLD_I	Input	12	Threshold for skip block decision This value represents the SAD value of 16 x 16 Macro block for skipping. The range is from 0 to 1024, with a typical value of 512. Higher threshold produces more skip blocks and low quality
WFRAME_START_ADDR_I	Input	7/8	DDR frame buffer address for reconstructed frames. 7 bits when the frame gap is configured for 32 MB. 8 bits when the frame gap is configured for 16 MB.
DATA_VALID_I	Input	1	Input Pixel data valid signal. Available when 4k is disabled.
DATA_Y_I	Input	8	8-bit Luma pixel input in 422 format. Available when 4k is disabled.
DATA_C_I	Input	8	8-bit Chroma pixel input in 422 format. Available when 4k is disabled.
ENABLE_I	Input	1	Drive '0' to halt the IP. It will not stop the IP in the middle of the Frame.
I_FIRCE_I	Input	1	User can force to I frame at anytime. It is pulse signal.
DATA0_O	Output	16	H.264 Slice0 encoded data output that contains NAL unit, Slice header, SPS, PPS, and the encoded data of macro blocks.
DATA0_VALID_O	Output	1	Signal denoting Slice0 encoded data is valid.
DATA1_O	Output	16	H.264 Slice1 encoded data output that contains Slice header, and the encoded data of macro blocks.
DATA1_VALID_O	Output	1	Signal denoting Slice1 encoded data is valid.
DATA2_O	Output	16	H.264 Slice2 encoded data output that contains Slice header, and the encoded data of macro blocks.
DATA2_VALID_O	Output	1	Signal denoting Slice2 encoded data is valid.
DATA3_O	Output	16	H.264 Slice3 encoded data output that contains Slice header, and the encoded data of macro blocks.
DATA3_VALID_O	Output	1	Signal denoting Slice3 encoded data is valid.
DDR_LINE_GAP_I	Input	16	Line gap between input image horizontal lines in the DDR memory.
RFRAME_START_ADDR_I	Input	7/8	DDR frame buffer address for input video frames. 7 bits when the frame gap is configured for 32 MB. 8 bits when the frame gap is configured for 16 MB.
FRAME_END_O	Output	1	End of H.264 bit stream for a frame.
Read Channel X Arbiter Interface Port X ranges from 0 to 7. The read channels 0 to 3 corresponds to input video frame read channels for slice 0 to 3 named as CF_RD_CH_x, read channels 4 to 7 corresponds to reconstructed frame read channels for slice 0 to 3 named as PF_RD_CH_x. When P frames enabled, PF_RD_CH channels are available.			

.....continued

Signal Name	Direction	Width	Description
RDATAX_I	Input	DDR AXI data width	Read data from arbiter
RVALIDX_I	Input	1	Read data valid from arbiter
ARREADYX_I	Input	1	Arbiter acknowledgment
BUSERX_I	Input	1	Read completion
ARADDRX_O	Output	32	DDR address from where read must be started
ARVALIDX_O	Output	1	Read request to arbiter
ARSIZEX_O	Output	8	Read burst size
Write Channel z Arbiter Interface Ports z ranges from 0 to 3, write channels 0 to 3 corresponds to reconstructed frame write channels for slice 0 to 3.			
AWREADYz_I	Input	1	Arbiter acknowledgment from write request
BUSERz_I	Input	1	Write completion
WDATAz_O	Output	1	Write data to arbiter
WVALIDz_O	Output	DDR AXI data width	Write data valid to arbiter
AWADDRz_O	Output	32	DDR address to which write has to be happen
AWVALIDz_O	Output	1	Write request from arbiter
AWSIZEz_O	Output	8	Write burst size
AXI4 Lite Interface Ports			
ACLK_I	Input	1	AXI clock
ARESETN_I	Input	1	Asynchronous Active-Low AXI reset
AWVALID_I	Input	1	Write address valid
AWREADY_O	Output	1	Write address ready
AWADDR_I	Input	32	Write address
WDATA_I	Input	32	Write data
WVALID_I	Input	1	Write data valid
WREADY_O	Output	1	Write data ready
BRESP_O	Output	2	Write response
BVALID_O	Output	1	Write response valid
BREADY_I	Input	1	Write response ready
ARADDR_I	Input	32	Read address
ARVALID_I	Input	1	Read address valid
ARREADY_O	Output	1	Read address ready
RREADY_I	Input	1	Read data ready
RDATA_O	Output	32	Read data
RRESP_O	Output	2	Read data response
RVALID_O	Output	1	Read valid

4. Clock Constraints (Ask a Question)

The H.264 Encoder IP uses PIX_CLK_I, ACLK_I, and DDR_CLK_I clock inputs. Clock grouping constraints must be used for place and routing to verify timing, as the IP implements the clock domain crossing logic.

5. Register Map and Descriptions (Ask a Question)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	IP_VER	7:0	IP VERSION[7:0]							
		15:8	IP VERSION[15:8]							
		23:16	IP VERSION[23:16]							
		31:24								
0x04	Control_Register	7:0							IP RESET	ENABLE/ DISABLE
		15:8								
		23:16								
		31:24								
0x08	H.264 Encoder IP type	7:0							H.264 ENCODER IP TYPE[1:0]	
		15:8								
		23:16								
		31:24								
0x0C	Q Factor	7:0			Q FACTOR[5:0]					
		15:8								
		23:16								
		31:24								
0x10	IN_Format	7:0					IN_FORMAT[3:0]			
		15:8								
		23:16								
		31:24								
0x14	P_Frame_COUNT	7:0	P_FRAME_COUNT[7:0]							
		15:8								
		23:16								
		31:24								
0x18	Input_Horizontal_Resolution	7:0	INPUT_HORIZONTAL_RESOLUTION[7:0]							
		15:8	INPUT_HORIZONTAL_RESOLUTION[15:8]							
		23:16								
		31:24								
0x1C	Input_Vertical_Resolution	7:0	INPUT_VERTICAL_RESOLUTION[7:0]							
		15:8	INPUT_VERTICAL_RESOLUTION[15:8]							
		23:16								
		31:24								
0x20	Skip Threshold	7:0	SKIP THRESHOLD[7:0]							
		15:8	SKIP THRESHOLD[15:8]							
		23:16								
		31:24								
0x24	I Frame Force	7:0								I FRAME FORCE
		15:8								
		23:16								
		31:24								
0x28	Line Gap	7:0	LINE GAP[7:0]							
		15:8	LINE GAP[15:8]							
		23:16								
		31:24								

5.1 IP Version (Ask a Question)

Name: IP_VER
Offset: 0x000
Reset: 0x20000
Property: Read-only

Current H.264 Encoder IP version number.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	IP VERSION[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	1	0

Bit	15	14	13	12	11	10	9	8
	IP VERSION[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IP VERSION[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – IP VERSION[23:0] Current H.264 Encoder IP version number.

5.2 Control Register (Ask a Question)

Name: Control_Register
Offset: 0x004
Reset: 0x1
Property: Read/Write

Register to Enable/Disable/Reset the H.264 IP.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							IP RESET	ENABLE/ DISABLE
Access							W	R/W
Reset							0	1

Bit 1 – IP RESET To reset the IP core value of '1' needs to be written once to this bit. It does not hold the written value.

Bit 0 – ENABLE/DISABLE This bit controls Enabling/Disabling the IP. Register bit value of 1 enables the IP and 0 disables.

5.3 H.264 Encoder IP type (Ask a Question)

Name: H.264 Encoder IP type
Offset: 0x008
Reset: 0x0
Property: Read-only

H.264 Encoder IP type

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							H.264 ENCODER IP TYPE[1:0]	
Access							R	R
Reset							0	0

Bits 1:0 – H.264 ENCODER IP TYPE[1:0] Denotes the current type of H.264 Encoder IP: 00 - 2k Iframe support, 01 - 2k I and P frame support, 10 - 4k Iframe support, 11 - 4k I and P frame support.

5.4 Q Factor (Ask a Question)

Name: Q Factor
Offset: 0x00C
Reset: 0x1e
Property: Write-only

Quality Factor

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			Q FACTOR[5:0]					
Access			W	W	W	W	W	W
Reset			0	1	1	1	1	0

Bits 5:0 – Q FACTOR[5:0] It denotest the quality factor for H.264 IP quantization. The values range from 0 to 51. The value of 0 represents highest quality and lowest compression. The value of 51 represents highest compression.

5.5 IN_Format (Ask a Question)

Name: IN_Format
Offset: 0x010
Reset: 0x0
Property: Read-only

Input format

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					IN_FORMAT[3:0]			
Access					R	R	R	R
Reset					0	0	0	0

Bits 3:0 – IN_FORMAT[3:0] YUV420 input format

5.6 P_Frame_COUNT (Ask a Question)

Name: P_Frame_COUNT
Offset: 0x014
Reset: 0x10
Property: Write-only

Number of P Frames for every I frame configuration

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P_FRAME_COUNT[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	1	0	0	0	0

Bits 7:0 – P_FRAME_COUNT[7:0] Range: 0-255; Default value of 16 indicates 16 P frames for every I frame

5.7 Input_Horizontal_Resolution (Ask a Question)

Name: Input_Horizontal_Resolution
Offset: 0x018
Reset: 0x780
Property: Write-only

Horizontal Resolution of the input image to the H.264 Encoder IP

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	INPUT_HORIZONTAL_RESOLUTION[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	1	1	1

Bit	7	6	5	4	3	2	1	0
	INPUT_HORIZONTAL_RESOLUTION[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	1	0	0	0	0	0	0	0

Bits 15:0 – INPUT_HORIZONTAL_RESOLUTION[15:0] Horizontal Resolution of the input image to the H.264 Encoder IP.When 4k is disabled: The value must be multiple of 16 and the input data valid must be high for the exact horizontal resolution clocks, otherwise the IP produces unexpected output.When 4k is enabled: The value must be multiples of 64, otherwise the IP will ignore the LSB bits and generates the output with maximum possible resolution which is multiple of 64.

5.8 Input_Vertical_Resolution (Ask a Question)

Name: Input_Vertical_Resolution
Offset: 0x01C
Reset: 0x430
Property: Write-only

Vertical Resolution of the input image to the H.264 Encoder IP

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	INPUT_VERTICAL_RESOLUTION[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	1	0	0

Bit	7	6	5	4	3	2	1	0
	INPUT_VERTICAL_RESOLUTION[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	1	1	0	0	0	0

Bits 15:0 – INPUT_VERTICAL_RESOLUTION[15:0] Vertical Resolution of the input image to the H.264 Encoder IP.When 4k is disabled: The value must be multiple of 16 and the number of input data valid falling edges must be same as vertical resolution, otherwise the IP produces unexpected output.When 4k is enabled: The value must be multiples of 16, otherwise the IP will ignore the LSB bits and generates the output with maximum possible vertical resolution which is multiple of 16.

5.9 Skip Threshold (Ask a Question)

Name: Skip Threshold
Offset: 0x020
Reset: 0x200
Property: Write-only

Macro block error threshold for generating skip blocks in P Frame.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	SKIP THRESHOLD[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	1	0

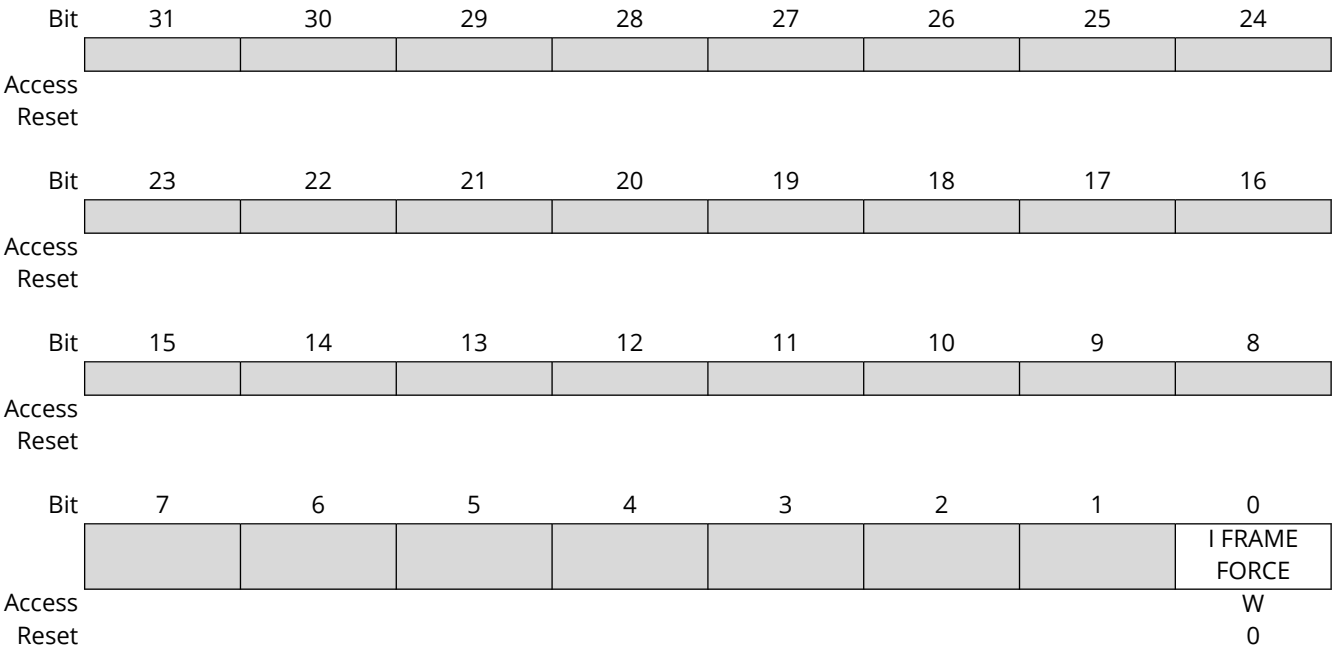
Bit	7	6	5	4	3	2	1	0
	SKIP THRESHOLD[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SKIP THRESHOLD[15:0] Threshold for skip block decision. This value represents the SAD value of 16 x 16 Macro block for skipping. The range is from 0 to 1024, with a typical value of 512. Higher threshold produces more skip blocks and higher compression with reduced quality.

5.10 I Frame Force (Ask a Question)

Name: I Frame Force
Offset: 0x024
Reset: 0x0
Property: Write-only

forces the current frame to I frame



Bit 0 – I FRAME FORCE Write 1 to this bit forces the current frame encoding to I frame

5.11 Line Gap (Ask a Question)

Name: Line Gap
Offset: 0x028
Reset: 0x2000
Property: Write-only

Line Gap or address offset between two adjacent lines of the frame stored in DDR memory

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	LINE GAP[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	1	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LINE GAP[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – LINE GAP[15:0] Line Gap between image lines stored in DDR memory. IP uses it when 4K is enabled to read input image from DDR memory

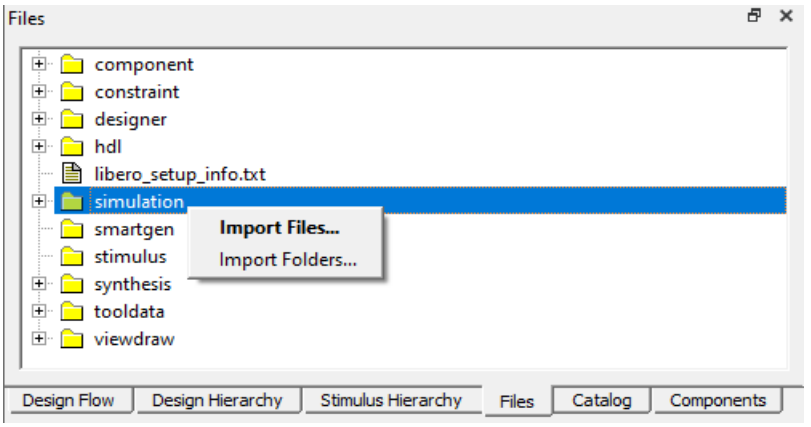
6. Testbench Simulation (Ask a Question)

Testbench is provided to check the functionality of H.264 Encoder IP core. The simulation uses a 224 x 224 or 512 x 240 image in YCbCr422 format represented by two files, each for Y and C as input and generates a H.264 file format that contains two frames.

To simulate the core using the testbench, perform the following steps:

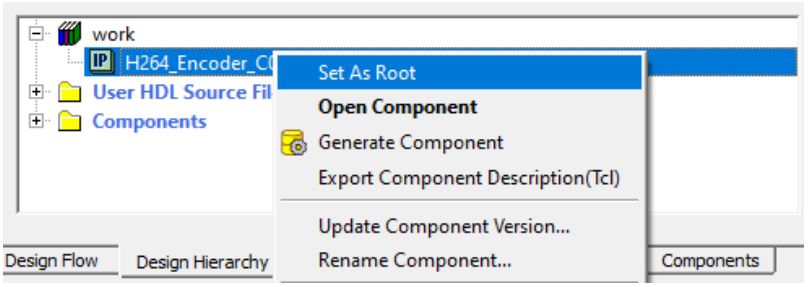
1. Navigate to Libero® SoC Catalog, select **View** > **Windows** > **IP Catalog**, and then expand **Solutions-Video**. Double-click **H264_Encoder**, configured as required and then click **OK**. H264_Encoder IP appears on the **SmartDesign** canvas.
2. Navigate to the **Files** tab, select **Simulation** > **Import Files**.
3. Import the `H264_Input.dat` and `H264_refOut.txt` files from the following path: `..\<Project_name>\component\Microchip\SolutionCore\H264_Encoder\<IP Version>\Stimulus\<IP type>`.
4. To import a different file, browse the folder that contains the required file, and click **Open**. The imported file is listed under simulation, see the following figure.

Figure 6-1. Imported Files



5. On the **Design Hierarchy** tab, right-click **H264_Encoder_C0**, and then select **Set As Root**.

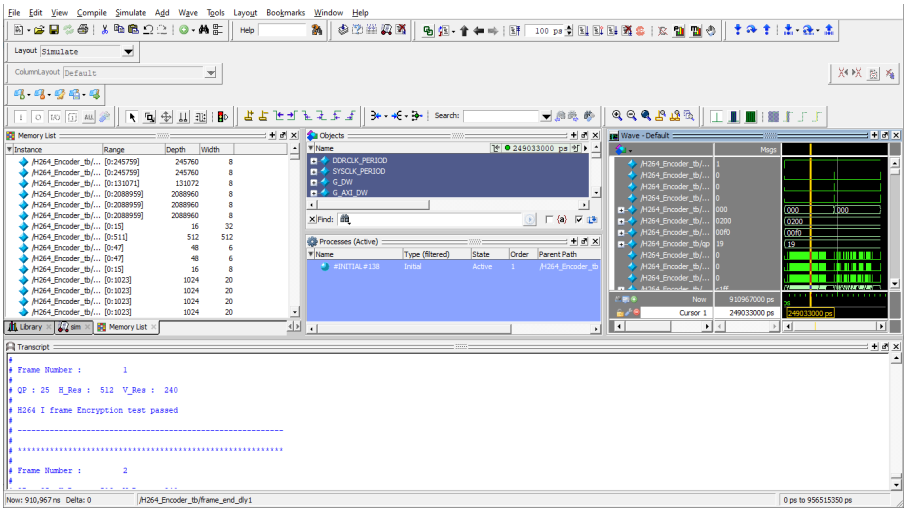
Figure 6-2. Set As Root



6. On the **Stimulus Hierarchy** tab, right-click **H264_Encoder_tb (H264_Encoder_tb. v)** testbench file, and then click **Simulate Pre-Synth Design** > **Open Interactively**. The IP is simulated for two frames.

The QuestaSim tool opens with the testbench, as shown in the following figure.

Figure 6-3. QuestaSim Simulation Window



Important: If the simulation is interrupted due to the runtime limit specified in the `.do` file, use the `run -all` command to complete the simulation.

7. System Integration (Ask a Question)

This section provides a guidance to facilitate the seamless integration of H.264 IP.

7.1 System Integration for Resolutions up to FHD (Ask a Question)

This section describes the system integration, which includes support for I-frame only, as well as support for both I and P frames up to FHD resolutions.

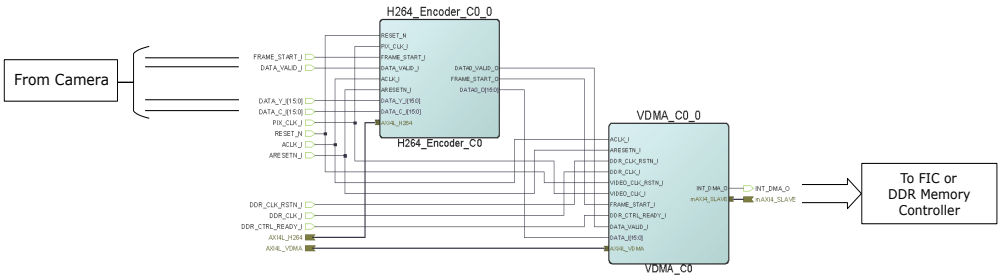
Only with I Frames Support

The following figure illustrates the integration support for H.264 IP, exclusively with I-frame up to FHD resolution.

In this example design, the following components are part of the design:

- The H.264 IP is configured to support only I frames (4k - disable, slices - 1, and P_Frames - disable)
- The FRAME_START_I, DATA_VALID_I, DATA_Y_I, and DATA_C_I signals of H.264 Encoder IP are connected to YUV 422 video source (camera). These signals are generated on PIX_CLK_I of H.264 Encoder IP.
- AXI4 Lite interfaces need to be connected to MSS FIC or AXI4 master to configure the H.264 and VDMA IPs
- H.264 Encoder IP outputs, DATA0_VALID_O, and DATA0_O are connected to the VDMA IP
- The VDMA IP AXI4 master is to be connected to the MSS FIC slave to DMA the encoded data to DDR memory connected to the MSS. Linux® running on MSS accesses the encoded data for streaming.

Figure 7-1. Only with I Frames Support



I and P Frames Support

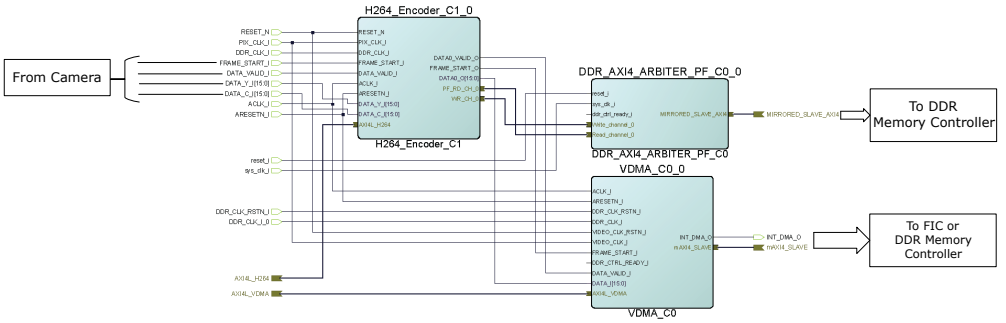
The following figure illustrates the integration support for H.264 IP, with I and P frames up to FHD resolution.

In this example design, the following components are part of the design:

- The H.264 IP is configured to support I and P frames (4k – disable, slices – 1, and P_Frames - Enable)
- The FRAME_START_I, DATA_VALID_I, DATA_Y_I, and DATA_C_I signals of H.264 Encoder IP are connected to YUV 422 video source (camera). These signals are generated on PIX_CLK_I of H.264 Encoder IP.
- AXI4 Lite interfaces need to be connected to MSS FIC or AXI4 master to configure the H.264 and VDMA IPs.
- The WR_CH_0 and PF_RD_CH_0 arbiter bus interfaces are connected to DDR_AXI4_ARBITER_PF_C0 to write and read the decoded frames from frame buffers (DDR memory).
- H.264 Encoder IP outputs, DATA0_VALID_O, and DATA0_O are connected to the VDMA IP.

- The VDMA IP AXI4 master is to be connected to the MSS FIC slave to write the encoded data to the DDR memory connected to the MSS. Linux running on MSS accesses the encoded data for streaming.

Figure 7-2. I and P Frames Support



7.2 System Integration for Resolutions up to 4K (Ask a Question)

This section describes the system integration, which includes support for I-frame only, as well as support for both I and P frames up to 4K resolutions.

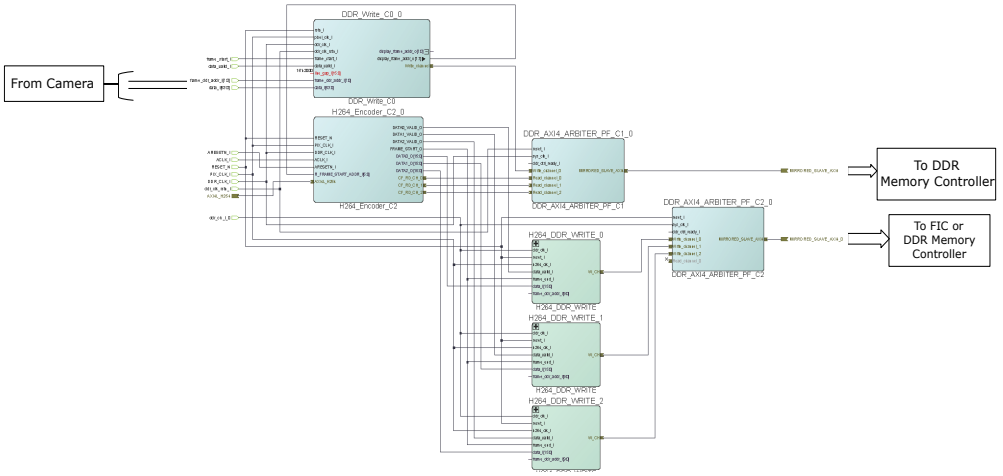
Only with I Frames Support

The following figure illustrates the integration support for H.264 IP, exclusively with I-frame up to 4K resolution.

In this example design, the following components are part of the design:

- The H.264 IP is configured to support only I frames (4k - Enable, slices - 3, and P_Frames - disable)
- The DDR Write IP is connected to a YUV 422 video source (camera) and DDR_AXI4_ARBITER_PF_C1 to write the source frames into frame buffers (DDR memory).
- The H.264 Encoder IP CF_RD_CH_x arbiter bus interfaces are connected to DDR_AXI4_ARBITER_PF_C1 to read the video source frames
- The H.264 Encoder IP PIX_CLK_I need to drive from clock source of 175 MHz to get 60 fps frame rate
- AXI4 Lite interface needs to be connected to MSS FIC or AXI4 master to configure the H.264
- H.264 Encoder IP outputs, DATAx_VALID_O, and DATAx_O are connected to H264_DDR_WRITE AXI4 master RTL logic
- Three instances of H264_DDR_WRITE RTL logic are used to pack the encoded data of each slice and write to the DDR memory connected to MSS through DDR_AXI4_ARBITER_PF_C2 and MSS FIC slave. Linux running on MSS accesses the encoded data slice by slice for streaming.

Figure 7-3. Only with I Frames Support



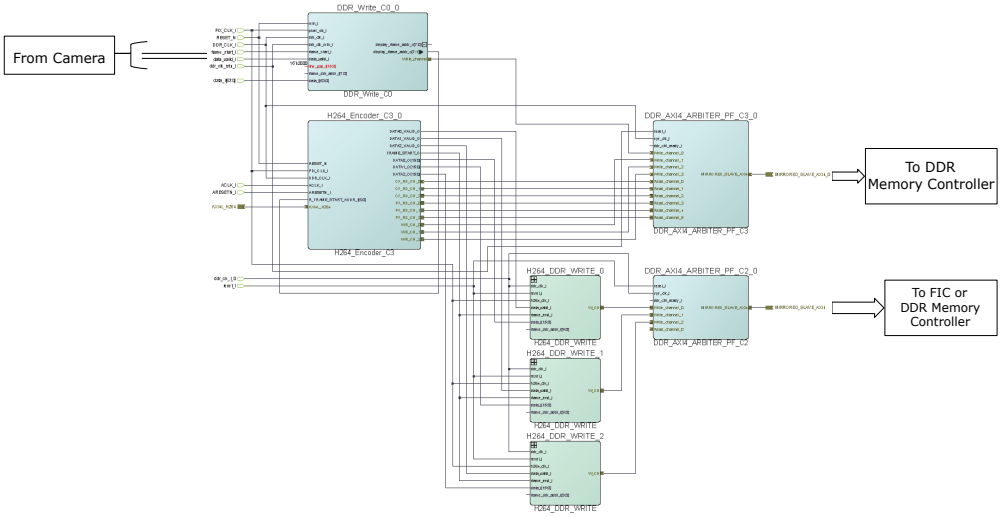
I and P Frames Support

The following figure illustrates the integration support for H.264 IP, with I and P frames up to 4K resolution.

In this example design, the following components are part of the design:

- The H.264 IP is configured to support I and P frames (4k - Enable, slices - 3, and P_Frames - Enable)
- The DDR Write IP is connected to a YUV 422 video source (camera) and DDR_AXI4_ARBITER_PF_C3 to write the source frames into frame buffers (DDR memory).
- The H.264 Encoder IP CF_RD_CH_x arbiter bus interfaces are connected to DDR_AXI4_ARBITER_PF_C3 to read the video source frames
- The H.264 Encoder IP PIX_CLK_I need to drive from clock source of 175 MHz to get 60 fps frame rate
- AXI4 Lite interface needs to be connected to MSS FIC or AXI4 master to configure the H.264
- The WR_CH_x and PF_RD_CH_x arbiter bus interfaces are connected to DDR_AXI4_ARBITER_PF_C3 to write and read the decoded frames from frame buffers (DDR memory).
- H.264 Encoder IP outputs, DATAx_VALID_O, and DATAx_O are connected to the H264_DDR_WRITE AXI4 master RTL logic
- Three instances of H264_DDR_WRITE RTL logic are used to pack the encoded data of each slice and write to the DDR memory connected to MSS through DDR_AXI4_ARBITER_PF_C2 and MSS FIC slave. Linux running on MSS accesses the encoded data slice by slice for streaming.

Figure 7-4. I and P Frames Support



8. Revision History (Ask a Question)

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 8-1. Revision History

Revision	Date	Description
B	07/2024	The following is the list of changes in revision B of the document: • Updated "H.264 4K I-Frame Encoder" to "H.264 Encoder" • Updated Introduction section • Updated Table 2 and added Table 3 and Table 4 in Resource Utilization section • Updated 1. H.264 Encoder IP Configurator section • Updated Figure 2-6, added Figure 2-1 through Figure 2-4 in 2. Hardware Implementation section • Removed 16 x 16 Matrix Framer, 8 x 8 Matrix Framer, and 4 x 4 Matrix Framer sections • Added 2.1.4. Motion Estimation and Compensation, 2.1.8. DDR Write Channel and Read Channel, and 4. Clock Constraints sections • Updated Table 3-1 in 3.1. Configuration Parameters section • Updated Read channel ports and added Write channel ports inTable 3-2 in 3.2. Inputs and Outputs section • Updated 6. Testbench Simulation section • Added 7. System Integration section
A	01/2023	Initial Release.

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