

**VSC8584**  
**Application Note**  
**VSC8584 Family Revision A/B 1588 Timestamp Out-of-Sync (OOS) Summary**

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a  MICROCHIP company

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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.0

Revision 1.0 was published in August 2017. It was the first publication of this document.

## 2 1588 Timestamp Out-of-Sync (OOS)

This document describes the susceptibility of the VSC8584 family of devices (revision A and B die) to incorrectly process timestamps within the IEEE 1588 block. When IEEE 1588 functionality is enabled, the device should process precision time protocol (PTP) frames by inserting or modifying timestamps within these packets. Certain link conditions, signal impairments, and protocol events can lead to a loss of timestamp coherency, commonly termed out-of-sync (OOS). The methods and impact of entering OOS as well as the software mitigation and recovery routine are covered.

The VSC8584 device family contains several part numbers, of which the VSC8584, VSC8582, and VSC8575 base part numbers have an IEEE 1588 block, and are therefore relevant to this document. Different revisions and grade devices exist within each base part number and are indicated by different dash extensions (for example, VSC8584XKS-10). A device's full part number is visibly marked on the top of each package. The die revision can be determined by reading the last letter of the device's datecode, also printed on the top of the package. The die revisions A and B are impacted by the loss of timestamp coherency issue, and are addressed within this document.

### 2.1 Loss of Timestamp Coherency

The VSC8584, VSC8582, and VSC8575 devices support the IEEE 1588 functionality by timestamping classified frames with a timestamp based on a calibrated local time counter (LTC) located within the device. The classification of the frame can be based on various types of supported PTP encapsulations, such as PTPoE, PTP-over-IP, and so on.

Timestamp coherency is impacted by several factors. Link conditions such as cable cuts, SFP pulls, auto-negotiations (ANEG), link flaps due to link reprovisioning, toggling the power-down management bit in MII register 0, or impairments may truncate packets. Signal impairments, especially to the reference clock for the 1588 engine, will impact the engine's behavior and accuracy.

Under normal operating conditions, the device will generate a timestamp upon reception of any packet, either at the MAC or media interface. Although every packet creates a timestamp, only PTP-classified packets will require its timestamp for further processing. Timestamps of non-classified packets will traverse the processor, but not be used. Based on the 1588 operating mode, PTP-related timestamps may be directly inserted into PTP frames at a specific field location, and/or added to the correction field of the packet. The process for ingress PTP frames is the same as egress PTP frames. The scope of each timestamp is strictly local to the frame for which it is generated.

For each frame reception, regardless of the classification, the following operations are expected:

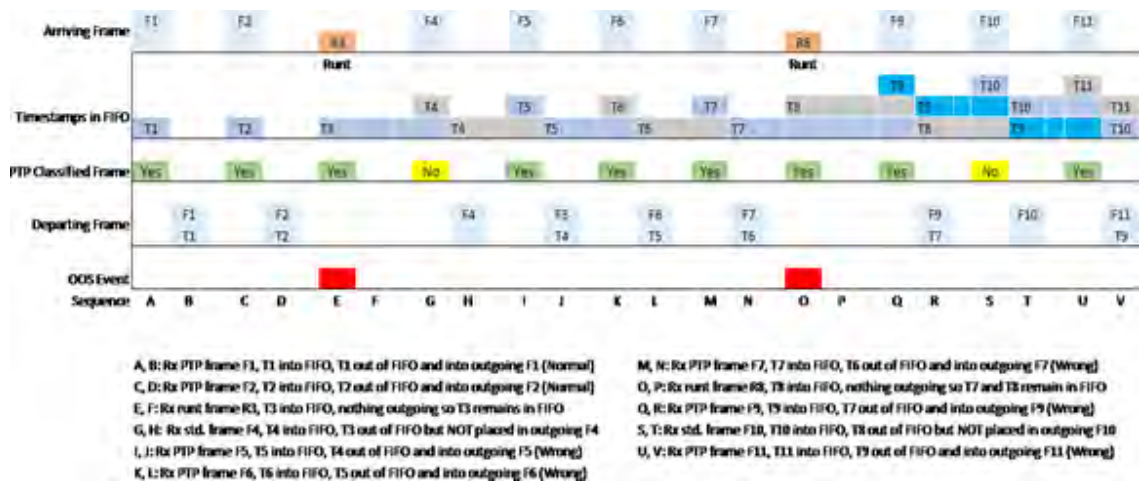
- Push timestamp entry into the TSP\_FIFO corresponding to frame reception on the media or MAC interface (depending on the direction: ingress or egress).
- Optional write of the timestamp from the head of the TSP\_FIFO into the frame upon its departure.
- Pop the timestamp entry from the TSP\_FIFO when the frame completes.

Every time a start of frame is detected at the interface, a timestamp is generated and pushed into the TSP\_FIFO, which will hold this entry until a pop operation is issued to pull the FIFO's next entry before the frame is written with this timestamp upon its departure from the 1588 processor. However, if for some reason every frame received does not have a corresponding pop operation, the FIFO will accumulate an extra timestamp, causing subsequent packets to be loaded with the incorrect timestamp.

It is possible that link events such as link breaks, cable pulls, link flaps, or certain traffic interruptions may meet the defined criteria and cause the TSP\_FIFO to go out-of-sync. Frames following an OOS condition will be timestamped with the time from past frames. This continues for every classified frame thereafter, until the OOS condition is cleared.

The following illustration shows the sequence of events relating to timestamps. It demonstrates two OOS conditions as a result of short or runt frames that fail to induce a corresponding TSP\_FIFO pop operation and the events that follow.

Figure 1 • Timestamp Sequence



## 2.2 Impact of Packet Size

The 1588 processor expects valid packets from the PCS/MAC in both directions, ingress and egress. These packets must be at least 64 bytes long for normal traffic. Short frames are typically a result of a link-down failure, traffic interruption due to fault signaling, or certain manual interventions such as enabling/disabling a loopback, enabling or disabling the MACsec datapath, or restarting autonegotiation during live traffic.

The 1588 processor initiates an internal start of frame (SOF) signal soon after receiving the preamble and start of frame delimiter (SFD) of a frame sequence. This signal writes the timestamp (TSP) relating to that frame into a timestamp-storing FIFO (TSP\_FIFO). An internal end of frame (EOF) signal is later triggered by several possible events and causes the TSP to be removed from the TSP\_FIFO.

The 1588 processor handles short frames (shorter than 64 bytes) in different ways. The handling of short frames depends on a variety of factors that are specific to the detailed frame content presented by the internal physical coding sublayer (PCS), but generally fall into the following three categories:

- Frames with 25 bytes or more (including preamble) are handled properly with a pair of internal SOF/EOF signal triggers inside the 1588 processor.
- Frames with 7 bytes or few (including preamble, with no SFD) are handled properly. Because the short frame does not initiate an internal SOF signal due to missing SFD, the block does not initiate a timestamp.
- Frames with 8 bytes to 24 bytes (inclusive) may cause a loss of timestamp coherency. In this case, a valid internal SOF signal is created, thus a timestamp is entered into the TSP\_FIFO, but the internal EOF signal generation is influenced by control characters, faults, and their location.

As the “at-risk” short frames composed of 8 bytes to 24 bytes can only manifest in the presence of a system fault condition, the remaining subsections cover those fault areas of concern.

## 2.3 Impact of Link Status

As previously discussed, the positioning and handling of faults are a significant contributor to the initiation of OOS. During a link transition from up to down or down to up, external factors (such as RJ45 plug tension, optical module stabilization, SerDes lock and stabilization, and PCS synchronization) all result in some amount of PCS-codeword chatter that may impact the MAC as well as assertion of link up or down by the PHY. During this chatter, fault codes may appear that affect the internal SOF/EOF signal triggering inside the 1588 processor.

As a result of such non-determinism, a link transition must be assumed fatal to the timestamp coherency of the 1588 processor.

## 2.4 Impact of Local Time Counter Clock

The local time clock is the primary clock to the 1588 processor logic. Signals are transferred from the PCS block into the 1588 processor, which operates in different clock domains. Synchronization logic is used to ensure proper signal transfer between domains. The SOF signal from the PCS domain is stretched to three words (24 ns) as it crosses to the 1588 processor domain. Assuming the lowest allowed 1588 processor clock frequency of 125 MHz (or an 8 ns period), if one edge is missed due to a glitch or intended clock transition, the second edge will still arrive within the 24 ns SOF pulse width, thus allowing the signal to correctly cross domains. If no edges occur during the 24 ns SOF pulse, the 1588 processor domain will lose synchronization with the data path, resulting in a command FIFO error known as TSP\_CMD\_FIFO OOS.

A local time clock error greater than two clock cycles must be assumed fatal to the timestamp coherency of the 1588 processor.

**Note:** Because the local time counter (LTC) is based off the 1588 processor clock, any missing edges will result in a LTC error (for instance, the time of day value). This error will continue until the counter is reloaded or updated.

## 2.5 Impact of MACsec Datapath

The MACsec datapath elements, including the processing engine and traffic control MACs, may affect the internal SOF/EOF signal triggering inside the 1588 processor whenever the MACsec pipeline control is reconfigured (for example, by bypassing elements of the MACsec pipeline). Order-of-operations and enabling features in the MACsec pipeline to prevent short frame propagation is essential to ensure timestamp coherency through the 1588 processor datapath.

User applications utilizing the MACsec datapath need to maintain correct order-of-operations by calling the MACsec initialization functions before 1588 initialization functions during PHY configuration.

Prevention of short frame propagation through the MACsec datapath is handled by the API. However, API revision 4.67.03 or newer is required for all of these capabilities.

## 2.6 Impact on Revision A Silicon

Revision A devices (VSC8584XKS-10/13 and VSC8582XKS-10/13) are end-of-life products, superseded by the pin-compatible revision B. With regards to all of the described potential losses to timestamp coherency within the 1588 processor logic, no recovery routine exists for revision A die. As a result, users of revision A devices must examine packet delay variation and/or slave offset from master (OFM) in both directions to assess the need for a reset in the event a timestamp coherence error has occurred. Because there is no alternative to hardware pin reset to recover OOS for revision A silicon, the ability to eliminate other factors that degrade PDV and OFM in the PTP system is paramount for revision A applications, to assess whether hardware reset of the PHY is necessary to recover PTP performance.

## 3 Software Recovery

The software routine for revision B to recover from the OOS condition within the 1588 timestamping engine uses the on-chip Ethernet pattern generator (EPG) along with on-chip loopback modes to perform a full system recovery. A high-level description of the recovery algorithm is provided, along with resource reservations required of the host system in order to execute this recovery algorithm. Any register settings modified by the routine are saved at entry and restored prior to exit. The routine executes as a blocking process, preventing interruption by any other calls to the PHY API.

This software routine is available in PHY API revision 4.67.03 or later releases. The following events should be used to trigger the revision B device's recovery API:

- Interruption of local time clock to the 1588 engine while traffic is flowing (assuming 1588 bypass was not enabled during the interruption)

### 3.1 Recovery Procedure

The initial steps of the VSC8584 software patch will isolate the targeted recovery port in the PHY so that traffic ends in the 1588 egress block and by enabling MII isolate. The software routine utilizes register-controlled FIFO-clearing logic within the VSC8584 device in order to assure FIFO coherency within the 1588 processor.

The following transactions occur within the routine to recover the OOS condition within the 1588 timestamping engine:

- EPG generates frames using test mode configuration.
- Frames are not transmitted on the MAC side (through the MII Isolate bit) or media side because the PHY datapath is isolated early in the routine.
- SW\_POP\_FIFO register commands are executed for the ingress and egress 1588 blocks to clear any errors in the 1588 FIFOs.
- Check that SW\_POP\_FIFO commands successfully completed; if unsuccessful, repeat recovery steps while packet mode datapath is enabled.

Once complete, the EPG is disabled and the 1588 engine configuration is restored to the original configuration programmed by the user PTP application, packet mode datapath is disabled (if OOS recovery needed to enable it), and external frame traffic is re-enabled in the PHY datapath.

### 3.2 API Call

The software recovery API referenced in this application note does not require the user to add compilation defines to include VSC8584 OOS recovery. The following compilation defines are already enabled within the PHY API fileset in order to include the VSC8584 OOS Recovery code: VIPER\_B\_FIFO\_RESET and VIPER\_B\_FIFO\_RESET\_API\_CALL.

With these compilation options, the call within the 1588 API for a user to execute the recovery is as follows:

```
vtss_rc vtss_phy_ts_viper_fifo_reset(const vtss_inst_t inst,
const vtss_port_no_t port_no, const vtss_phy_ts_fifo_conf_t *fifo_conf)
```

This function will in turn call other functions to perform the steps outlined in 5.1.1, depending upon the intended response. See the 1588 API header file, for a strict definition of the function arguments to `vtss_phy_ts_viper_fifo_reset()`.

**Note:** Direct calls from the user application are only needed in the operational situations outlined in this document. The PHY API OOS recovery routine may execute twice-in-a-row whenever it is called from the user application.

### 3.3 Design Considerations

The PHY API OOS recovery routine should never be called while the PHY is in packet mode (that is, when MACsec is enabled).

The following sequence is appropriate for invoking the OOS routine if the device is configured in packet mode.

1. Drop links on both the MAC and media interface of the PHY
2. Enable 1588 bypass
3. Shut down MACsec engine
4. Disable 1588 bypass
5. Call the OOS recovery routine
6. Enable 1588 bypass
7. Enable MACsec engine
8. Disable 1588 bypass
9. Restore links on both the MAC and media interface of the PHY.

**Note:** The shutdown of the MACsec engine in step three shall be a complete deletion of the SecY for the physical port executing OOS recovery, as well as using the `vtss_macsec_init_set()` API with the `enable` parameter set to `FALSE`. Always refer to the MACsec Programming User Guide on the VSC8584 product page for the best programming practices for the MACsec engine.

The software workaround for VSC8584 will drop both the MAC and media interface links during execution. No frame traffic will traverse the device while the workaround is executing. Execution time will vary based on MDIO utilization for a customer application, but typically will complete in less than

500 ms per call to `vtss_phy_ts_viper_fifo_reset()`.

After execution all PHY configuration is restored to its original state programmed by the user PTP application, and external frame flow resumes.

## 4 Frequently Asked Questions

### 4.1 Is the out-of-sync timestamp FIFO the one accessed by MDIO or read out by the SPI interface?

No. The FIFO is internal to the 1588 engine datapath and is not directly accessible through the PHY management interface.

### 4.2 Can we write our own recovery method for the out-of- sync timestamp FIFO?

Microsemi will only support the recovery API referenced in this application note and provided by Microsemi engineering.

### 4.3 Can we avoid changing the Microsemi PHY API software?

Adding the software patch will require a software upgrade to the system.

### 4.4 Which 1588-capable VSC8584 family devices have OOS recovery API capability?

The mapping of revisions is listed in the following table.

**Table 1 • VSC8584 Family Part Numbers**

Part Number	Software OOS Recovery API Available
VSC8584XKS-11	Yes
VSC8584XKS-14	Yes
VSC8582XKS-11	Yes
VSC8582XKS-14	Yes
VSC8575XKS-11	Yes
VSC8575XKS-14	Yes
VSC8584XKS-10	No
VSC8584XKS-13	No
VSC8582XKS-10	No
VSC8582XKS-13	No

### 4.5 Are there resource constraints on the 1588 timestamping engine for the OOS recovery routine?

No elements of the VSC8584 1588 timestamping engine need a pre-determined configuration in order to properly execute the OOS recovery routine.

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