# MIC26603

## 28V, 6A HyperLight Load® Synchronous DC/DC Buck Regulator

### Features

- HyperLight Load® Efficiency: Up to 80% at 10 mA
- Hyper Speed Control® Architecture Enables
  - High Delta V Operation ($V_{IN}$ = 28V and $V_{OUT}$ = 0.8V)
  - Small Output Capacitance
- Input Voltage Range: 4.5V to 28V
- Output Current up to 6A
- Up to 95% Efficiency
- Adjustable Output Voltage from 0.8V to 5.5V
- ±1% Feedback Accuracy
- Any Capacitor™ Stable: Zero-to-High ESR
- 600 kHz Switching Frequency
- Power Good (PG) Output
- Foldback Current Limit and “Hiccup Mode” Short-Circuit Protection
- Safe Start-Up into Pre-Biased Loads
- 5 mm x 6 mm VQFN Package
- –40°C to +125°C Junction Temperature Range

### Applications

- Distributed Power Systems
- Telecom/Networking Infrastructure
- Printers, Scanners, Graphic Cards, and Video Cards

### General Description

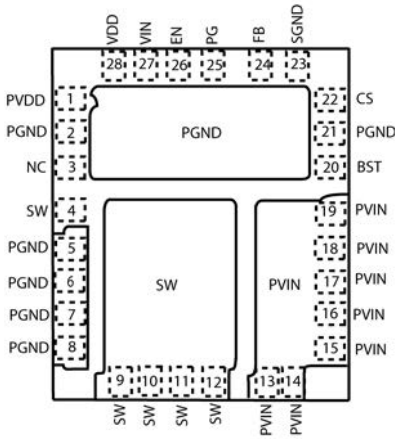
The MIC26603 is a constant-frequency, synchronous DC/DC buck regulator that features adaptive on-time control architecture. The MIC26603 operates over a supply range of 4.5V to 28V. It has an internal linear regulator that provides a regulated 5V to power the internal control circuitry. MIC26603 operates at a constant 600 kHz switching frequency in continuous-conduction mode and can be used to provide up to 6A of output current. The output voltage is adjustable down to 0.8V.

Microchip’s HyperLight Load® architecture provides the same high-efficiency and ultra-fast transient response as the Hyper Speed Control® architecture under medium to heavy loads, but also maintains high efficiency under light load conditions by transitioning to variable-frequency, discontinuous-mode operation.

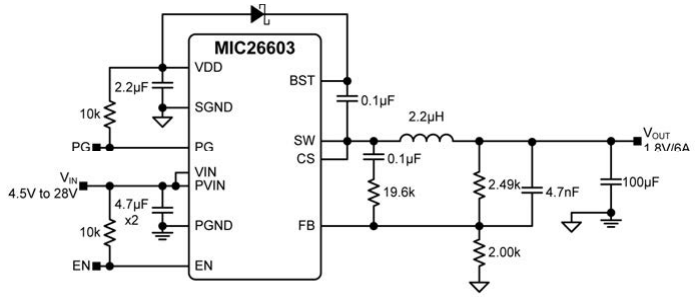
The MIC26603 offers a full suite of protection features to ensure protection of the IC during fault conditions. These include undervoltage lockout to ensure proper operation under power-sag conditions, thermal shutdown, internal soft-start to reduce the inrush current, foldback current limit and “hiccup mode” short-circuit protection. The MIC26603 includes a Power Good (PG) output to allow simple sequencing.

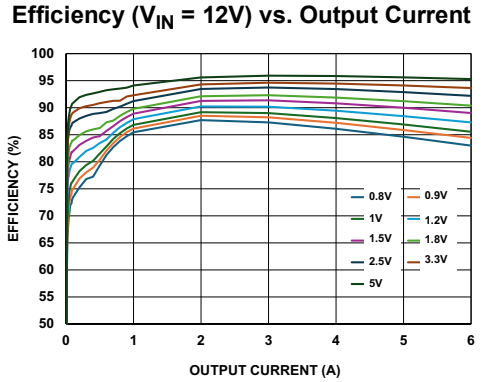
### Package Type

**MIC26603**
28-Lead VQFN (JL)
(Top View)

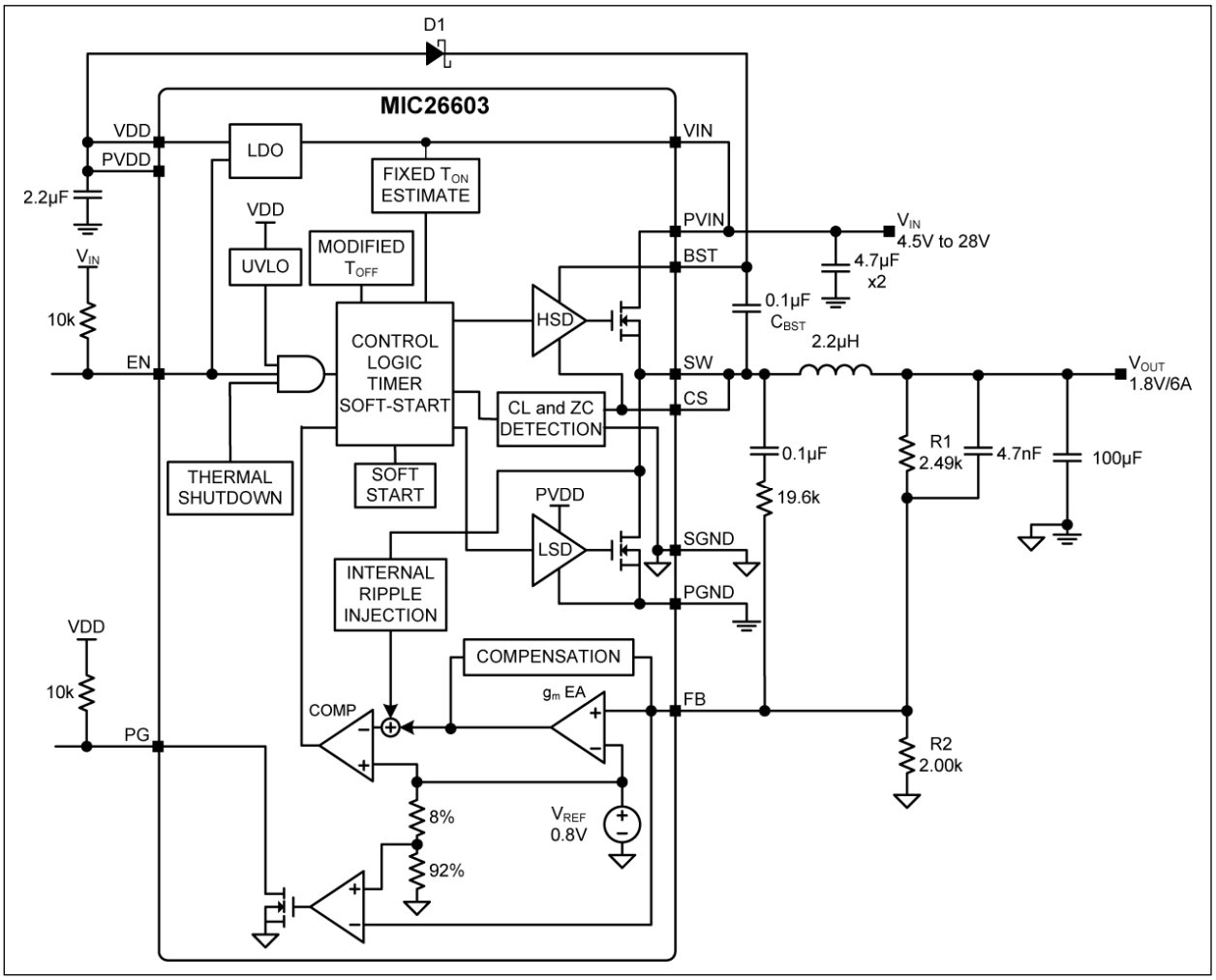


## Typical Application Circuit




## Functional Block Diagram



# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings †

$PV_{IN}$ to PGND ..... –0.3V to +29V
$V_{IN}$ to PGND ..... –0.3V to $PV_{IN}$
$PV_{DD}$, $V_{DD}$ to PGND ..... –0.3V to +6V
$V_{SW}$, $V_{CS}$ to PGND ..... –0.3V to ($PV_{IN}$ + 0.3V)
$V_{BST}$ to $V_{SW}$ ..... –0.3V to +6V
$V_{BST}$ to PGND ..... –0.3V to +35V
$V_{FB}$, $V_{PG}$ to PGND ..... –0.3V to ($V_{DD}$ + 0.3V)
$V_{EN}$ to PGND ..... –0.3V to ($V_{IN}$ + 0.3V)
PGND to SGND ..... –0.3V to +0.3V

## Operating Ratings ‡

Supply Voltage ($PV_{IN}$, $V_{IN}$) ..... +4.5V to +28V
PVDD, VDD Supply Voltage ($PV_{DD}$, $V_{DD}$) ..... +4.5V to +5.5V
Enable Input ($V_{EN}$) ..... 0V to $V_{IN}$
Maximum Power Dissipation ..... Note 1

**† Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Device is ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

**‡ Notice:** The device is not guaranteed to function outside its operating ratings.

**Note 1:** $P_{D(MAX)} = (T_{J(MAX)} – T_A)/\theta_{JA}$, where $\theta_{JA}$ depends upon the printed circuit layout. A 5 square inch 4 layer, 0.62”, FR-4 PCB with 2 oz finish copper weight per layer is used for the $\theta_{JA}$.

## ELECTRICAL CHARACTERISTICS

$PV_{IN} = V_{IN} = V_{EN}$ = 12V, $V_{BST} – V_{SW}$ = 5V; $T_A$ = +25°C, unless noted. **Bold** values valid for –40°C ≤ $T_J$ ≤ +125°C. Note 1

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **Power Supply Input** | | | | | |
| Input Voltage Range ($V_{IN}$, $PV_{IN}$) | **4.5** | — | **28** | V | — |
| Quiescent Supply Current | — | 450 | **750** | µA | $V_{FB}$ = 1.5V (non-switching) |
| Shutdown Supply Current | — | 5 | **10** | µA | $V_{EN}$ = 0V |
| **$V_{DD}$ Supply Voltage** | | | | | |
| $V_{DD}$ Output Voltage | **4.8** | 5 | **5.4** | V | $V_{IN}$ = 7V to 28V, $I_{DD}$ = 40 mA |
| $V_{DD}$ UVLO Threshold | **3.7** | 4.2 | **4.5** | V | $V_{DD}$ Rising |
| $V_{DD}$ UVLO Hysteresis | — | 400 | — | mV | — |
| Dropout Voltage ($V_{IN} – V_{DD}$) | — | 300 | **600** | mV | $I_{DD}$ = 25 mA |
| **DC/DC Controller** | | | | | |
| Output Voltage Adjust Range ($V_{OUT}$) | 0.8 | — | **5.5** | V | — |
| **Reference** | | | | | |
| Reference Voltage | **0.792** | 0.8 | **0.808** | V | 0°C ≤ $T_J$ ≤ 85°C (±1.0%) |
| | **0.788** | 0.8 | **0.812** | V | –40°C ≤ $T_J$ ≤ 125°C (±1.5%) |
| Load Regulation | — | 0.25 | — | % | $I_{OUT}$ = 1A to 6A (Continuous Mode) |
| Line Regulation | — | 0.25 | — | % | $V_{IN}$ = 4.5V to 28V |
| FB Bias Current | — | 50 | **500** | nA | $V_{FB}$ = 0.8V |

## ELECTRICAL CHARACTERISTICS (CONTINUED)

$PV_{IN}$ = $V_{IN}$ = $V_{EN}$ = 12V, $V_{BST}$ – $V_{SW}$ = 5V; $T_A$ = +25°C, unless noted. **Bold** values valid for –40°C ≤ $T_J$ ≤ +125°C. Note 1

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **Enable Control** | | | | | |
| EN Logic Level High | **1.8** | — | — | V | — |
| EN Logic Level Low | — | — | **0.6** | V | — |
| EN Bias Current | — | 6 | **30** | µA | $V_{EN}$ = 12V |
| **Oscillator** | | | | | |
| Switching Frequency | **450** | 531 | **750** | kHz | Note 2 |
| Maximum Duty Cycle | — | 82 | — | % | Note 3, $V_{FB}$ = 0V |
| Minimum Duty Cycle | — | 0 | — | % | $V_{FB}$ = 1.0V |
| Minimum Off-Time | — | 300 | — | ns | — |
| **Soft-Start** | | | | | |
| Soft-Start Time | — | 5 | — | ms | — |
| **Short-Circuit Protection** | | | | | |
| Current-Limit Threshold | 7.5 | 13 | 18 | A | $V_{FB}$ = 0.8V, $T_J$ = 25°C |
| | 6.6 | 13 | 18 | A | $V_{FB}$ = 0.8V, $T_J$ = 125°C |
| Short-Circuit Current | — | 2.7 | — | A | $V_{FB}$ = 0V |
| **Internal FETs** | | | | | |
| Top-MOSFET $R_{DS(ON)}$ | — | 22.5 | — | mΩ | $I_{SW}$ = 3A |
| Bottom-MOSFET $R_{DS(ON)}$ | — | 10.5 | — | mΩ | $I_{SW}$ = 3A |
| SW Leakage Current | — | — | **60** | µA | $V_{EN}$ = 0V |
| VIN Leakage Current | — | — | **25** | µA | $V_{EN}$ = 0V |
| **Power Good** | | | | | |
| Power Good Threshold Voltage | **85** | 92 | **95** | $\%V_{OUT}$ | Sweep $V_{FB}$ from Low to High |
| Power Good Hysteresis | — | 5.5 | — | $\%V_{OUT}$ | Sweep $V_{FB}$ from High to Low |
| Power Good Delay Time | — | 100 | — | µs | Sweep $V_{FB}$ from Low to High |
| Power Good Low Voltage | — | 70 | **200** | mV | Sweep $V_{FB}$ < 0.9 x $V_{NOM}$, $I_{PG}$ = 1 mA |
| **Thermal Protection** | | | | | |
| Overtemperature Shutdown | — | 160 | — | °C | $T_J$ rising |
| Overtemperature Shutdown Hysteresis | — | 15 | — | °C | — |

**Note 1:** Specifications for packaged product only.

**2:** Measured in test mode.

**3:** The maximum duty cycle is limited by the fixed mandatory off-time ($t_{OFF}$) of 300 ns typical.

## TEMPERATURE SPECIFICATIONS

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Junction Temperature Range | $T_J$ | –40 | — | +125 | °C | — |
| Maximum Junction Temperature | $T_{J(MAX)}$ | — | — | +150 | °C | — |
| Storage Temperature Range | $T_S$ | –65 | — | +150 | °C | — |
| Lead Temperature | $T_{LEAD}$ | — | — | 260 | °C | Soldering, 10 sec. |
| **Package Thermal Resistances** | | | | | | |
| Thermal Resistance, VQFN 28-Ld | $\theta_{JA}$ | — | 28 | — | °C/W | Note 1 |

**Note 1:** $P_{D(MAX)} = (T_{J(MAX)} – T_A)/\theta_{JA}$, where $\theta_{JA}$ depends upon the printed circuit layout. A 5 square inch 4 layer, 0.62”, FR-4 PCB with 2 oz finish copper weight per layer is used for the $\theta_{JA}$.

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

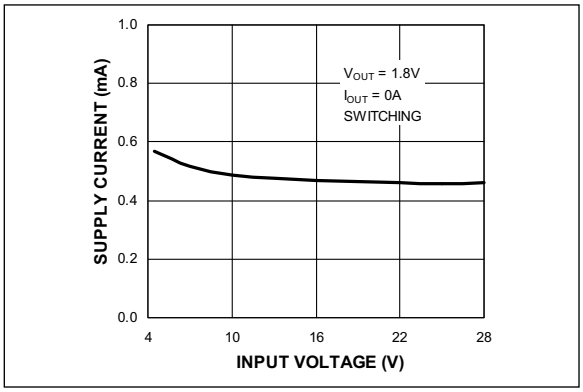



***FIGURE 2-1:*** *$V_{IN}$ Operating Supply Current vs. Input Voltage.*

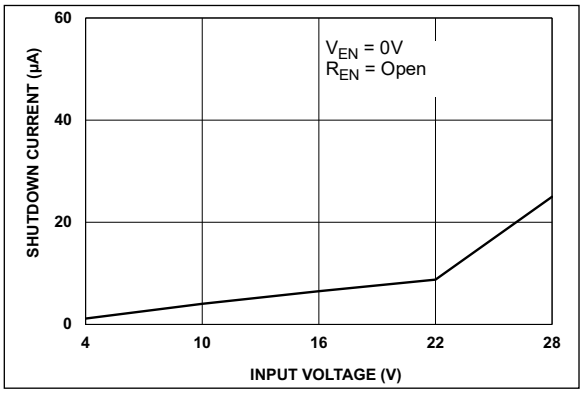



***FIGURE 2-2:*** *$V_{IN}$ Shutdown Current vs. Input Voltage.*

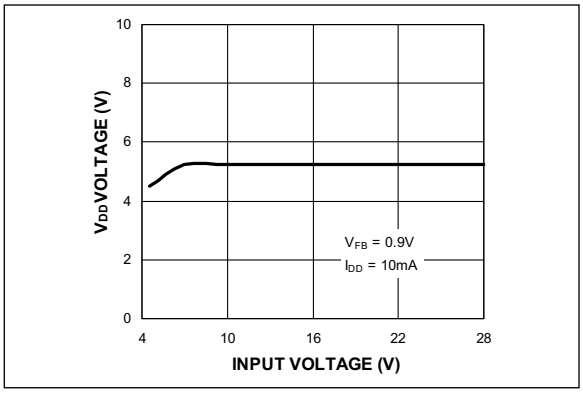



***FIGURE 2-3:*** *$V_{DD}$ Output Voltage vs. Input Voltage.*

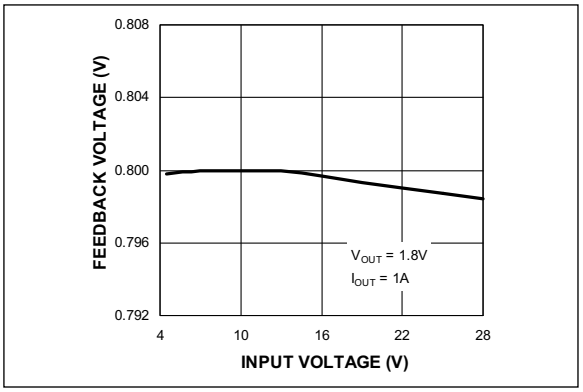



***FIGURE 2-4:*** *Feedback Voltage vs. Input Voltage.*

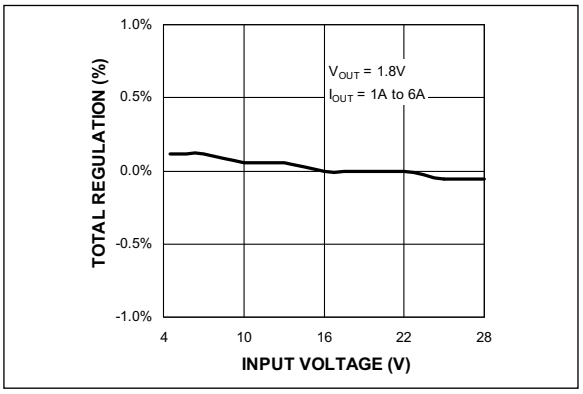



***FIGURE 2-5:*** *Total Regulation vs. Input Voltage.*

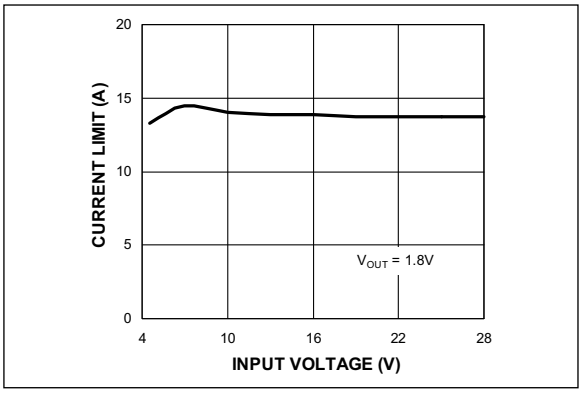



***FIGURE 2-6:*** *Current Limit vs. Input Voltage.*

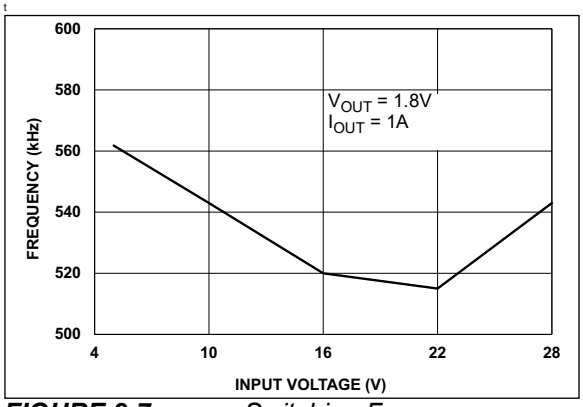



***FIGURE 2-7:*** *Switching Frequency vs. Input Voltage.*

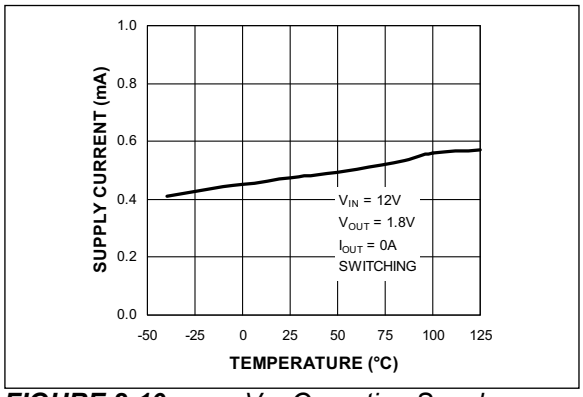



***FIGURE 2-10:*** *$V_{IN}$ Operating Supply Current vs. Temperature.*

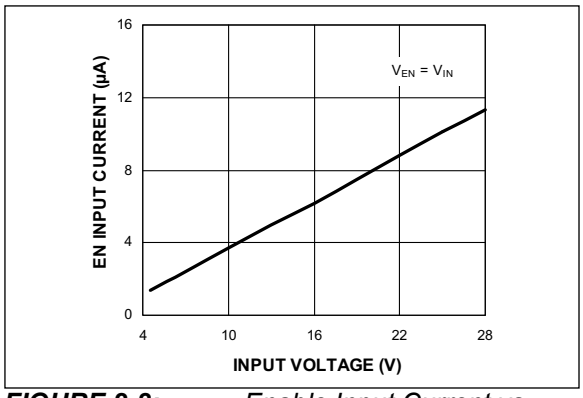



***FIGURE 2-8:*** *Enable Input Current vs. Input Voltage.*

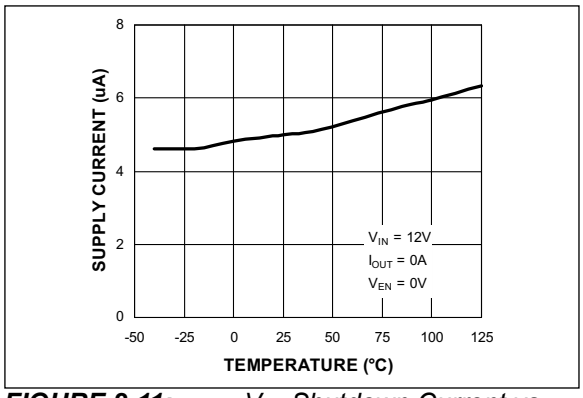



***FIGURE 2-11:*** *$V_{IN}$ Shutdown Current vs. Temperature.*

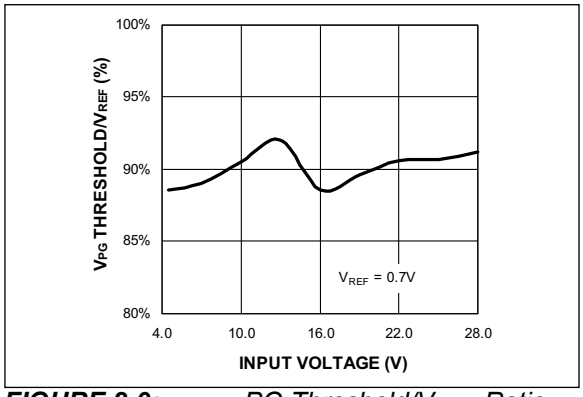



***FIGURE 2-9:*** *PG Threshold/$V_{REF}$ Ratio vs. Input Voltage.*

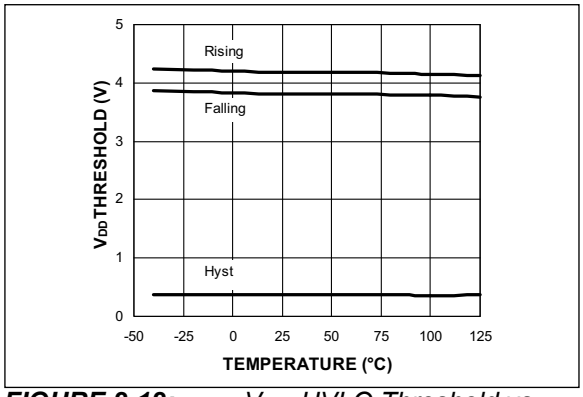



***FIGURE 2-12:*** *$V_{DD}$ UVLO Threshold vs. Temperature.*

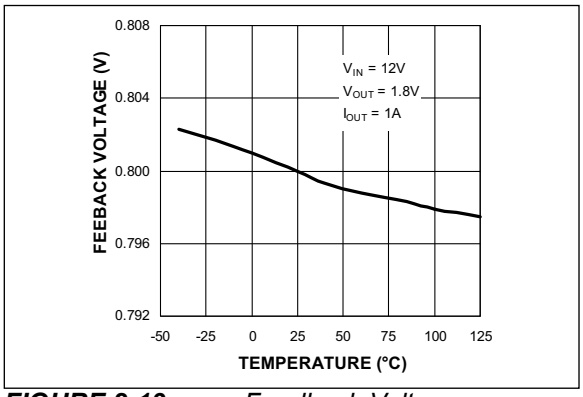



***FIGURE 2-13:*** *Feedback Voltage vs. Temperature.*

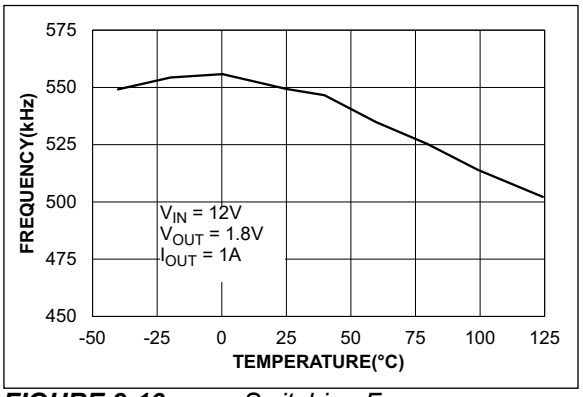



***FIGURE 2-16:*** *Switching Frequency vs. Temperature.*

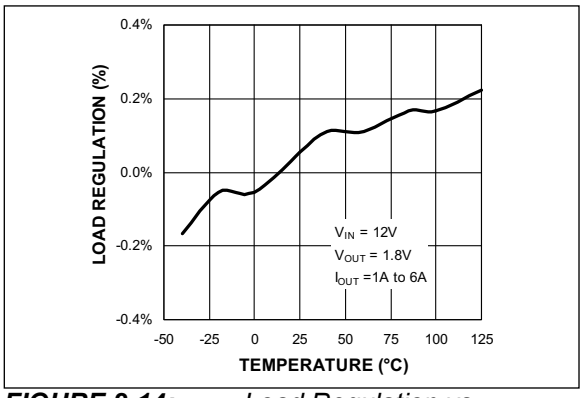



***FIGURE 2-14:*** *Load Regulation vs. Temperature.*

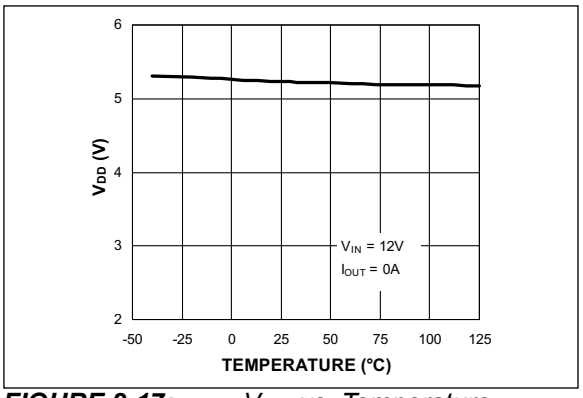



***FIGURE 2-17:*** *$V_{DD}$ vs. Temperature.*

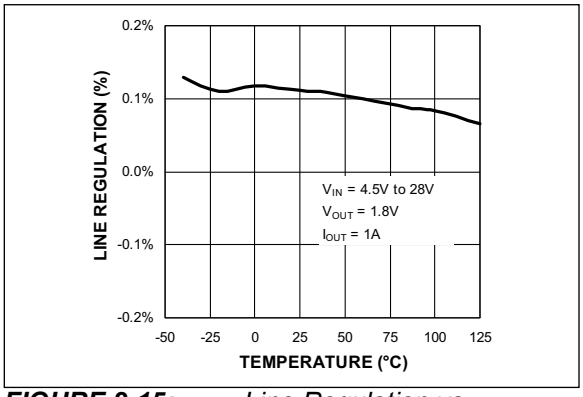



***FIGURE 2-15:*** *Line Regulation vs. Temperature.*

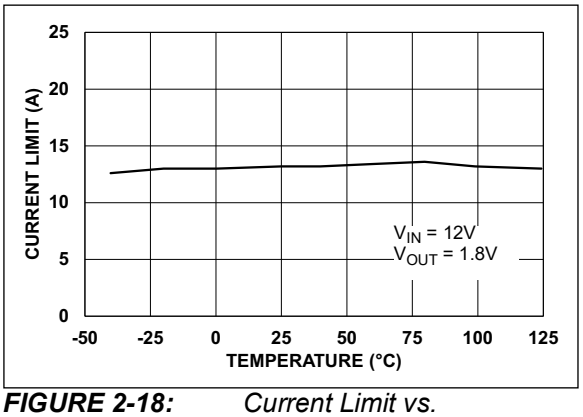



***FIGURE 2-18:*** *Current Limit vs. Temperature.*

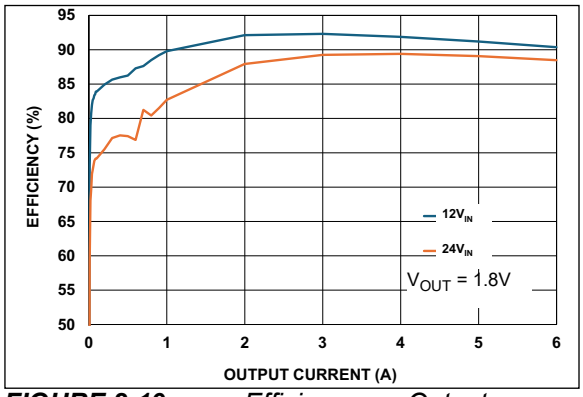



***FIGURE 2-19:*** *Efficiency vs. Output Current.*

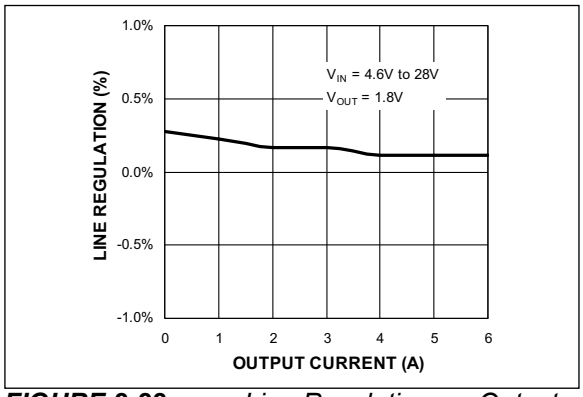



***FIGURE 2-22:*** *Line Regulation vs. Output Current.*

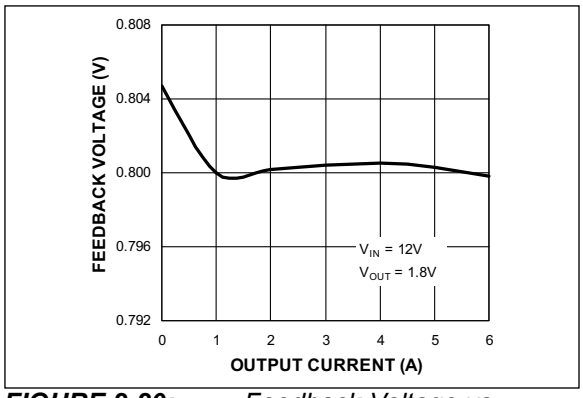



***FIGURE 2-20:*** *Feedback Voltage vs. Output Current.*

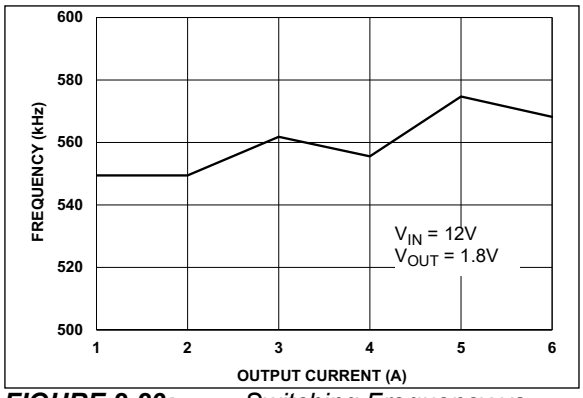



***FIGURE 2-23:*** *Switching Frequency vs. Output Current.*

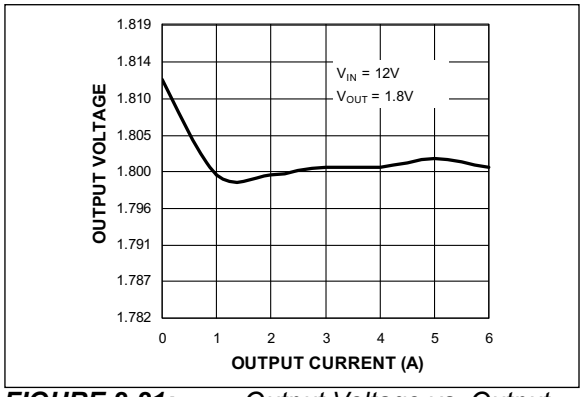



***FIGURE 2-21:*** *Output Voltage vs. Output Current.*

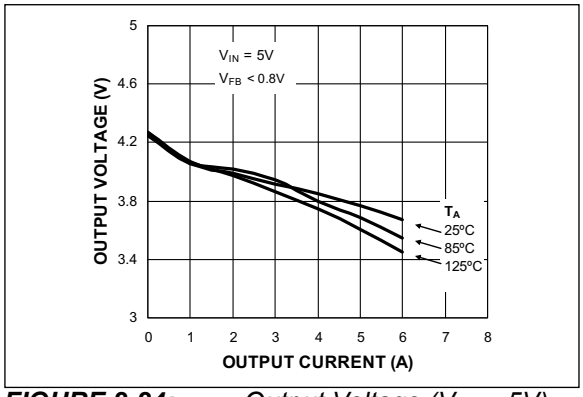



***FIGURE 2-24:*** *Output Voltage ($V_{IN}$ = 5V) vs. Output Current.*

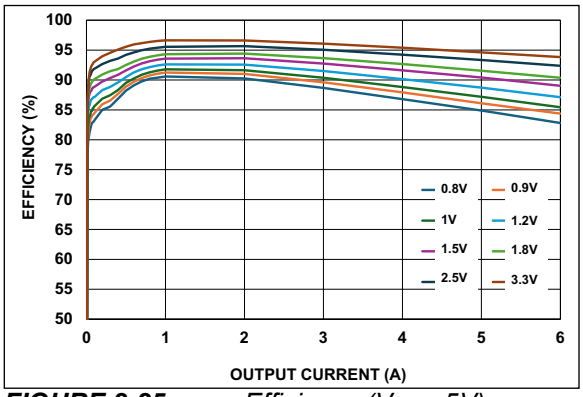



***FIGURE 2-25:*** *Efficiency ($V_{IN}$ = 5V) vs. Output Current.*

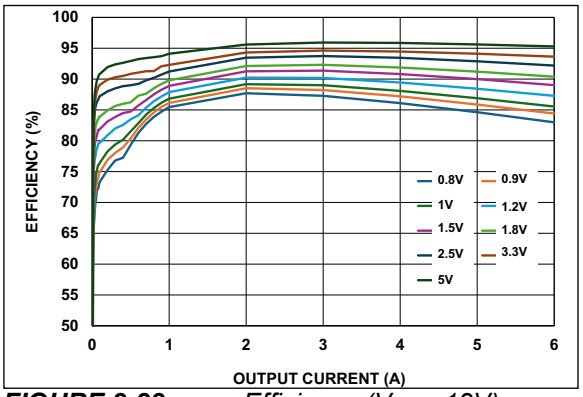



***FIGURE 2-28:*** *Efficiency ($V_{IN}$ = 12V) vs. Output Current.*

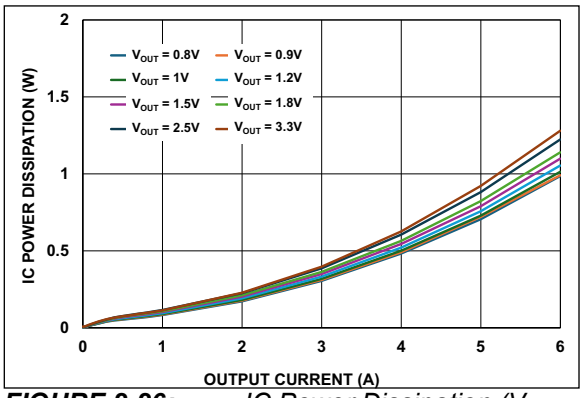



***FIGURE 2-26:*** *IC Power Dissipation ($V_{IN}$ = 5V) vs. Output Current.*

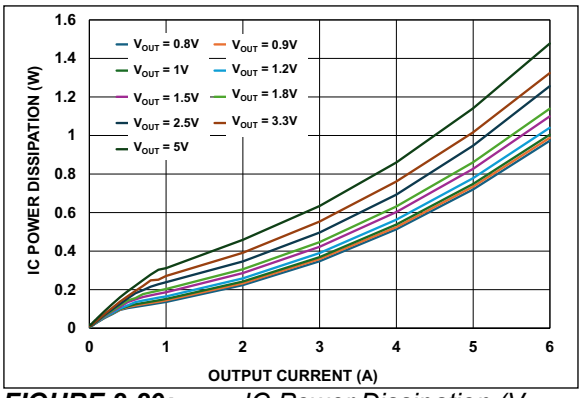



***FIGURE 2-29:*** *IC Power Dissipation ($V_{IN}$ = 12V) vs. Output Current.*

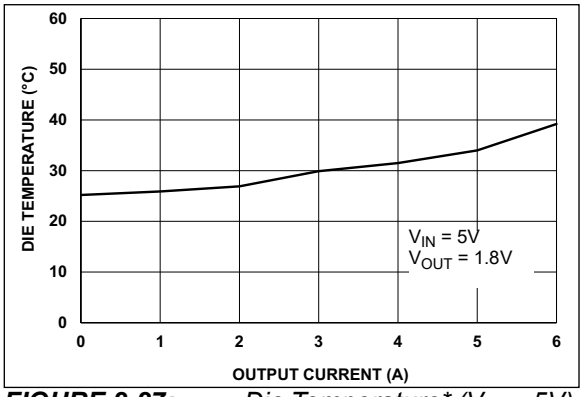



***FIGURE 2-27:*** *Die Temperature* ($V_{IN}$ = 5V) vs. Output Current.*

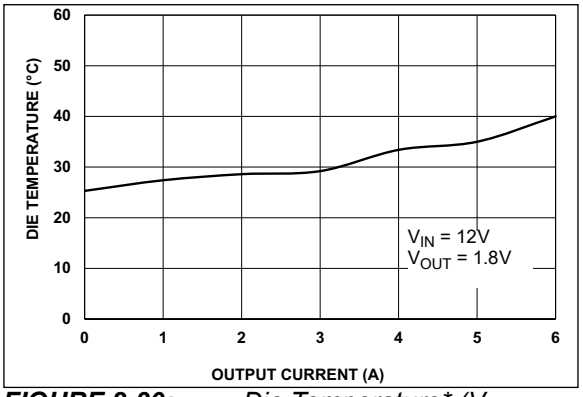



***FIGURE 2-30:*** *Die Temperature* ($V_{IN}$ = 12V) vs. Output Current.*

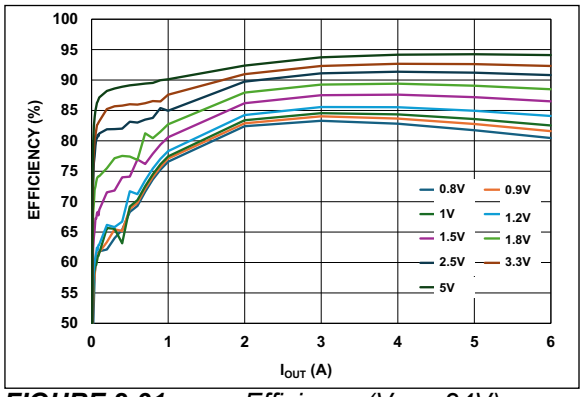



***FIGURE 2-31:*** *Efficiency ($V_{IN}$ = 24V) vs. Output Current.*

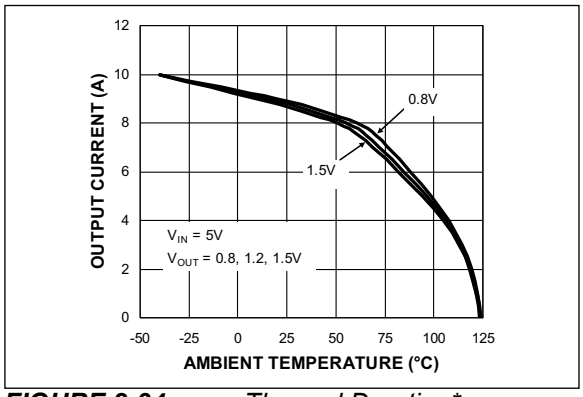



***FIGURE 2-34:*** *Thermal Derating* vs. Ambient Temperature.*

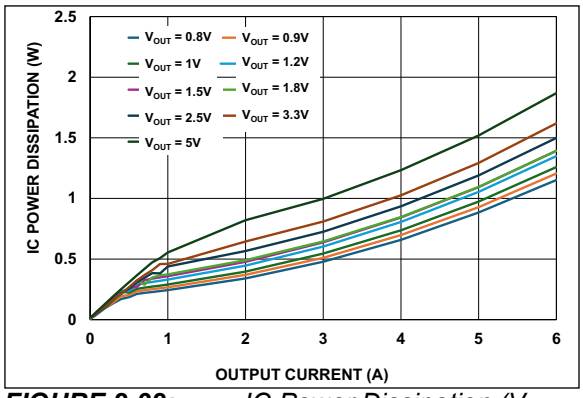



***FIGURE 2-32:*** *IC Power Dissipation ($V_{IN}$ = 24V) vs. Output Current.*

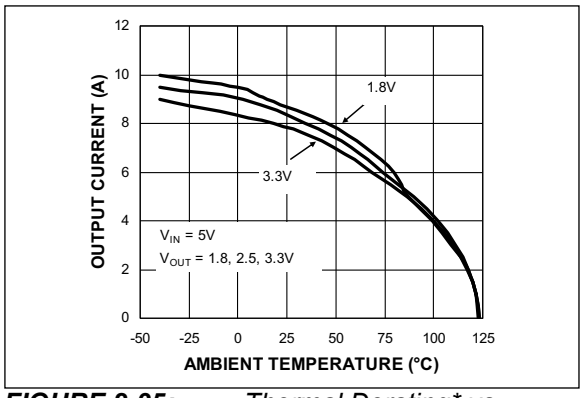



***FIGURE 2-35:*** *Thermal Derating* vs. Ambient Temperature.*

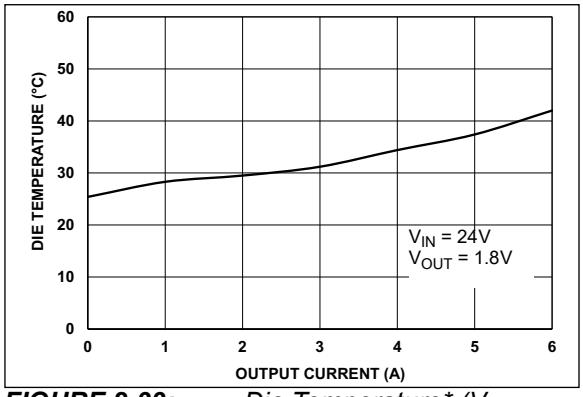



***FIGURE 2-33:*** *Die Temperature* ($V_{IN}$ = 24V) vs. Output Current.*

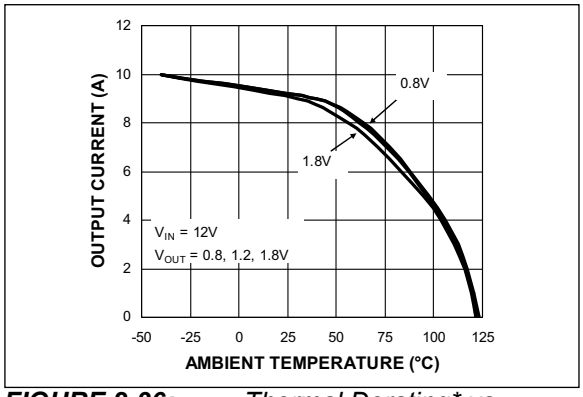



***FIGURE 2-36:*** *Thermal Derating* vs. Ambient Temperature.*

* The temperature measurement was taken at the hottest point on the MIC26603 case mounted on a 5 square inch PCB, tested in an ambient temperature of 23°C to 25°C degrees in an open space with no forced cooling. See the Thermal Measurement section. Actual results will depend upon the size of the PCB, ambient temperature, and proximity to other heat emitting components.

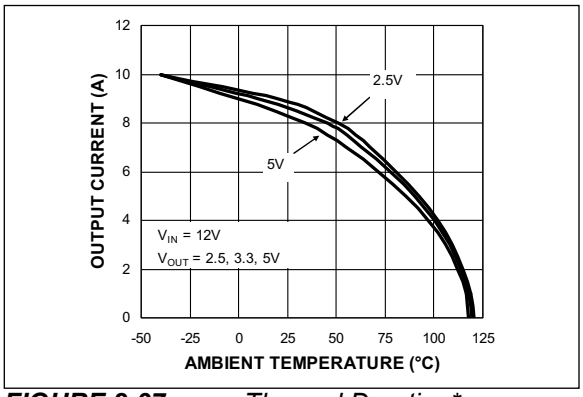



***FIGURE 2-37:*** *Thermal Derating* vs. Ambient Temperature.*

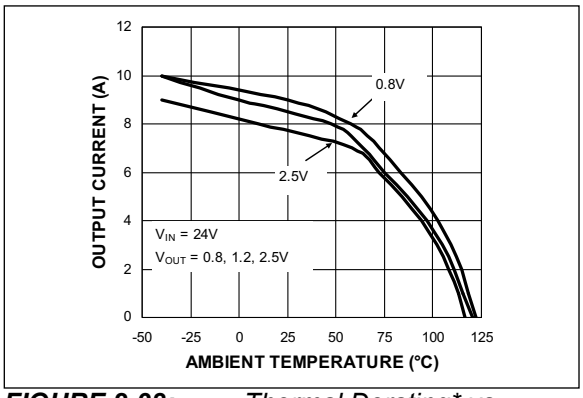



***FIGURE 2-38:*** *Thermal Derating* vs. Ambient Temperature.*

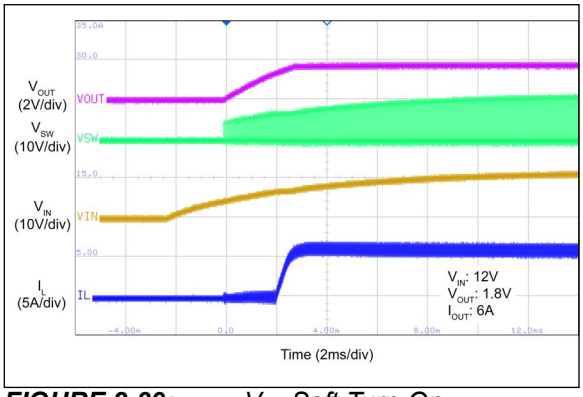



***FIGURE 2-39:*** *$V_{IN}$ Soft Turn-On.*

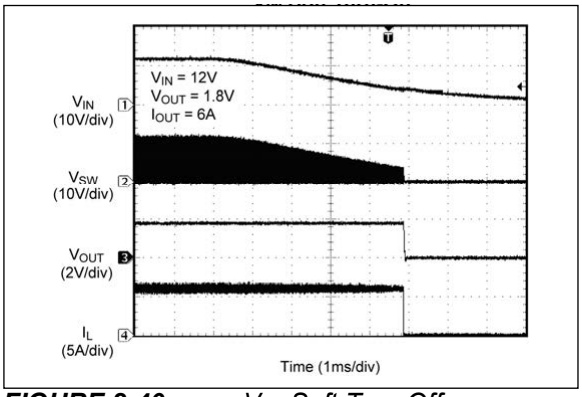



***FIGURE 2-40:*** *$V_{IN}$ Soft Turn-Off.*

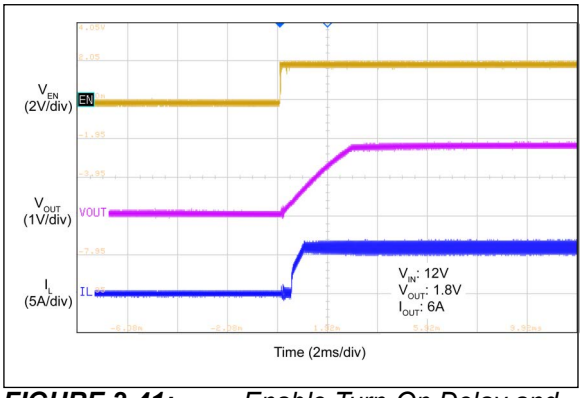



***FIGURE 2-41:*** *Enable Turn-On Delay and Rise Time.*

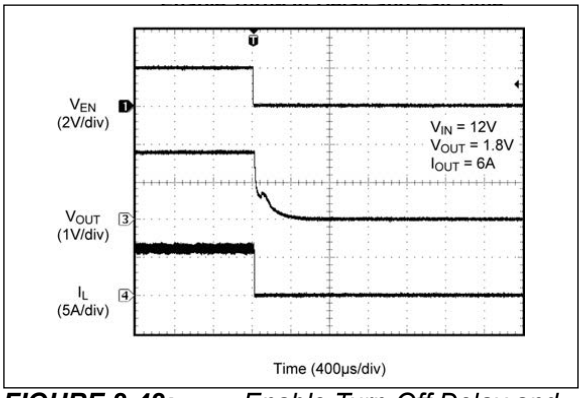



***FIGURE 2-42:*** *Enable Turn-Off Delay and Fall Time.*

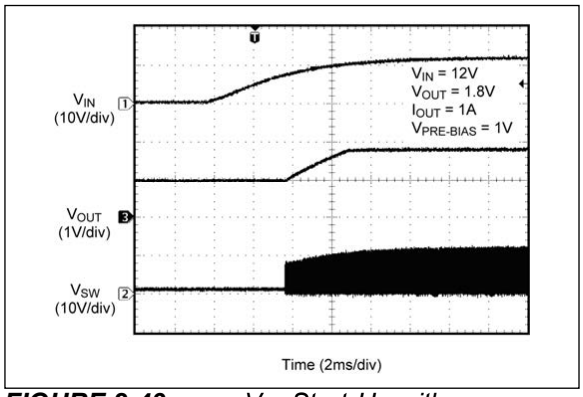



***FIGURE 2-43:*** *$V_{IN}$ Start-Up with Pre-Biased Output.*

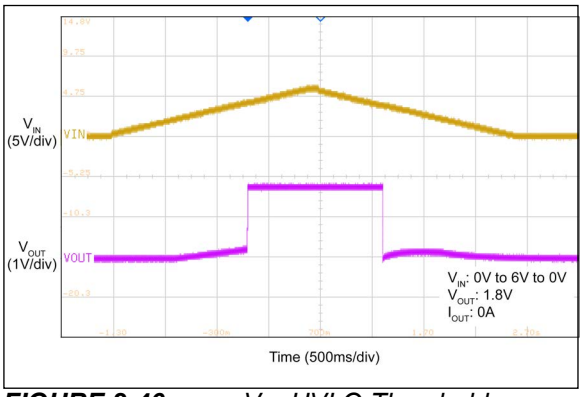



***FIGURE 2-46:*** *$V_{IN}$ UVLO Thresholds.*

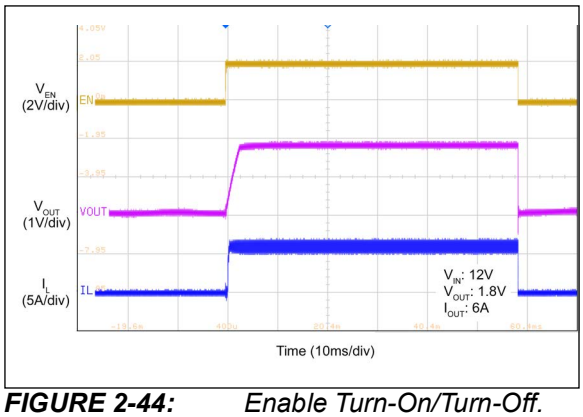



***FIGURE 2-44:*** *Enable Turn-On/Turn-Off.*

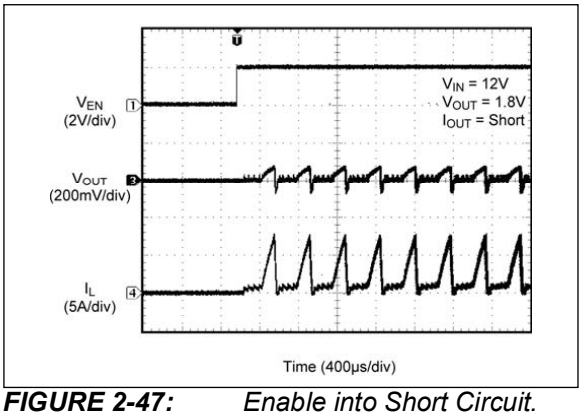



***FIGURE 2-47:*** *Enable into Short Circuit.*

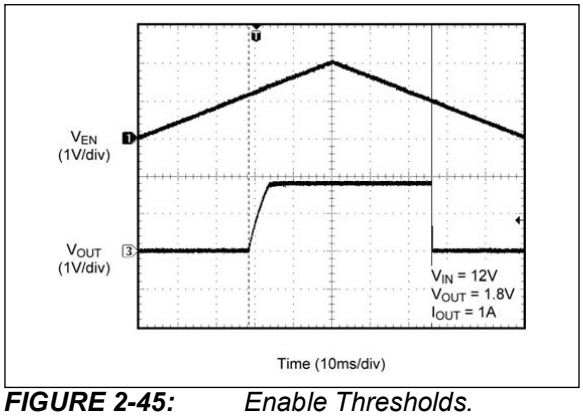



***FIGURE 2-45:*** *Enable Thresholds.*

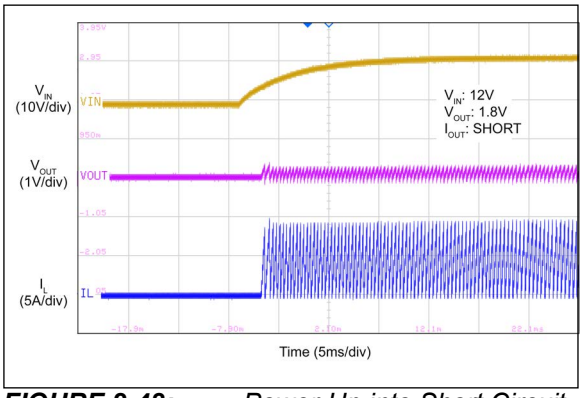



***FIGURE 2-48:*** *Power-Up into Short Circuit.*

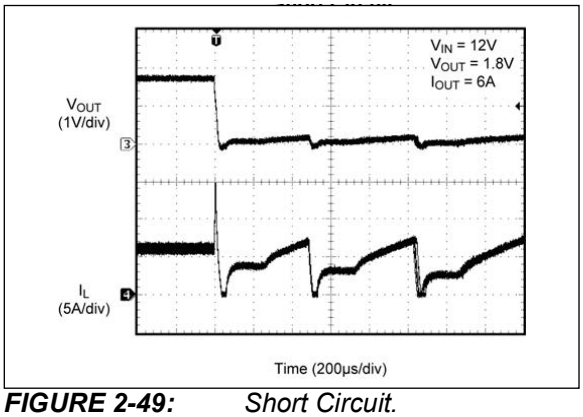



***FIGURE 2-49:*** *Short Circuit.*

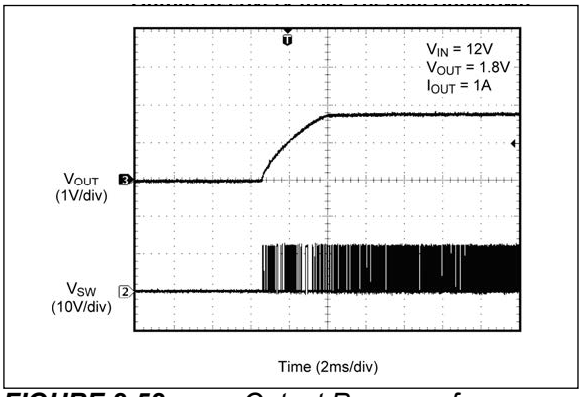



***FIGURE 2-52:*** *Output Recovery from Thermal Shutdown.*

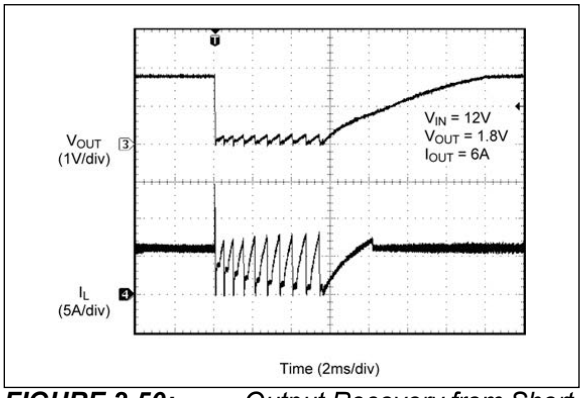



***FIGURE 2-50:*** *Output Recovery from Short Circuit.*

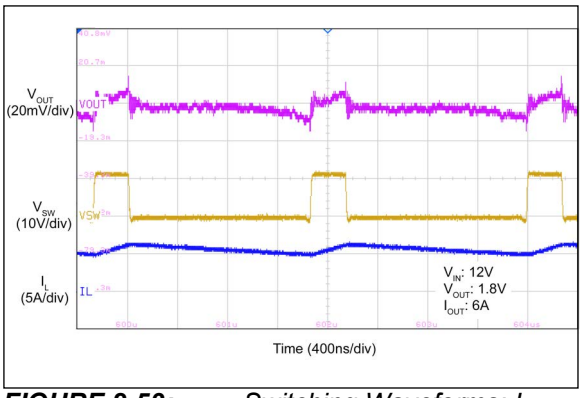



***FIGURE 2-53:*** *Switching Waveforms; $I_{OUT}$ = 6A.*

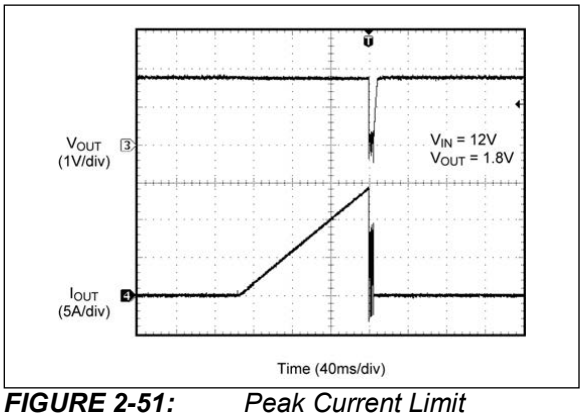



***FIGURE 2-51:*** *Peak Current Limit Threshold.*

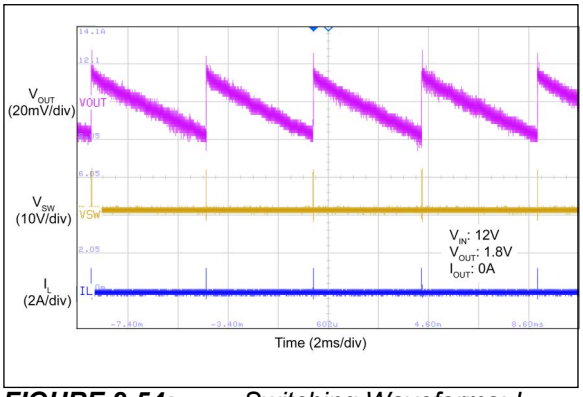



***FIGURE 2-54:*** *Switching Waveforms; $I_{OUT}$ = 0A.*

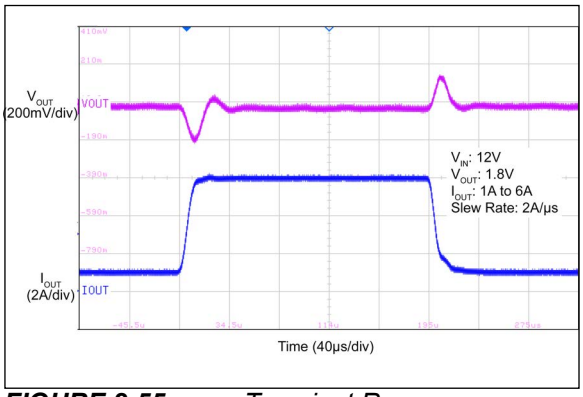



***FIGURE 2-55:*** *Transient Response.*

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | PVDD | 5V Internal Linear Regulator (Output): PVDD supply is the power MOSFET gate drive supply voltage and created by internal LDO from VIN. When $V_{IN}$ < 5.5V, PVDD should be tied to the PVIN pins. A 2.2 µF ceramic capacitor from the PVDD pin to PGND (Pin 2) must be placed next to the IC. |
| 3 | NC | No connect. |
| 4, 9, 10, 11, 12 | SW | Switch Node (Output): Internal connection for the high-side MOSFET source and low-side MOSFET drain. Due to the high speed switching on this pin, the SW pin should be routed away from sensitive nodes. |
| 2, 5, 6, 7, 8, 21 | PGND | Power Ground: PGND is the ground path for the MIC26603 buck converter power stage. The PGND pins connect to the low-side N-Channel internal MOSFET gate drive supply ground, the sources of the MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the Signal Ground (SGND) loop. |
| 13, 14, 15, 16, 17, 18, 19 | PVIN | High-Side N-internal MOSFET Drain Connection (Input): The PVIN operating voltage range is from 4.5V to 28V. Input capacitors between the PVIN pins and the Power Ground (PGND) are required and keep the connection short. |
| 20 | BST | Boost (Output): Bootstrapped voltage to the high-side N-channel MOSFET driver. A Schottky diode is connected between the PVDD pin and the BST pin. A boost capacitor of 0.1 µF is connected between the BST pin and the SW pin. Adding a small resistor at the BST pin can slow down the turn-on time of high-side N-Channel MOSFETs. |
| 22 | CS | Current Sense (Input): The CS pin senses current by monitoring the voltage across the low-side MOSFET during the OFF-time. The current sensing is necessary for short-circuit protection and zero current cross comparator. In order to sense the current accurately, connect the low-side MOSFET drain to SW using a Kelvin connection. The CS pin is also the high-side MOSFET's output driver return. |
| 23 | SGND | Signal Ground: SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer. See the PCB layout guidelines section for details. |
| 24 | FB | Feedback (Input): Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage. |
| 25 | PG | Power Good (Output): Open-Drain Output. The PG pin is externally tied with a resistor to VDD. A high output is asserted when $V_{OUT}$ > 92% of nominal. |
| 26 | EN | Enable (Input): A logic level control of the output. The EN pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the off state, supply current of the device is greatly reduced (typically 5 µA). The EN pin should not be left open. |
| 27 | VIN | Power Supply Voltage (Input): Requires bypass capacitor to SGND. |
| 28 | VDD | 5V Internal Linear Regulator (Output): VDD supply is the supply bus for the IC control circuit. $V_{DD}$ is created by internal LDO from VIN. When $V_{IN}$ < 5.5V, VDD should be tied to the PVIN pins. A 1.0 µF ceramic capacitor from the VDD pin to the SGND pins must be placed next to the IC. |

## 4.0 FUNCTIONAL DESCRIPTION

The MIC26603 is an adaptive ON-time, synchronous step-down, DC/DC regulator with an internal 5V linear regulator and a Power Good (PG) output. It is designed to operate over a wide input voltage range from 4.5V to 28V and provides a regulated output voltage at up to 6A of output current. An adaptive ON-time control scheme is employed in to obtain a constant switching frequency and to simplify the control compensation. Over-current protection is implemented without the use of an external sense resistor. The device includes an internal soft-start function that reduces the power supply input surge current at start-up by controlling the output voltage rise time.

### 4.1 Theory of Operation

The MIC26603 is able to operate in either continuous mode or discontinuous mode. The operating mode is determined by the output of the Zero Cross comparator (ZC) as shown in the Functional Block Diagram.

### 4.2 Continuous Mode

In continuous mode, the output voltage is sensed by the MIC26603 feedback pin (FB) via the voltage divider R1 and R2, and compared to a 0.8V reference voltage ($V_{REF}$) at the error comparator through a low gain transconductance ($g_m$) amplifier. If the feedback voltage decreases and the output of the $g_m$ amplifier is below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the Fixed $t_{ON}$ Estimation circuitry:

**EQUATION 4-1:**

$$t_{ON(estimated)} = \frac{V_{OUT}}{V_{IN} \times 600kHz}$$

Where:
$V_{OUT}$ = The output voltage.
$V_{IN}$ = The power stage input voltage.

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the $g_m$ amplifier is below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(MIN)}$, which is about 300 ns, the MIC26603 control logic will apply the $t_{OFF(MIN)}$ instead. $t_{OFF(MIN)}$ is required to maintain enough energy in the boost capacitor ($C_{BST}$) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 300 ns $t_{OFF(MIN)}$:

**EQUATION 4-2:**

$$D_{MAX} = \frac{t_S - t_{OFF(MIN)}}{t_S} = 1 - \frac{300ns}{t_S}$$

Where:
$t_S$ = 1/600 kHz = 1.66 µs

It is not recommended to use MIC26603 with an OFF-time close to $t_{OFF(MIN)}$ during steady-state operation. Also, as $V_{OUT}$ increases, the internal ripple injection will increase and reduce the line regulation performance. Therefore, the maximum output voltage of the MIC26603 should be limited to 5.5V and the maximum external ripple injection should be limited to 200 mV. Please refer to the Setting Output Voltage section for more details.

The actual ON-time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the $V_{DD}$ voltage. Also, the minimum $t_{ON}$ results in a lower switching frequency in high $V_{IN}$-to-$V_{OUT}$ applications, such as 24V to 1.0V. The minimum $t_{ON}$ measured on the MIC26603 evaluation board is about 100 ns. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios.

Figure 4-1 shows the MIC26603 control loop timing during steady-state operation. During steady-state, the $g_m$ amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON-time period. The ON-time is predetermined by the $t_{ON}$ estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when $V_{FB}$ falls below $V_{REF}$, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

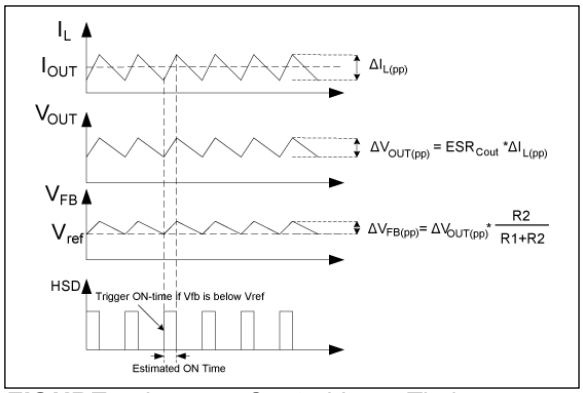



***FIGURE 4-1:*** *Control Loop Timing.*

Figure 4-2 shows the operation of the MIC26603 during a load transient. The output voltage drops due to the sudden load increase, which causes the $V_{FB}$ to be less than $V_{REF}$. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time [$t_{OFF(MIN)}$] is generated to charge $C_{BST}$ because the feedback voltage is still below $V_{REF}$. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC26603 converter.

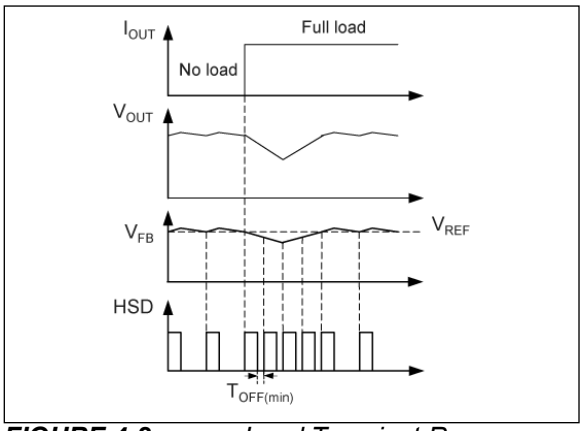



***FIGURE 4-2:*** *Load Transient Response.*

Unlike true current-mode control, the MIC26603 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. The MIC26603 control loop has the advantage of eliminating the need for slope compensation.

In order to meet the stability requirements, the MIC26603 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the $g_m$ amplifier and the error comparator. The recommended feedback voltage ripple is 20 mV~100 mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the $g_m$ amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to the Ripple Injection section for more details about the ripple injection technique.

## 4.3 Discontinuous Mode

In continuous mode, the inductor current is always greater than zero; however, at light loads the MIC26603 is able to force the inductor current to operate in discontinuous mode. Discontinuous mode is where the inductor current falls to zero, as indicated by trace ($I_L$) shown in Figure 4-3. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current. The MIC26603 wakes up and turns on the high-side MOSFET when the feedback voltage ($V_{FB}$) drops below 0.8V.

The MIC26603 has a zero crossing comparator that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If $V_{FB}$ >0.8V and the inductor current goes slightly negative, then the MIC26603 automatically powers down most of the IC circuitry and goes into a low-power mode.

Once the MIC26603 goes into discontinuous mode, both LSD and HSD are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and $V_{OUT}$ drops. If the drop of $V_{OUT}$ causes $V_{FB}$ to go below $V_{REF}$, then all the circuits will wake up into normal continuous mode. First, the bias currents of most circuits reduced during the discontinuous mode are restored, then a $t_{ON}$ pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 4-3 shows the control loop timing in discontinuous mode.

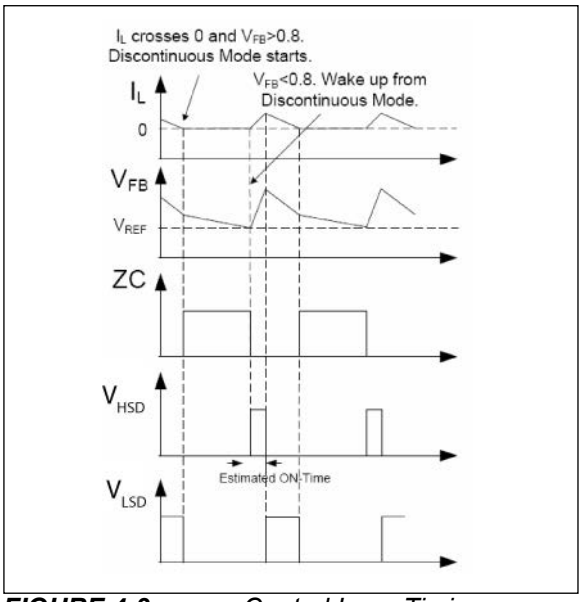



***FIGURE 4-3:*** *Control Loop Timing (Discontinuous Mode).*

During discontinuous mode, the bias current of most circuits are reduced. As a result, the total power supply current during discontinuous mode is only about 450 µA, allowing the MIC26603 to achieve high efficiency in light load applications.

## 4.4 $V_{DD}$ Regulator

The MIC26603 provides a 5V regulated output for input voltage $V_{IN}$ ranging from 5.5V to 28V. When $V_{IN}$ <5.5V, VDD should be tied to the PVIN pins to bypass the internal linear regulator.

## 4.5 Soft-Start

Soft-start reduces the power supply input surge current at start-up by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC26603 implements an internal digital soft-start by making the 0.8V reference voltage $V_{REF}$ ramp from 0 to 100% in about 5 ms with 9.7 mV steps. Therefore, the output voltage is controlled to increase slowly by a staircase $V_{FB}$ ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. $V_{DD}$ must be powered up at the same time or after $V_{IN}$ to make the soft-start function correctly.

## 4.6 Current Limit

The MIC26603 uses the $R_{DS(ON)}$ of the internal low-side power MOSFET to sense over-current conditions. This method will avoid adding cost, board space, and power losses taken by a discrete current sense resistor. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.

In each switching cycle of the MIC26603 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. If the inductor current is greater than 13A, then the MIC26603 turns off the high-side MOSFET and a soft-start sequence is triggered. This mode of operation is called “hiccup mode” and its purpose is to protect the downstream load in case of a hard short. The load current-limit threshold has a foldback characteristic related to the feedback voltage as shown in Figure 4-4.

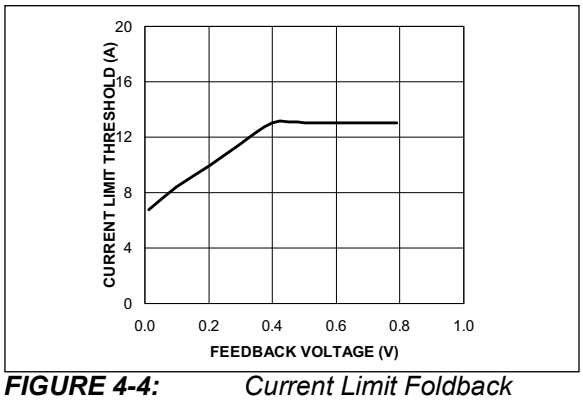



***FIGURE 4-4:*** *Current Limit Foldback Characteristic.*

## 4.7 Power Good (PG)

The Power Good (PG) pin is an open-drain output that indicates logic high when the output is nominally 92% of its steady state voltage. A pull-up resistor of more than 10 kΩ should be connected from PG to VDD.

## 4.8 MOSFET Gate Drive

The Functional Block Diagram shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and $C_{BST}$. This circuit supplies energy to the high-side drive circuit. Capacitor $C_{BST}$ is charged, while the low-side MOSFET is on, and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from $C_{BST}$ is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately $V_{IN}$. Diode D1 is reverse-biased and $C_{BST}$ floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10 mA, so a 0.1 µF to 1 µF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle (i.e. ΔBST = 10 mA × 1.67 µs/0.1 µF = 167 mV). When the low-side MOSFET is turned back on, $C_{BST}$ is recharged through D1. A small resistor $R_G$, which is in series with $C_{BST}$, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the $V_{DD}$ supply voltage. The nominal low-side gate drive voltage is $V_{DD}$ and the nominal high-side gate drive voltage is approximately $V_{DD} - V_{DIODE}$, where $V_{DIODE}$ is the voltage drop across D1. An approximate 30 ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

# 5.0 APPLICATION INFORMATION

## 5.1 Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and, therefore, a larger and more expensive inductor. A good compromise between size, loss, and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated in Equation 5-1:

**EQUATION 5-1:**

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times 20\% \times I_{OUT(MAX)}}$$

Where:
$f_{SW}$ = Switching frequency, 600 kHz
20% = Ratio of AC ripple current to DC output current
$V_{IN(MAX)}$ = Maximum power stage input voltage

The peak-to-peak inductor current ripple is:

**EQUATION 5-2:**

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

**EQUATION 5-3:**

$$I_{L(PK)} = I_{OUT(MAX)} + 0.5 \times \Delta I_{L(PP)}$$

The RMS inductor current is used to calculate the $I^2R$ losses in the inductor.

**EQUATION 5-4:**

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{\Delta I_{L(PP)}^2}{12}}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high-frequency operation of the MIC26603 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used, but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized, although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 5-5:

**EQUATION 5-5:**

$$P_{IND(CU)} = I_{L(RMS)}^2 \times R_{WIND}$$

The resistance of the copper wire, $R_{WIND}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

**EQUATION 5-6:**

$$P_{WIND(HT)} = R_{WIND(20C)} \times (1 + 0.0042 \times (T_H - T_{20C}))$$

Where:
$T_H$ = Temperature of the wire under full load
$T_{20C}$ = Ambient temperature
$R_{WIND(20C)}$ = Room temperature winding resistance (usually specified by the manufacturer)

## 5.2 Output Capacitor Selection

The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are tantalum, low-ESR aluminum electrolytic, OS-CON, and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view.

The maximum value of ESR is calculated using the following formula:

**EQUATION 5-7:**

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:
$\Delta V_{OUT(PP)}$ = Peak-to-peak output voltage ripple
$\Delta I_{L(PP)}$ = Peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 5-8:

**EQUATION 5-8:**

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{COUT}\right)^2}$$

Where:
$C_{OUT}$ = Output capacitance value
$f_{SW}$ = Switching frequency

As described in the Theory of Operation section, the MIC26603 requires at least 20 mV peak-to-peak ripple at the FB pin to make the $g_m$ amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough feedback voltage ripple. Please refer to the Ripple Injection section for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 5-9:

**EQUATION 5-9:**

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is calculated using the following equation:

**EQUATION 5-10:**

$$P_{DISS(COUT)} = I_{COUT(RMS)}^2 \times ESR_{COUT}$$

## 5.3 Input Capacitor Selection

The input capacitor for the power stage input $V_{IN}$ should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

**EQUATION 5-11:**

$$\Delta V_{IN} = I_{L(PK)} \times ESR_{CIN}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

**EQUATION 5-12:**

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is:

**EQUATION 5-13:**

$$P_{DISS(CIN)} = I_{CIN(RMS)}^2 \times ESR_{CIN}$$

## 5.4 Ripple Injection

The $V_{FB}$ ripple required for proper operation of the MIC26603 $g_m$ amplifier and error comparator is 20 mV to 100 mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as a 1V, the output voltage ripple is only 10 mV to 20 mV, and the feedback voltage ripple is less than 20 mV. If the feedback voltage ripple is so small that the $g_m$ amplifier and error comparator can't sense it, then the MIC26603 will lose control and the output voltage will not be regulated. In order to have some amount of $V_{FB}$ ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback voltage due to the large ESR of the output capacitors.

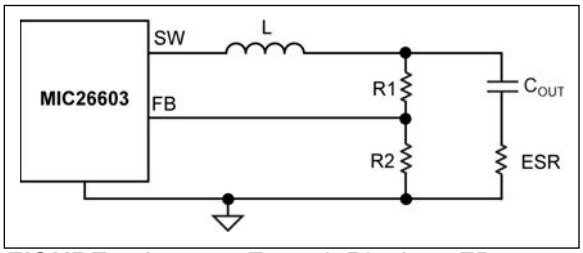



***FIGURE 5-1:*** *Enough Ripple at FB.*

As shown in Figure 5-1, the converter is stable without any ripple injection. The feedback voltage ripple is:

**EQUATION 5-14:**

$$\Delta V_{FB(PP)} = \frac{R2}{R1 + R2} \times ESR_{COUT} \times \Delta I_{L(PP)}$$

Where:
$\Delta I_{L(PP)}$ = Peak-to-peak value of the inductor current ripple

2. Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

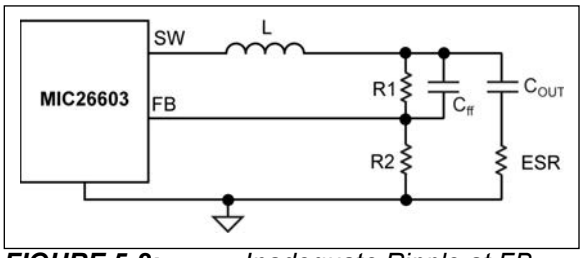



***FIGURE 5-2:*** *Inadequate Ripple at FB.*

The output voltage ripple is fed into the FB pin through a feed-forward capacitor, $C_{ff}$ in this situation, as shown in Figure 5-2. The typical $C_{ff}$ value is between 1 nF and 100 nF. With the feed-forward capacitor, the feedback voltage ripple is very close to the output voltage ripple:

**EQUATION 5-15:**

$$\Delta V_{FB(PP)} \approx ESR \times \Delta I_{L(PP)}$$

3. Virtually no ripple at the FB pin voltage due to the very low ESR of the output capacitors.

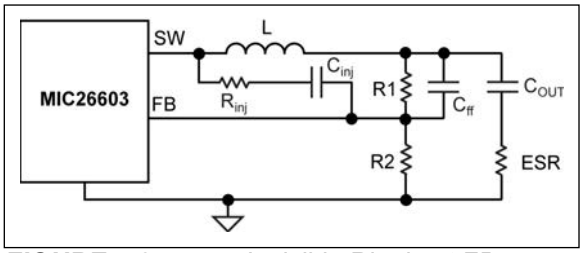



***FIGURE 5-3:*** *Invisible Ripple at FB.*

In this situation, the output voltage ripple is less than 20 mV. Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor $R_{inj}$ and a capacitor $C_{inj}$, as shown in Figure 5-3. The injected ripple is:

**EQUATION 5-16:**

$$\Delta V_{FB(PP)} = V_{IN} \times K_{DIV} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

$$K_{DIV} = \frac{R1//R2}{R_{INJ} + R1//R2}$$

Where:
$V_{IN}$ = Power stage input voltage
D = Duty cycle
$f_{SW}$ = Switching frequency
$\tau = (R1//R2//R_{INJ}) \times C_{ff}$

In Equation 5-16, it is assumed that the time constant associated with $C_{ff}$ must be much greater than the switching period:

**EQUATION 5-17:**

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} \ll 1$$

If the voltage divider resistors R1 and R2 are in the kΩ range, a $C_{ff}$ of 1 nF to 100 nF can easily satisfy the large time constant requirements. Also, a 100 nF injection capacitor $C_{inj}$ is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

***Step 1.*** Select $C_{ff}$ to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice for $C_{ff}$ is 1 nF to 100 nF if R1 and R2 are in kΩ range.

***Step 2.*** Select $R_{inj}$ according to the expected feedback voltage ripple using Equation 5-18:

**EQUATION 5-18:**

$$K_{DIV} = \frac{\Delta V_{FB(PP)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1 - D)}$$

Then the value of $R_{inj}$ is obtained as:

**EQUATION 5-19:**

$$R_{inj} = (R1//R2) \times \left(\frac{1}{K_{DIV}} - 1\right)$$

***Step 3.*** Select $C_{inj}$ as 100 nF, which could be considered as short for a wide range of the frequencies.

## 5.5 Setting Output Voltage

The MIC26603 requires two resistors to set the output voltage as shown in Figure 5-4.

The output voltage is determined by the following equation:

**EQUATION 5-20:**

$$V_{OUT} = V_{IN} \times \left(1 + \frac{R1}{R2}\right)$$

Where:
$V_{FB}$ = 0.8V

A typical value of R1 can be between 3 kΩ and 10 kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using:

**EQUATION 5-21:**

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}}$$

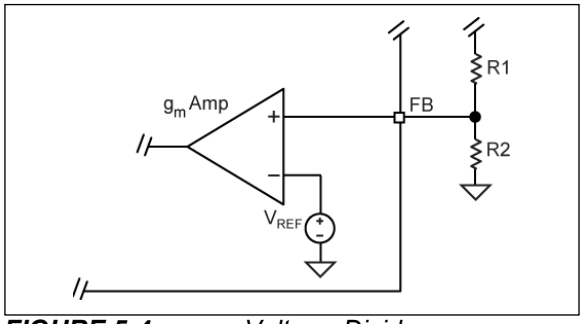



***FIGURE 5-4:*** *Voltage-Divider Configuration.*

In addition to the external ripple injection added at the FB pin, internal ripple injection is added at the inverting input of the comparator inside the MIC26603, as shown in Figure 5-5. The inverting input voltage $V_{INJ}$ is clamped to 1.2V. As $V_{OUT}$ is increased, the swing of $V_{INJ}$ will be clamped. The clamped $V_{INJ}$ reduces the line regulation because it is reflected as a DC error on the FB terminal. Therefore, the maximum output voltage of the MIC26603 should be limited to 5.5V to avoid this problem.

It is recommended to use a bleeder resistor of 33 kΩ at VOUT for better regulation at output voltages below 1V.

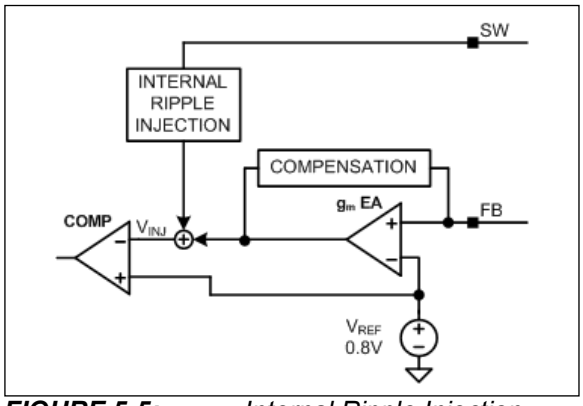



***FIGURE 5-5:*** *Internal Ripple Injection.*

## 5.6 Thermal Measurements

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, which results in a lower case temperature measurement.

Two methods of reliable temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher then (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, a IR thermometer from Optris has a 1 mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

## 6.0 PCB LAYOUT GUIDELINES

PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths. To minimize EMI and output noise, follow these layout recommendations.

The guidelines below should be followed to ensure proper operation of the MIC26603 regulator.

### 6.1 IC

- A 2.2 µF ceramic capacitor, which is connected to the PVDD pin, must be located right at the IC. The PVDD pin is very noise sensitive and placement of the capacitor is critical. Use wide traces to connect to the PVDD and PGND pins.
- A 1.0 µF ceramic capacitor must be placed right between VDD and the signal ground SGND. The SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer.
- Place the IC close to the point-of-load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

### 6.2 Input Capacitor

- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PVIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the overvoltage spike seen on the input supply with power is suddenly applied.

### 6.3 Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The CS pin should be connected directly to the SW pin to accurate sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough air flow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the IC.

### 6.4 Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

### 6.5 Optional RC Snubber

- Place the RC snubber on either side of the board and as close to the SW pin as possible.

## 7.0 EVALUATION BOARD SCHEMATIC

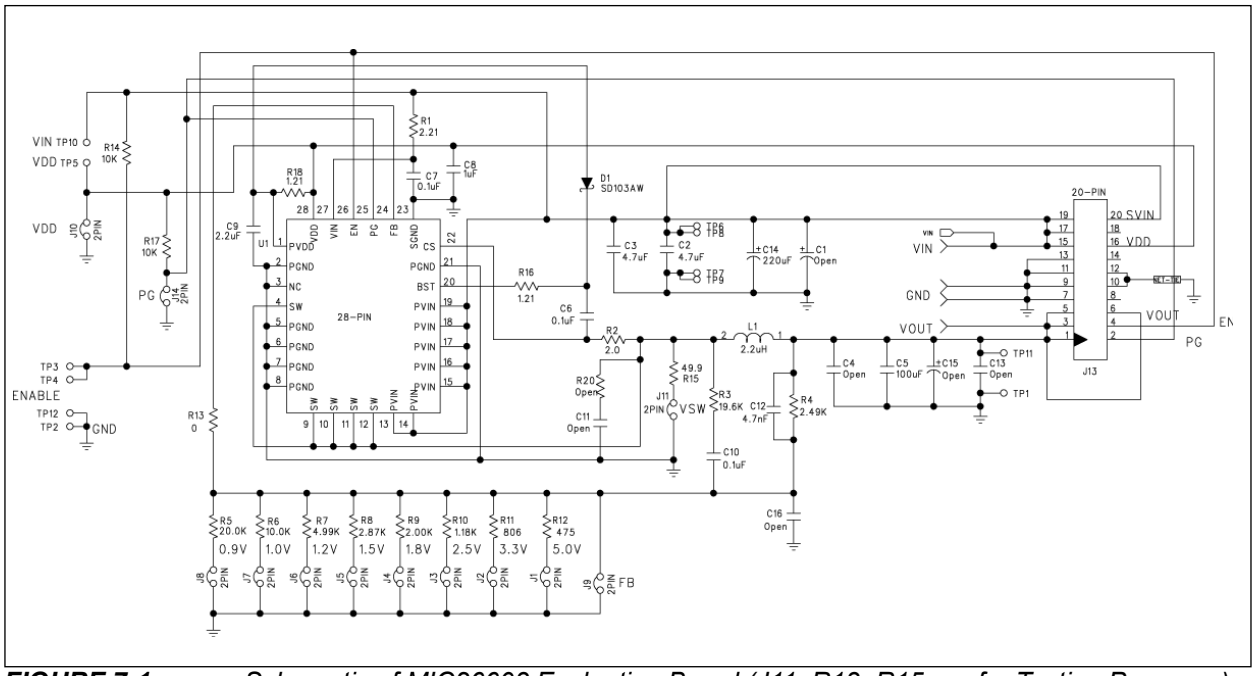



***FIGURE 7-1:*** *Schematic of MIC26603 Evaluation Board (J11, R13, R15 are for Testing Purposes).*

**TABLE 7-1: BILL OF MATERIALS**

| Item | Part Number | Manufacturer | Description | Qty. |
|---|---|---|---|---|
| C1 | Open | | | |
| C2, C3 | 12105C475KAZ2A | AVX | 4.7 µF Ceramic Capacitor, X7R, Size 1210, 50V | 2 |
| | GRM32ER71H475KA88L | Murata | | |
| | C3225X7R1H475K | TDK | | |
| C4, C13, C15 | Open | | | |
| C5 | 12106D107MAT2A | AVX | 100 µF Ceramic Capacitor, X5R, Size 1210, 6.3V | 1 |
| | GRM32ER60J107ME20L | Murata | | |
| | C3225X5R0J107M | TDK | | |
| C6, C7, C10 | 06035C104KAT2A | AVX | 0.1 µF Ceramic Capacitor, X7R, Size 0603, 50V | 3 |
| | GRM188R71H104KA93D | Murata | | |
| | C1608X7R1H104K | TDK | | |
| C8 | 0603ZC105KAT2A | AVX | 1.0 µF Ceramic Capacitor, X7R, Size 0603, 10V | 1 |
| | GRM188R71A105KA61D | Murata | | |
| | C1608X7R1A105K | TDK | | |
| C9 | 0603ZD225KAT2A | AVX | 2.2 µF Ceramic Capacitor, X5R, Size 0603, 10V | 1 |
| | GRM188R61A225KE34D | Murata | | |
| | C1608X5R1A225K | TDK | | |
| C12 | 06035C472KAZ2A | AVX | 4.7 nF Ceramic Capacitor, X7R, Size 0603, 50V | 1 |
| | GRM188R71H472K | Murata | | |
| | C1608X7R1H472K | TDK | | |
| C14 | B41851F7227M | EPCOS | 220 µF Aluminum Capacitor, 35V | 1 |
| C11, C16 | Open | | | |

**TABLE 7-1: BILL OF MATERIALS (CONTINUED)**

| Item | Part Number | Manufacturer | Description | Qty. |
|---|---|---|---|---|
| D1 | SD103AWS | MCC | 40V, 350 mA, Schottky Diode, SOD323 | 1 |
| | SD103AWS-7 | Diodes Inc. | | |
| | SD103AWS | Vishay | | |
| L1 | HCF1305-2R2-R | Cooper Bussman | 2.2 µH Inductor, 15A Saturation Current | 1 |
| R1 | CRCW06032R21FKEA | Vishay Dale | 2.21Ω Resistor, Size 0603, 1% | 1 |
| R2 | CRCW06032R00FKEA | Vishay Dale | 2.00Ω Resistor, Size 0603, 1% | 1 |
| R3 | CRCW060319K6FKEA | Vishay Dale | 19.6 kΩ Resistor, Size 0603, 1% | 1 |
| R4 | CRCW06032K49FKEA | Vishay Dale | 2.49 kΩ Resistor, Size 0603, 1% | 1 |
| R5 | CRCW060320K0FKEA | Vishay Dale | 20.0 kΩ Resistor, Size 0603, 1% | 1 |
| R6, R14, R17 | CRCW060310K0FKEA | Vishay Dale | 10.0 kΩ Resistor, Size 0603, 1% | 3 |
| R7 | CRCW06034K99FKEA | Vishay Dale | 4.99 kΩ Resistor, Size 0603, 1% | 1 |
| R8 | CRCW06032K87FKEA | Vishay Dale | 2.87 kΩ Resistor, Size 0603, 1% | 1 |
| R9 | CRCW06032K006FKEA | Vishay Dale | 2.00 kΩ Resistor, Size 0603, 1% | 1 |
| R10 | CRCW06031K18FKEA | Vishay Dale | 1.18 kΩ Resistor, Size 0603, 1% | 1 |
| R11 | CRCW0603806RFKEA | Vishay Dale | 806Ω Resistor, Size 0603, 1% | 1 |
| R12 | CRCW0603475RFKEA | Vishay Dale | 475Ω Resistor, Size 0603, 1% | 1 |
| R13 | CRCW06030000FKEA | Vishay Dale | 0Ω Resistor, Size 0603, 5% | 1 |
| R15 | CRCW060349R9FKEA | Vishay Dale | 49.9Ω Resistor, Size 0603, 1% | 1 |
| R16, R18 | CRCW06031R21FKEA | Vishay Dale | 1.21Ω Resistor, Size 0603, 1% | 2 |
| R20 | Open | | | |
| U1 | MIC26603YJL | Microchip | 28V, 6A HyperLight Load® Synchronous DC/DC Buck Regulator | 1 |

## 8.0 PCB LAYOUT RECOMMENDATIONS

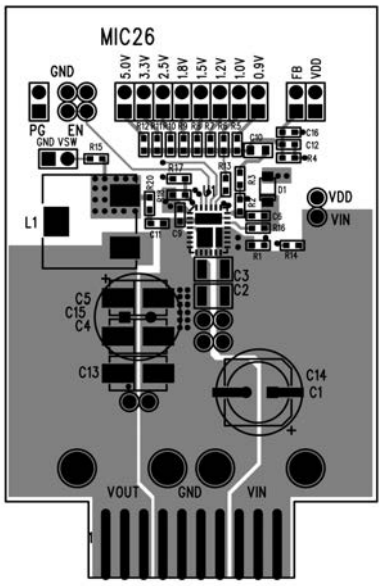



***FIGURE 8-1:*** *Evaluation Board Top Layer.*

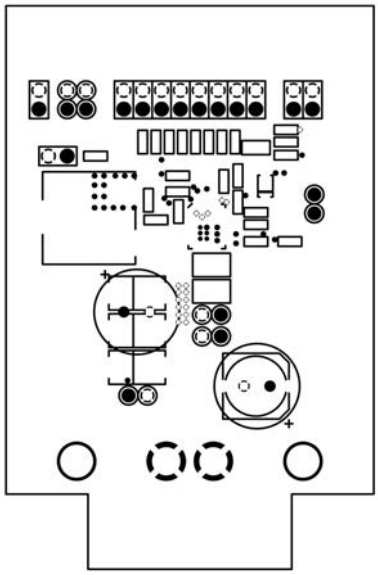


***FIGURE 8-2:*** *Evaluation Board Mid-Layer 1 (Ground Plane).*

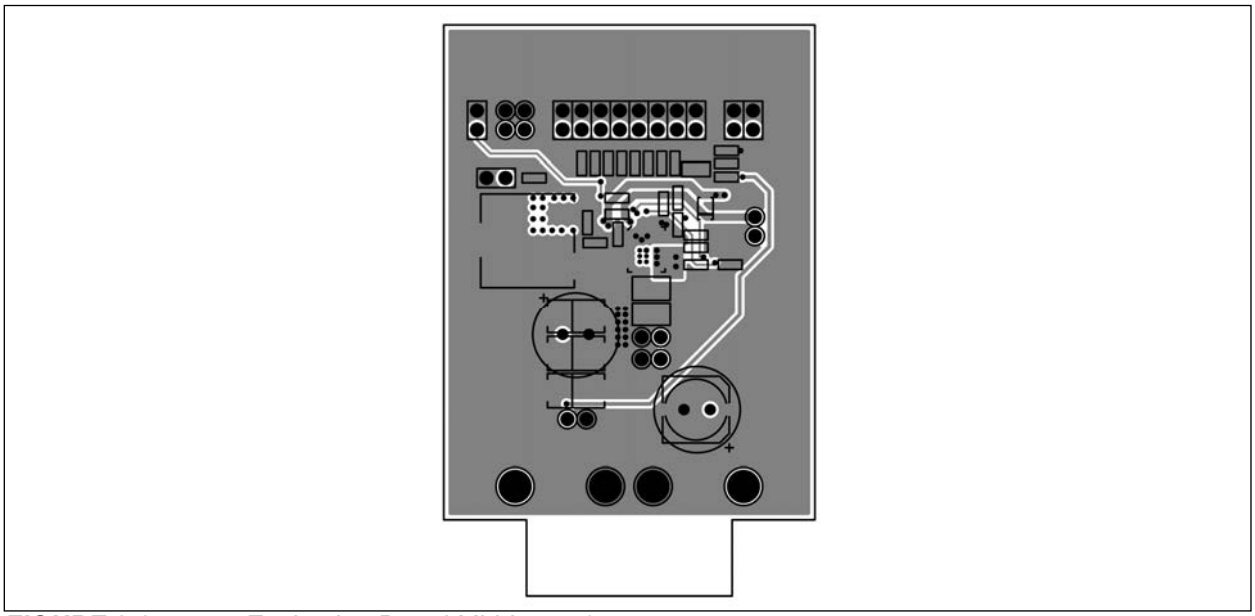


***FIGURE 8-3:*** *Evaluation Board Mid-Layer 2.*

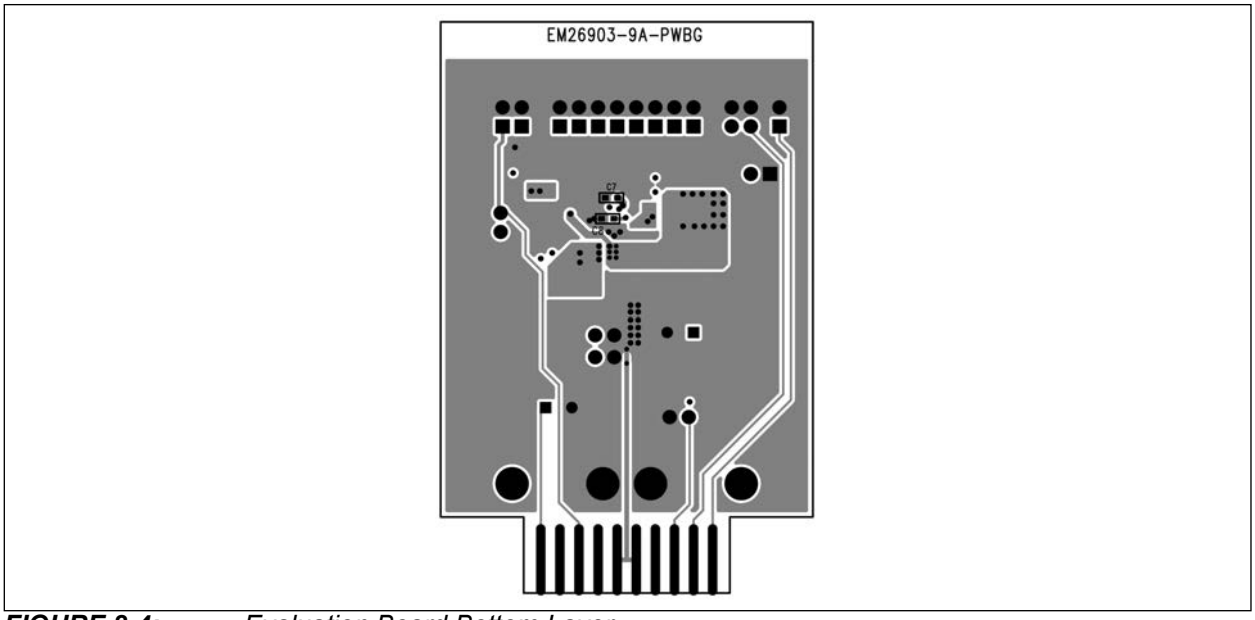
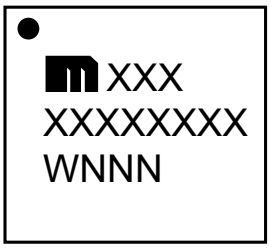



***FIGURE 8-4:*** *Evaluation Board Bottom Layer.*

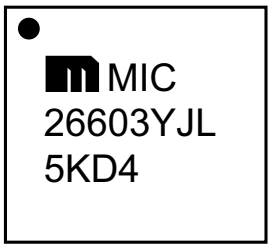
## 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information

28-Lead VQFN*




Example

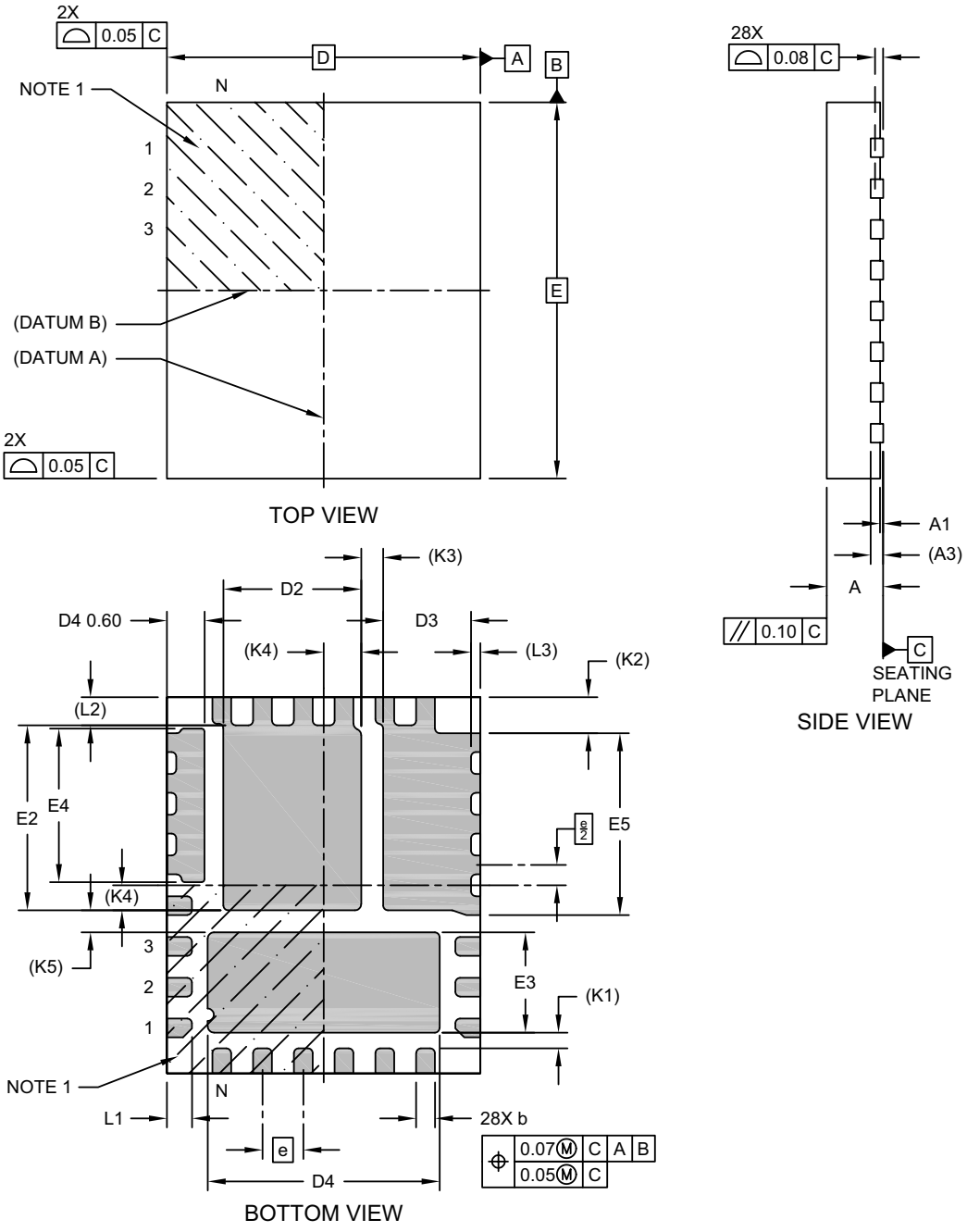



| | | |
|---|---|---|
| **Legend:** | XX...X | Product code or customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
| | ●, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle mark). |
| **Note**: | | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. |
| | | Underbar (_) and/or Overbar (¯) symbol may not be to scale. |

**Note:** If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

**28-Lead Very Thin Plastic Quad Flat, No Lead Package (PKA) - 5x6x0.9 mm Body [VQFN] With Multiple Exposed Pads and Fused Terminals; Micrel Legacy QFN56-28LD-PL-1**

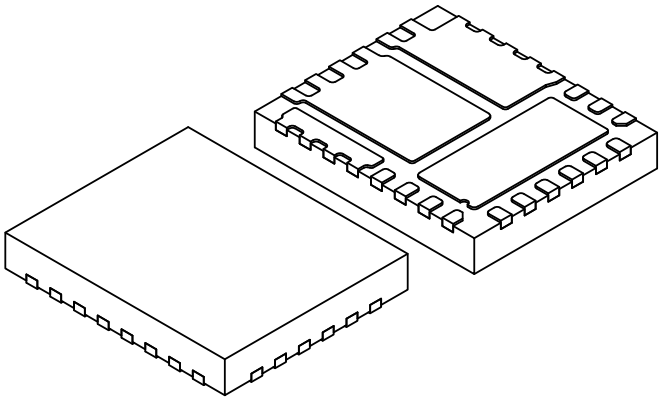
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-1120 Rev A Sheet 1 of 2

**28-Lead Very Thin Plastic Quad Flat, No Lead Package (PKA) - 5x6x0.9 mm Body [VQFN] With Multiple Exposed Pads and Fused Terminals; Micrel Legacy QFN56-28LD-PL-1**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 28 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.00 | 0.02 | 0.05 |
| Standoff | A1 | 0.80 | 0.85 | 0.85 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 5.00 BSC | |
| Exposed Pad Length | D2 | 2.15 | 2.20 | 2.25 |
| Exposed Pad Length | D3 | 1.35 | 1.40 | 1.45 |
| Exposed Pad Length | D4 | 3.65 | 3.70 | 3.75 |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 2.90 | 2.95 | 3.00 |
| Exposed Pad Width | E3 | 1.575 | 1.60 | 1.625 |
| Exposed Pad Width | E4 | 2.40 | 2.45 | 2.50 |
| Exposed Pad Width | E5 | 2.85 | 2.90 | 2.95 |
| Terminal Width | b | 0.25 | 0.30 | 0.35 |
| Terminal Length | L1 | 0.35 | 0.40 | 0.45 |
| Terminal Length | L2 | | 0.45 REF | |
| Terminal Length | L3 | | 0.15 REF | |
| Terminal to Exposed Pad | K1 | | 0.25 REF | |
| Body Edge to Exposed Pad | K2 | | 0.575 REF | |
| Exposed Pad to Exposed Pad | K3 | | 0.035 REF | |
| Exposed Pad Offset | K4 | | 0.40 REF | |
| Exposed Pad to Exposed Pad | K5 | | 0.35 REF | |

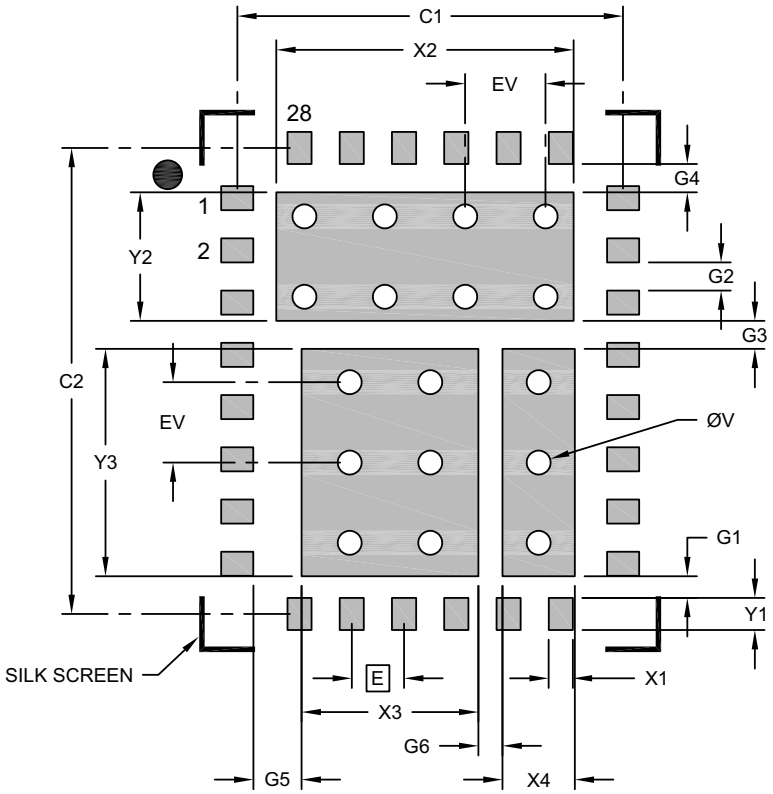
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1120 Rev A Sheet 2 of 2

**28-Lead Very Thin Plastic Quad Flat, No Lead Package (PKA) - 5x6x0.9 mm Body [VQFN] With Multiple Exposed Pads and Fused Terminals; Micrel Legacy QFN56-28LD-PL-1**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Center Pad Width | X2 | | | 3.70 |
| Center Pad Width | X3 | | | 2.20 |
| Center Pad Width | X4 | | | 0.90 |
| Center Pad Length | Y2 | | | 1.60 |
| Center Pad Length | Y3 | | | 2.83 |
| Contact Pad Width | X1 | | | 0.30 |
| Contact Pad Length | Y1 | | | 0.40 |
| Contact Pad Spacing | C1 | | 4.80 | |

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pad Spacing | C2 | | 5.80 | |
| Contact Pad to Center Pad | G1 | 0.12 | | |
| Contact Pad to Contact Pad | G2 | 0.35 | | |
| Center Pad to Center Pad | G3 | 0.35 | | |
| Contact Pad to Center Pad | G4 | 0.35 | | |
| Contact Pad to Center Pad | G5 | 0.60 | | |
| Center Pad to Center Pad | G6 | 0.13 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3120 Rev A

# APPENDIX A: REVISION HISTORY

## Revision A (May 2025)

- Converted Micrel document MIC26603 to Microchip data sheet DS20007012A.
- Minor text changes throughout.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| Part Number | X | XX | -XX |
|---|---|---|---|
| Device | Temp. Range | Package | Media Type |

| | | | |
|---|---|---|---|
| **Device:** | MIC26603: | | 28V, 6A HyperLight Load® Synchronous DC/DC Buck Regulator |
| **Temperature Range:** | Y | = | –40°C to +125°C |
| **Package:** | JL | = | 28-Lead 6 mm x 5 mm VQFN |
| **Media Type:** | TR | = | 1,000/Reel |

**Examples:**

a) MIC26603YLJ-TR:

MIC26603, –40°C to +125°C Temp. Range, 28-Lead VQFN, 1,000/Reel

**Note:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**NOTES:**

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