PIC32MZ W1 MCU and WFI32 Module with Wi-Fi® and Hardware-Based Security Accelerator Errata

PIC32MZ W1 and WFI32 Errata Sheet

Overview

The PIC32MZ W1 family of devices conform functionally to the current device data sheet, except for the anomalies described in this document.

The silicon/module issues discussed in the following pages are for silicon/module revisions with the device and revision IDs listed in the following table. The silicon/module issues are summarized in Table 1-1.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the Output window.

Note: If you are unable to extract the silicon revision level, visit support.microchip.com or contact your local Microchip sales office.

The following table details the device and revision ID values for the PIC32MZ W1 silicon.

Table 1. Device and Revision Details

Part Number	Device ID	Revision ID for Silicon Revision			
		A0	A1	B0	C0
PIC32MZ1025W104132	0x08C03053	NA	0x01	NA	NA
	0x0A403053	NA	NA	0x00	0x01
PIC32MZ2051W104132	0x0A603053	0x00	NA	NA	NA
WFI32E01	0x08C03053	NA	0x01	NA	NA
	0x0A403053	NA	NA	0x00	0x01
WFI32E02	0x0A403053	NA	NA	NA	0x01
WFI32E03	0x0A603053	0x00	NA	NA	NA

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1. Silicon Errata Summary

Table 1-1. Silicon Errata Summary

Module	Feature	Issue Summary	Affected Revisions			
			A0	A1	B0	C0
2.1. CAN	Interrupt	The CAN Wake Interrupt Flag bit, WAKIF, is set even when the CAN module is disabled.	X	X	X	X
2.2. CAN	CAN	The CAN FIFO abort operation during transmission does not set the TXABAT bit in FIFOCON register.	X	X	X	X
2.3. I2C	I^2C Client	The 7-bit address that matches the 10-bit upper address value (111_10xx_xxx) is not accepted regardless of the STRICT bit setting.	X	X	X	X
2.4. ICSP	TDO	The TDO pin becomes an output and toggles while programming on any ICSP™ PGECx/PGEDx pair.	—	X	X	X
2.5. SPI	Block Transmission	The SRMT bit incorrectly indicates the end of transmission for the last PBCLK.	X	X	X	X
2.6. Timer1	Asynchronous Counter	Timer1 in Asynchronous External Counter mode does not reflect the first count from an external T1CLK input.	X	X	X	X
2.7. Timer1	TMR1Register	The TMR1 register of Timer1 in Asynchronous mode remains at the initial set value for five external clock pulses after wake-up from Sleep mode.	X	X	X	X
2.8. Timer1	Asynchronous Mode	Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.	X	X	X	X
2.9. UART	TX/RX Interrupt	A UART Transmit Interrupt (UTXI- SEL[1:0] bits (UxSTA[15:14]) = `'0b00`) is generated and asserted while the transmit buffer contains at least one empty space and the UART Receiver Interrupt Flag bit (URXISEL[1:0] bits (UxSTA[7:6]) = `'0b00`) is asserted while the receive buffer is not empty and non-functional.	X	X	X	X
2.10. UART	TX Interrupt	A UART Transmit Interrupt (UTXI- SEL[1:0] bits = `'0b01`) is generated but does not remain asserted after all of the characters are transmitted.	X	X	X	X
2.11. UART	TX Interrupt	A UART Transmit Interrupt (UTXI- SEL[1:0]bits = `'0b10`) is generated but does not remain asserted while the transmit buffer is empty.	X	X	X	X
2.12. UART	RX Interrupt	The UART Receive Interrupt flag (URXISEL[1:0] bits = `'0b01`) is asserted only when the receive buffer equals one-half full and not when the receive buffer is greater than one-half full.	X	X	X	X
2.13. UART	RX Interrupt	The UART Receive Interrupt Flag bit (URXISEL[1:0] bits = `'0b10`) is asserted only when the receive buffer equals three-quarters full and not when the receive buffer is greater than three-quarters full.	X	X	X	X
2.14. Watchdog Timer (WDT)	WDT	WDT does not reset the CPU within the expected time period across the voltage and temperature ranges.	—	X	—	—
2.15. Wi-Fi	Data Transmission	Degraded TX EVM is observed during low Wi-Fi® traffic with a long idle duration between packet transmission.	—	X	—	—
2.16. USB	Compliance	SE0 output of the USB peripheral may not meet compliance requirements.	—	X	X	—
2.17. Power	Low-power mode	Excess leakage current observed in some devices under certain voltage and temperature ranges when the USB controller is disabled and not connected.	—	X	X	—
2.18. Wi-Fi	Wi-Fi	Potential issue where the DMA interface module can latch the sub-MSDU length for an A-MSDU from the header as a frame is received but before the FCS is validated, resulting in the possibility of subsequent valid frames being dropped.	—	X	—	—
2.19. PTG	PTGSWT	The hardware does not clear the PTGSWT bit in case of back-to-back execution of the `SWTRGE` command.	X	X	X	X

.....continued

Module	Feature	Issue Summary	Affected Revisions			
			A0	A1	B0	C0
2.20. PTG	PTGSTRT	PTGSTRT is not cleared when PTGON = 0.	X	X	X	X
2.21. CAN-FD	CAN Source Clock	Certain features of the CAN-FD cannot operate optimally if the UPB Clock's speed is equal to or less than that of the CAN clock.	X	X	X	X
2.22. NVM	NVM	PIC32MZ2051W104132/WFI32E03 may generate an invalid instruction exception while performing run-time self erase and self program operations.	X	—	—	—
2.23. NVM	NVM	PIC32MZ1025W104132/WFI32E01/WFI32E02 may require additional recovery time after Deep Sleep mode or require time after NVM program/erase to next read operation.	—	X	X	X
2.24. Power	Low-power mode	The system does not enter the Sleep mode or Deep Sleep mode or Extreme Deep Sleep mode when the Flash power-down (NVMCON2.SLEEP = 0) bit is disabled and the system is operating at less than 35 MHz.	X	—	—	—
2.25. Capacitive Voltage Divider (CVD) Controller	CVD Event	An invalid CVD event can occur while the FIFO counter increments.	X	X	X	X

2. Silicon Errata Issues

The following errata issues apply to the PIC32MZ W1 family of devices.

Notes:

1. Cells with an 'X' indicate the issue is present in this revision of the silicon.
2. Cells with a dash ('—') indicate the issue does not exist for this revision of the silicon.
3. Blank cells indicate the issue is corrected or does not exist in this revision of the silicon.

Note: Traditional Inter-Integrated Circuit (I^2C) and Serial Peripheral Interface (SPI) documentation uses the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client", respectively.

2.1 CAN

Clear the WAKIF (CxINT[14]) bit prior to enabling the CAN peripheral.

Work Around

During the CAN initialization and before enabling the CAN peripheral, clear the WAKIF bit in the user code and this work around is implemented in Harmony.

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.2 CAN

The CAN FIFO aborts the operation during transmission without setting the TXABAT bit in the FIFOCON register.

Work Around

None

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.3 I^2C

The7-bit address that matches the 10-bit upper address value (111_10xx_xxx) is not accepted regardless of the STRICT bit setting.

Work Around

None

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.4 ICSP

The TDO pin becomes an output and toggles while programming on any ICSP™ PGECx/ PGEDx pair.

Work Around

None

Affected Silicon Revisions

A0	A1	B0	C0
—	X	X	X

2.5 SPI

The SRMT bit may incorrectly indicate that the transmission is done right before the last block of a transmission is shifted out to the SPI pins. However, this does not affect the Transmit Buffer Empty Interrupt (STXISEL = 0).

Work Around

Use the interrupt indication bit to determine the end of transmission.

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.6 Timer1

In Asynchronous External Counter mode, TCS bit (T1CON[1] = 1), TSYNC bit (T1CON[2] = 0) and TECS[1:0] (T1CON[9:8] = '0b01)), the Timer1 register (TMR1) does not reflect the first count from an external T1CLK input.

Work Around

Always add 1 to the Timer1 count value to reflect the first count from an external T1CLK input.

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.7 Timer1

In Asynchronous External Counter mode, (TCS bit (T1CON[1] = 1), TSYNC bit (T1CON[2] = 0) and TECS[1:0] (T1CON[9:8] = '0b01)), the Timer1 register (TMR1) remains at the initial set value for five external clock pulses after wake-up from Sleep mode.

Work Around

None

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.8 Timer1

Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.

Work Around

Set the Timer1 period, PR1, to a value greater than 1.

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.9 UART

A UART Transmit Interrupt (UTXISEL[1:0] bits (UxSTA[15:14]) = '0b00) is generated and asserted while the transmit buffer contains at least one empty space and the UART Receiver Interrupt Flag

bit (URXISEL[1:0] bits (UxSTA[7:6]) = '0b00) is asserted while the receive buffer is not empty and non-functional.

Work Around

None

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.10 UART

A UART Transmit Interrupt (UTXISEL[1:0] bits = '0b01) is generated but does not remain asserted even after all of the characters were transmitted. When the IFSx bit is cleared by the user, it does not remain asserted even after all characters were transmitted. This behavior, compounded with finite interrupt latency, can create a race condition amongst subsequent TX interrupts.

Work Around

To avoid the race condition, clear the UARTx IFSx flag before writing a new value to the TX Buffer, UxTXREG, in the ISR.

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.11 UART

The UART Transmit UTXISEL[1:0] bits = '0b10 Interrupt is generated but does not remain asserted while the transmit buffer is empty. When the IFS bit is cleared by the user, it does not remain asserted even while the transmit buffer is empty. This behavior, compounded with finite interrupt latency, can create a race condition amongst subsequent TX interrupts.

Work Around

To avoid the race condition, clear the UARTx IFS flag before writing a new value to the TX Buffer, UxTXREG, in the ISR.

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.12 UART

The UART Receive Interrupt Flag (URXISEL[1:0] bits = '0b01) is asserted only when the receive buffer equals one-half full and not when the receive buffer is greater than one-half full.

Work Around

Before exiting the UART RX ISR, make sure all of the contents of the RX buffer were read by reading the contents of the RX buffer in the ISR until the URXDA bit (UxSTA[0]) is cleared and this work around is implemented in Harmony.

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.13 UART

The UART Receive Interrupt Flag bit (URXISEL[1:0] bits = '0b10) is asserted only when the receive buffer equals three-quarters full and not when the receive buffer is greater than three-quarters full.

Work Around

Before exiting the UART RX ISR, make sure the entire contents of the RX buffer were read by reading the contents of the RX buffer in the ISR until the URXDA bit (UxSTA[10]) is cleared and this work around is implemented in Harmony.

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.14 Watchdog Timer (WDT)

When using the LPRC as a WDT source prescalar, the WDT does not cause a CPU Reset within the time period expected by the WDTPS configurations. The following table provides details about the WDT and prescaler values with their corresponding expected Reset period and mean values.

Table 2-1. WDTPS Configuration

PS Value	Input Clock	Expected Time Period	Mean Value
0xA	LRPC	1s	1.026s
0xB	LPRC	2s	2.025s
0xA	LRPC	1s	1.439s
0xB	LPRC	2s	2.357s

Work Around

None

Affected Silicon Revisions

A0	A1	B0	C0
—	X	—	—

2.15 Wi-Fi®

Degraded TX EVM is observed during low Wi-Fi traffic with a long idle duration between packet transmission due to rapid transient surges in current consumption. The magnitude of EVM degradation varies from device to device. The range of degradation can cause EVM specification failure for MCS6 and MCS7 data rates. Operations like low-frequency ping will show this issue. There is no impact on throughput performance.

Work Around

None

Affected Silicon Revisions

A0	A1	B0	C0
—	X	—	—

2.16 USB

The SE0 output state of the USB peripheral while operating in host or device mode may not meet the USB 2.0 electrical standards and, hence, may cause the USB peripheral to fail the USB Eye pattern test.

Work Around

None

Affected Silicon Revisions

A0	A1	B0	C0
—	X	X	—

2.17 Power

Excess leakage current observed in some devices under certain voltage and temperature ranges when the USB controller is disabled and not connected.

Work Around

To achieve optimal power-down current in Deep Sleep and Extreme Deep Sleep states, the USB D+ and D- signals must not be left floating. The signals can be tied to GROUND if the USB peripheral is not used.

If the USB peripheral is used, the user can mitigate this issue by connecting two GPIO pins available on the PIC32MZ W1 device to the D+ and D- USB pins. These GPIO pins must be in the High Impedance state during normal USB operation. When the USB peripheral is disabled or the PIC32MZ W1 device enters the Deep Sleep state, program these GPIO pins as outputs driving 0V. Configure the GPIO pins as open drain input and disable internal pull-up/pull-down to change to the High Impedance state. The recommendation is to add a 0Ω resistor between the GPIO pins and the D+/D- lines to prevent design changes with the future versions of the silicon.

Affected Silicon Revisions

A0	A1	B0	C0
—	X	X	—

2.18 Wi-Fi®

Potential issue whereby the DMA interface module can latch the sub-MSDU length for an A-MSDU from the header as a frame is received but before the FCS is validated. Because of this, an incorrect length could be latched for a corrupted received frame (A-MSDU or not). When latched, this length is updated only on the reception of a valid A-MSDU.

This can cause the receiver to lock up. This issue is fixed in the B0 silicon revision by adding logic to clear the latched sub-MSDU length field.

Work Around

None

Affected Silicon Revisions

A0	A1	B0	C0
—	X	—	—

2.19 PTG

The hardware does not clear the PTGSWT bit when back-to-back execution of the `SWTRGE` command occurs.

Work Around

To clear the PTGSWT bit while executing the `SWTRGE` command consecutively, the user application must use any other command in between two `SWTRGE` commands. The recommendation is to use the `NOP` command.

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.20 PTG

The hardware does not clear the PTGSTRT when PTGON is set to '0'. The user can see the unexpected behavior after enabling the PTG if the PTGSTRT is not cleared when PTG is disabled.

Work Around

To avoid this issue, clear the PTGSTRT bit before clearing the PTGON bit.

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.21 CAN-FD

If the UPB clock is less than or equal to the CAN clock, it is going to have impact on some functionalities of CAN-FD.

Work Around

The CAN source clock must be less than the CAN UPB/peripheral clock (PB2_CLK). Select ETHPLL as the CAN source clock and configure CFGCON0.CANFDDIV such that the CAN source clock (ETHPLL) is less than PB2_CLK(CAN UPB/peripheral clock).

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

2.22 NVM

PIC32MZ2051W104132/WFI32E03 can generate an invalid instruction exception while performing run-time self-erase and self-program operations.

Work Around

Use MPLAB® Harmony v3 (CSP v3.18.4 or higher) or implement NVM write and erase routines such that NVM unlock, NVM write control and NVM wait operations are performed while executing from RAM. The steps required to be performed in NVM are: disable all the interrupts, set the NVMCON WREN bit, then execute the code from RAM. (Write the unlock key sequence, then set the NVMCON WR bit to start the operation. Then, wait until the operation completes. The NVMCON WR bit will be cleared when the operation completes.) Then, enable all the interrupts. For more details, refer to this Knowledge Base Article.

Affected Silicon Revisions

A0	A1	B0	C0
X	—	—	—

2.23 NVM

PIC32MZ1025W104132/WFI32E01/WFI32E02 may require additional recovery time after Deep Sleep mode or requires time after NVM program/erase to next read operation.

Work Around

Enable Flash ECC. The Flash ECC will correct one-bit errors and detect 2-bit errors. When a 2-bit error is detected, the CPU will generate a BUS EXCEPTION error. The MPLAB® Harmony V3 (CSP v3.18.4 or higher) general exception auto-generated code will handle this condition.

Affected Silicon Revisions

A0	A1	B0	C0
—	X	X	X

2.24 Power

The system does not enter the Sleep mode or Deep Sleep mode or Extreme Deep Sleep mode when the Flash power-down (NVMCON2.SLEEP = 0) bit is disabled when the system is operating at less than 35 MHz.

Work Around

Enable the Flash power-down (NVMCON2.SLEEP = 1) bit to enter into the Flash Sleep mode or Deep Sleep mode or Extreme Deep Sleep mode when the system is running at less than 35 MHz.

Affected Silicon Revisions

A0	A1	B0	C0
X	—	—	—

2.25 Capacitive Voltage Divider (CVD) Controller

An invalid CVD event can occur while the FIFO counter increments.

Work Around

After receiving a CVD interrupt, check whether the status of CVDSTAT[FIFOCNT] is greater than or equal to CVDCON[FIFOTH] to confirm that it is a true interrupt.

Affected Silicon Revisions

A0	A1	B0	C0
X	X	X	X

3. Data Sheet Clarifications

The following clarifications and additional information are applicable to the latest version of the *PIC32MZ W1 MCU and WFI32 Module with Wi-Fi® and Hardware- Based Security Accelerator Data Sheet* (DS70005425):

- The Low Power mode information updated in sections “35.0 Power Management Unit (PMU)”, “36.0 Power-saving Features” and “41.0 Electrical Specifications” are relevant for the B0 silicon version and later.
- Convert the external 5V VBUS signal to a 3.3V level using a series resistor before interfacing with the WFI32E01, WFI32E02 or WFI32E03 modules. For more details, refer to the *PIC32MZ W1 MCU and WFI32 Module with Wi-Fi® and Hardware-Based Security Accelerator Data Sheet* (DS70005425), “3.2.6 USB”, Figure 3-11.

4. Document Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Document Revision History

Revision	Date	Section	Description
J	06/2024	Overview	Updated Table 1 with the following: • Part number PIC32MZ1025W104132 • Part number PIC32MZ2051W104132
		1. Silicon Errata Summary	Updated Table 1-1 with the following: • Updated affected revisions column
		2. Silicon Errata Issues	• Added silicon errata issues 2.24. Power and 2.25. Capacitive Voltage Divider (CVD) Controller • Added A0 column for all the Affected Silicon Revisions table
		3. Data Sheet Clarifications	Updated section
H	03/2024	Overview	Updated Table 1 with the following: • PIC32MZ2051W104 silicon • WFI32E01 Module • WFI32E02 Module • WFI32E03 Module
		1. Silicon Errata Summary	Updated Table 1-1 with silicon issues (2.20. PTG, 2.21. CAN-FD, 2.22. NVM, 2.23. NVM and 2.24. Power)
		2. Silicon Errata Issues	Added silicon errata issues 2.20. PTG, 2.21. CAN-FD, 2.22. NVM, 2.23. NVM and 2.24. Power
G	04/2023	Document	Updated the Errata with C0 release information
		1. Silicon Errata Summary	Updated Table 1-1
		2. Silicon Errata Issues	Updated
		3. Data Sheet Clarifications	Updated
F	05/2022	1. Silicon Errata Summary	Updated Table 1-1 with silicon issues (2.18. Wi-Fi)
		2. Silicon Errata Issues	Added new silicon errata issue 2.18. Wi-Fi
E	01/2022	2. Silicon Errata Issues	Updated Workaround of 2.17. Power errata
		3. Data Sheet Clarifications	Added new section
D	11/2021	2. Silicon Errata Issues	Added 2.17. Power errata and its details
C	10/2021	Document	• Updated the Errata with B0 release information • Design/implementation related limitations are now available in the data sheet • Updated with the new terminologies: “For more details, see the following note.”
		2. Silicon Errata Issues	Added 2.16. USB errata and its details
B	01/2021	1. Silicon Errata Summary	Updated Table 1-1 with silicon issues (2.15. Wi-Fi)
		2. Silicon Errata Issues	Added new silicon errata issue 2.15. Wi-Fi
A	09/2020	Document	Initial release

Note: *Microchip is aware that some terminologies used in the technical documents and existing software codes of this product are outdated and unsuitable. This document may use these new terminologies, which may ormay not reflect on the source codes, software GUIs, and the documents referenced within this document. The following table shows the relevant terminology changes made in this document.*

Table 4-2. Terminology Related Changes

Old Terminology	New Terminology	Description
I^2C Slave	I^2C Client	Table 1-1 is updated with new terminology.

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