16-Bit PWM Migration

Migration from 16-Bit PWM to 16-Bit PWM with Compare

Overview

Author: Ward Brown, Microchip Technology Inc.

The 16-bit Pulse-Width Modulator (PWM) with the Compare feature is the next generation of 16-bit PWM that is available on selected 8-bit devices. A features comparison between this PWM and the legacy 16-bit PWM is shown in Table 1 below. Although the table may indicate that a feature is available in both PWM types, there may be significant differences in how that feature is enabled in each. The emphasis in this document is on how the new 16-bit PWM with compare can be configured to perform an equivalent mode of the legacy 16-bit PWM, details of which are given in the sections titled by the feature name.

In those cases where a feature in the legacy 16-bit PWM module is not supported, suggestions about combining the new PWM with other peripherals to perform those functions are given. Features new to this PWM that are not supported in the legacy PWM are beyond the scope of this document. Refer to the family data sheet for more information.

Table 1. Feature Comparison Between 16-Bit and 16-Bit with Compare PWMs

Feature	Legacy 16-Bit PWM	New 16-Bit PWM w/Compare
Left Aligned	●	●
Right Aligned	●	●
Center Aligned	●	●
Variable Aligned	●	●
Pulsed Compare		●
Set on Compare	●	
Toggled Compare	●	●
Push-Pull		●
Output Polarity	●	●
Outputs	1	2 per slice, up to 4 slices
Timer	Integrated	Integrated
Clock Sources	3	20 (1)
Clock Prescale	divide by 2^n where n=0 to 7	divide by n where n=1 to 255
Synchronous Reset	●	●
Asynchronous Reset		●
Reset Sources	Other PWMs only	13 (1)
External Load Trigger	Other PWMs only	15 (1)
Period Interrupt	●	●

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Feature	**Legacy 16-Bit PWM**	**New 16-Bit PWM w/Compare**
Duty Cycle Interrupt	●	●
Offset Interrupt	●	
Phase Interrupt	●	●

Note:
1. Selection register can accommodate up to 255 sources.

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1. Timer and Period

The period and timer functions are identical between the legacy and new PWM modules. However, the 16-bit timer value is not accessible in the new PWM, whereas it is accessible in the legacy PWM.

2. Output Polarity

The polarity of each output can be selected independently. The number of outputs in the new PWM depend on the number of slices whereas the legacy PWM has only one output per PWM.

3. Alignment Modes

The new PWM has specific Left, Right, and Center Alignment modes, whereas the legacy PWM specifies only the Center Alignment mode. In general, the legacy PWM used two registers (Phase and Duty Cycle) to define the active PWM period for modes other than Center Aligned. The new PWM uses only one parameter register (for each output) to define the active PWM period for each of the alignment modes.

For the sake of comparison between the legacy PWM and new PWM, only one parameter register corresponding to one of the PWM outputs will be mentioned in the following alignment sections. The other PWM outputs and corresponding parameter registers of the new PWM operate identically.

Details for realizing the equivalent legacy versus new PWM operation for each of the specific alignment modes is given in the following sections. The legacy PWM is assumed to be set to operate in the independent run mode (OFM = `b’00`) for these examples.

3.1 Left Aligned

In Standard mode (MODE = `b’00`) the legacy PWM output goes active when the timer value matches the Phase register (PWMxPH), and then goes inactive when the timer value matches the Duty Cycle register (PWMxDC). Left aligned operation in the legacy PWM is realized by setting the Phase register to zero.

In Left Aligned mode (MODE = `b’000`) the new PWM output always goes active at the beginning of the period and then goes inactive when the timer value matches the parameter register (PWMxSaP1).

3.2 Right Aligned

Right Aligned mode in the new PWM is simply a matter of selecting the Right Aligned mode (MODE = `b’001`). The PWM output starts inactive then goes active the Duty Cycle time (set by PWMxSaP1) before the end of the period.

An equivalent legacy PWM operation is accomplished in the Standard mode (MODE = `b’00`). Set the Phase register (PWMxPH) to the value obtained by subtracting the desired Duty Cycle from the PWM period (PWMxPR), and set the Duty Cycle register (PWMxDC) to the same value as the period register (PWMxPR).

3.3 Center Aligned

Setting the legacy PWM to Center Aligned mode (MODE = `b’11`) is equivalent to setting the new PWM to Center Aligned mode (MODE = `b’010`). The legacy Duty Cycle value (PWMxDC) is equivalent to the new PWM parameter value (PWMxSaP1). The legacy PWM Phase value (PWMxPH) has no effect in this mode.

3.4 Variable Aligned

The new PWM Variable Aligned mode (MODE = `b’011`) is equivalent to the legacy PWM Standard mode (MODE = `b’00`). In this mode, the new PWM Parameter 1 register (PWMxSaP1) determines when the output goes active. This is equivalent to the legacy PWM Phase register (PWMxPH). The new PWM Parameter 2 register (PWMxSaP2) determines when the output goes inactive. This is equivalent to the legacy PWM Duty Cycle register (PWMxDC).

The new PWM has effectively only one output in Variable Aligned mode because both parameter registers are used to determine the active period and both outputs have the same waveform.

4. Compare Modes

The legacy PWM has two compare modes: Set on Match and Toggle on Match. The new PWM has Pulse on Match and Toggle on Match modes. Comparisons of each to follow.

4.1 Set On Compare

The legacy PWM Set on Match mode (MODE = `b'01`) sets the PWM output active when the timer value matches the Phase value (PWMxPH). The output stays active until the OUT bit is cleared.

The new PWM in Pulsed Compare mode (MODE = `b'100`) pulses the output active for one prescaled PWM_clk period when the timer matches the parameter value (PWMxSaP1). An equivalent set-on-match operation can be achieved by triggering a CLC configured as an S-R latch or one of the Flip-Flop modes with the PWM pulsed output. Specific CLC configuration setups are beyond the scope of this document. Clearing the CLC latch after a set event is equivalent to clearing the OUT bit of the legacy PWM.

4.2 Toggle On Compare

The legacy PWM Toggle mode (MODE = `b'10`) and new PWM Toggled Compare mode (MODE = `b'101`) are equivalent. The legacy PWM output toggles when the timer matches the Phase value (PWMxPH). The new PWM output toggles when the timer matches the parameter value (PWMxSaP1).

5. Offset Modes

The legacy PWM has several modes of operation in which the output can be suspended or synchronized with one of the other PWMs. These Offset modes work in conjunction with the Compare, Standard, and Center Aligned modes. Although there are no modes of operation in the new PWM that correlate directly with the legacy PWM Offset modes, in many cases an equivalent operation can be achieved with the reset and trigger sources available in the new PWM, sometimes with the help of one or more CLCs as described in the following sections.

5.1 Independent Run

The legacy PWM operates as a free running PWM in Independent Run mode (OFM = `b'00`) with no synchronizing or Reset events. The equivalent operation in the new PWM is achieved by disabling the Reset sources (PWMxERS = `0x00`) and reload sources (PWMxLDS = `0x00`).

5.2 Slave Run With Synchronous Start

In the legacy PWM Slave Run with Synchronous Start mode (OFM = `b'01`), the slave PWM operation does not start until triggered to do so by a master PWM offset event. The offset determines the phase relationship of the master to the slave PWM outputs.

In the new PWM, an equivalent phase alignment between two outputs can be accomplished by using the Variable Alignment mode (MODE = `b'011`) and enabling multiple PWM modules simultaneously with the mirrored enables in the PWMEN register. The variable alignment duty cycle start parameter (PWMxSaP1) value determines the phase offset and the stop parameter (PWMxSaP2) value determines the duty cycle.

Another possible method is to keep the PWMs held in Reset with the external Reset sources (PWMxERS) then release the Resets at the desired offset times. For example, use the CLCs configured as latches as the Reset sources and then release the latches by means of a timer or the other PWMs.

5.3 Slave One-Shot with Synchronous Start

The legacy PWM can output a single duty cycle pulse in the Slave One-Shot mode. In this mode, the slave's output is triggered by the offset event of a master PWM.

A single duty cycle pulse can be achieved with the new PWM with two CLCs configured to receive the trigger event. One of the two CLCs drives the PWM external Reset source. Refer to the figures below.

CLC1 accepts the trigger and CLC2 releases the PWM Reset signal to allow a single PWM cycle. The trigger event is an edge so the duration of the trigger level is irrelevant. A third CLC can be added for zero latency. Note that the PWM period must be greater than one period of the CLC clock for the first method, or greater than two periods of the CLC clock for the zero latency method.

Figure 5-1. PWM Single-Shot Trigger

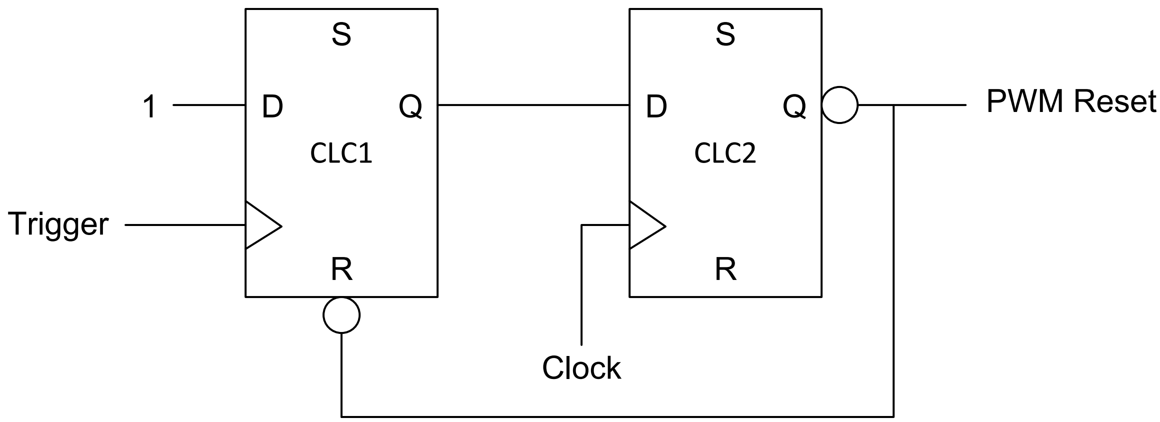
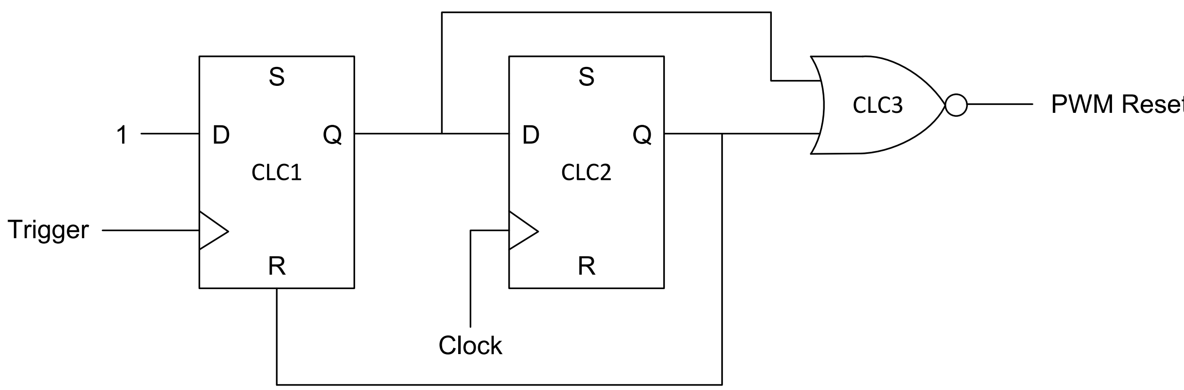


Figure 5-2. PWM Zero Latency Single-Shot Trigger



5.4 Slave Run with Sync Start and Timer Reset

The legacy PWM can maintain the phase relationship between a master and slave PWM with the Synchronous Start and Timer Reset mode. The slave PWM maintains the same phase offset from the master PWM as the master's period varies.

The new PWM can emulate this mode by using the second output of the master PWM to reset the slave PWM. The following configurations are a guide to set this up:

- Master PWM configuration
  - Left Aligned mode (MODE = `b'000`)
  - P1 set to the desired duty cycle
  - P2 set to 1 to generate the Reset signal for the slave PWM
  - Period set to the desired value. As this is changed, the slave will follow.
- Slave PWM configuration
  - Variable Aligned mode (MODE = `b'011`)
  - P1 set to the desired offset from master PWM minus one prescaled timer period to compensate for the Reset pulse width
  - P2 set to the desired duty cycle. The PWM output will be active for P2-P1 prescaled clock cycles
  - ERS set to select the master PWM P2 output
  - ERSNOW = `1` for immediate response to the Reset signal
  - Period set to be greater than the longest expected PWM period

Master and slave are started synchronously by enabling both simultaneously with the PWMEN register.

6. Reload Triggers

In the legacy PWM and new PWM, changes to the period value and values for events that occur when the timer reaches that value are double-buffered. The buffer values always take effect at the end of the period in which a trigger flag has been set. The legacy PWM can either set the trigger flag immediately by software or wait for one of the other PWMs to set the flag. The new PWM has multiple load trigger sources in addition to the other PWMs and can also use the PWMLOAD register to set the trigger flag by software for all PWMs simultaneously. Any combination of load triggering can be setup in the new PWM with the independently programmable load trigger source selections.

7. Interrupts

The legacy PWM has four separate interrupts, one for each of the timer match events: Period, Phase, Duty Cycle, and Offset. These four interrupts are ORd together into a single interrupt flag in one of the PIR registers.

The new PWM has two separate interrupts in one of the PIR registers: One for the period interrupt (PWMxPIF) and the other (PWMxIF) is the OR of all the parameter interrupts.

The period interrupt has a postscaler counter whereas the parameter interrupts do not. Each slice has two parameter registers for which each has an interrupt flag. There can be up to four slices in one PWM, meaning that the summary interrupt can be the OR of up to eight parameter interrupts. The following sections discuss ways the new PWM interrupts can perform the same as the legacy PWM interrupts.

7.1 Period Interrupt

The legacy PWM period interrupt is ORd together with the other timer event interrupts, whereas the new PWM period interrupt is independent from the parameter interrupts and has a postscaler counter. When the postscaler count (PWMxPIPOS) is zero then the new and legacy PWM period interrupts are essentially the same. The main difference is that the new PWM period interrupt (PWMxPIF) is enabled in one of the PIE registers and needs to be cleared in the corresponding PIR register, whereas the legacy period interrupt is enabled in the Summary Enable register (PWMxINTE) and cleared in the Summary Interrupt register (PWMxINTF).

7.2 Phase Interrupt

The legacy phase interrupt corresponds to the new PWM parameter 1 interrupt. Both interrupt when the PWM output goes active. Both are included in the Summary Interrupt register. Both need to be enabled twice: First in the Summary Enable register and second at the top level by another enable in one of the PIE registers.

7.3 Duty Cycle Interrupt

In the legacy PWM, the duty cycle is independent from the period value. The duty cycle interrupt occurs when the PWM output goes inactive when the timer value equals the duty cycle value.

There is no interrupt identified as the duty cycle interrupt in the new PWM. Instead, the selected mode determines when the output goes inactive at which time an interrupt is generated. This is the equivalent to the duty cycle interrupt in the legacy PWM. The following table shows the new PWM interrupt for each mode that is equivalent to the legacy PWM duty cycle interrupt.

Table 7-1. New PWM Interrupts Equivalent to Legacy PWM Duty Cycle Interrupts

Mode	Equivalent Duty Cycle Interrupt	
	SaP1_out	SaP2_out
Left Aligned	SaP1IF	SaP2IF
Right Aligned	PWMxPIF	PWMxPIF
Center Aligned	P1 Output changed	P2 Output changed
Variable Aligned	N/A	SaP2IF
Pulsed Compare	N/A	N/A
Toggled Compare	N/A	N/A

7.4 Offset Interrupt

The new PWM has no built-in Offset function and therefore no Offset interrupt. However, the new PWM output can be delayed using the External Reset Function (ERS). This replaces the Offset function of the legacy PWM. The peripheral generating the Reset signal may also generate an Offset interrupt. For example, if a CLC is used to hold the PWM in Reset then the CLC falling interrupt would signal the Offset event.

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