USB4624

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB4624. These checklist items should be followed when utilizing the USB4624 in a new design. A summary of these items is provided in Section 10.0, "Hardware Checklist Summary," on page 17. Detailed information on these subjects can be found in the corresponding section:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "USB Signals"
- Section 5.0, "USB Connectors"
- Section 6.0, "Clock Circuit"
- Section 7.0, "Power and Startup"
- Section 8.0, "Configuration Options"
- Section 9.0, "External SPI Memory"

2.0 GENERAL CONSIDERATIONS

2.1 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.2 Ground

- The ground pins, **GND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

2.3 USB-IF-Compliant USB Connectors

- USB-IF-certified USB connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

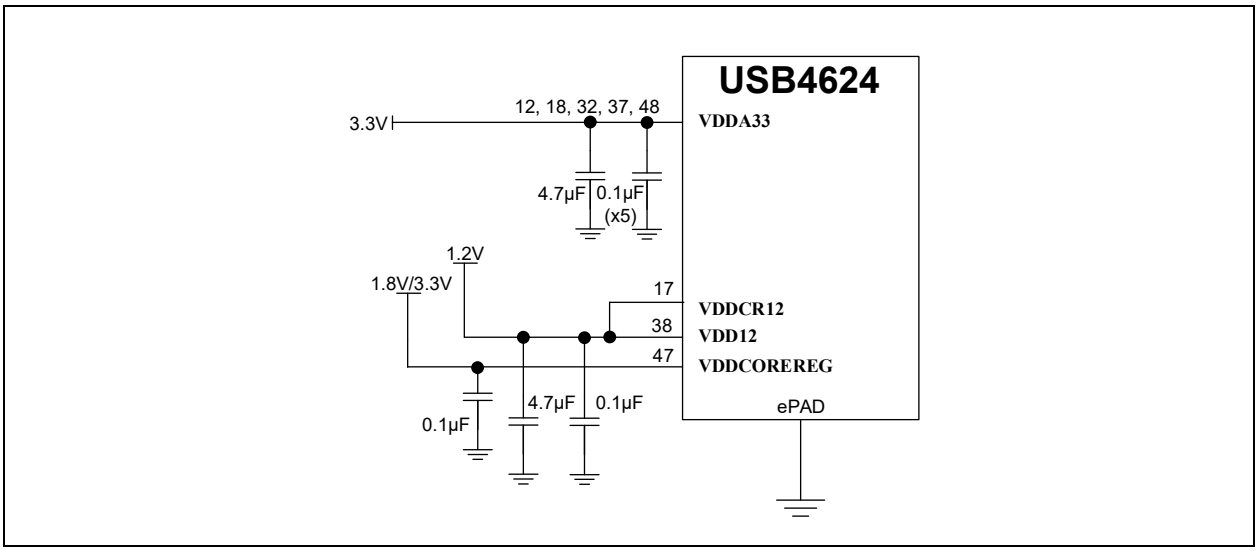
3.0 POWER

- The analog supplies (**VDDA33**) are located on pins 12, 18, 32, 37, and 48. These pins all require a connection to a regulated 3.3V power plane. It is recommended to connect a 0.1 µF capacitor close to each **VDDA33** pin, along with a 1.0 µF bulk capacitance that is shared across all **VDDA33** pins. The capacitor size should be SMD_0603 or smaller.
- The **VDDCOREREG** pin (pin 47) is the input supply to the internal 1.2V regulator. A supply voltage of 1.8V or 3.3V should be connected along with 4.7 µF and 0.1 µF capacitors positioned close to the pin.
- The **VDDCR12** pin (pin 17) supplies power to the core, and it is recommended to include a 1.0 µF capacitor positioned close to this pin. The capacitor size should be SMD_0603 or smaller.
- The **VDD12** pin (pin 38) supplies voltage to the digital HSIC blocks. The design should include a 0.1 µF capacitor positioned close to the pin. The capacitor size should be SMD_0603 or smaller.

  Note: If HSIC is not used, the **VDD12** pin may be optionally left disconnected.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



4.0 USB SIGNALS

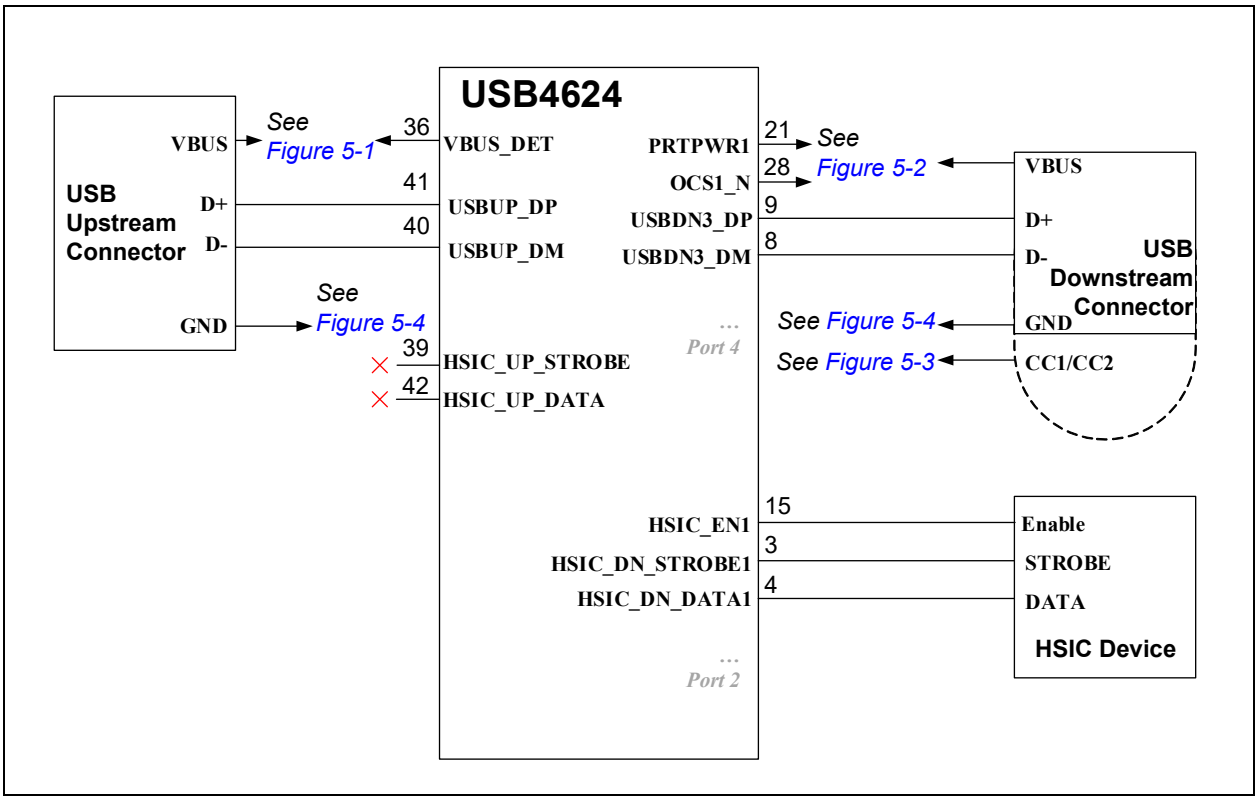
4.1 USB PHY Interface

- **USBUP_DP** (pin 41): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP pin of a USB connector.
- **USBUP_DM** (pin 40): This pin is the negative (–) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM pin of a USB connector.
- **USBDN[3:1]_DP** (pins 4/5/9/11): These pins are the positive (+) signal of the downstream ports 1, 2, 3, and 4 USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. These pins can connect directly to the D+/DP pin of a USB connector.
- **USBDN[3:1]_DM** (pins 3/6/8/10): These pins are the negative (–) signal of the downstream ports 1, 2, 3, and 4 USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. These pins can connect directly to the D–/DM pin of a USB connector.

Note: The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via SMBus/I^{2}C configuration registers.

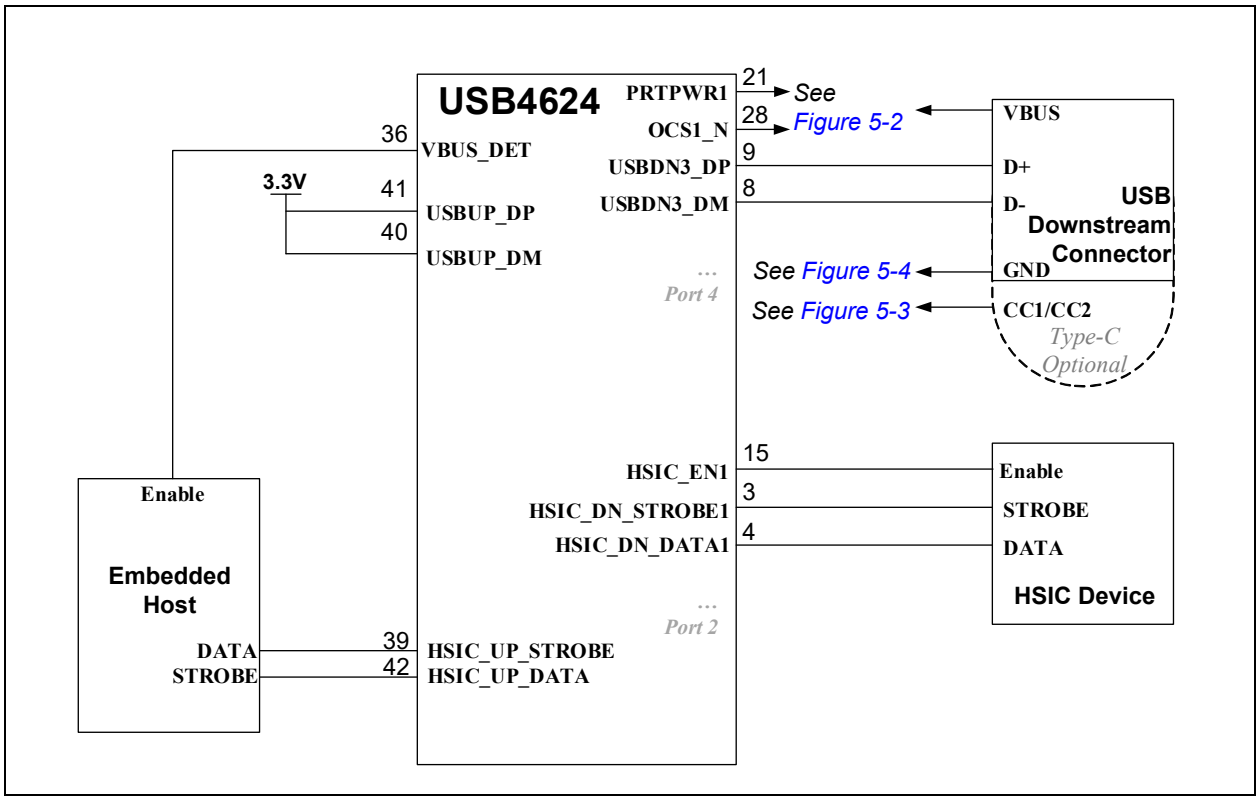
For transmit and receive channel connection details, refer to Figure 4-1.

FIGURE 4-1: USB DATA SIGNAL CONNECTIONS



Note: Downstream ports 3 and 4 have identical schematic implementation requirements; ports 3 and 4 are shown to simplify the figure.

FIGURE 4-2: HSIC UPSTREAM CONNECTIONS (OPTIONAL)



4.1.1 DISABLE DOWNSTREAM PORTS IF UNUSED

If any downstream port of the USB4624 is unused, it should be disabled. This can be achieved through hub configuration (I^2C) or through the port strap disable option by pulling the unused D+ and D– up to 3.3V (directly to 3.3V or through a pull-up resistor).

4.2 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These generally are grouped into three categories:

- TVS protection diodes
  - ESD protection for IEC-61000-4-2 system-level tests
- Application-targeted protection ICs or galvanic isolation devices
  - DC overvoltage protection for short-to-battery protection
- Common-mode chokes
  - For EMI reduction

The USB4624 can be used in conjunction with these types of devices, but it is important to understand the negative effect that these devices may have on USB signal integrity and to select components accordingly and to follow the implementation guidelines from the manufacturer of these devices. The following general guidelines may also be used for implementing these devices:

- Select only devices that are designed specifically for high-speed applications. Per the USB specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry.
- Place these devices as close as possible to the USB connector.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.

- Always ensure a very low impedance path to a large ground plane. The effectiveness of TVS devices depends heavily on effective grounding.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

Note: Microchip PHYBoost configuration options are available for compensating the negative effects of these devices. This feature may help to overcome marginal failures. It is simplest to determine the appropriate setting using lab experiments, such as USB eye diagram tests, on physical hardware.

5.0 USB CONNECTORS

5.1 Upstream Port VBUS and VBUS_DET

The upstream port VBUS line must have no more than 10 µF of total capacitance connected.

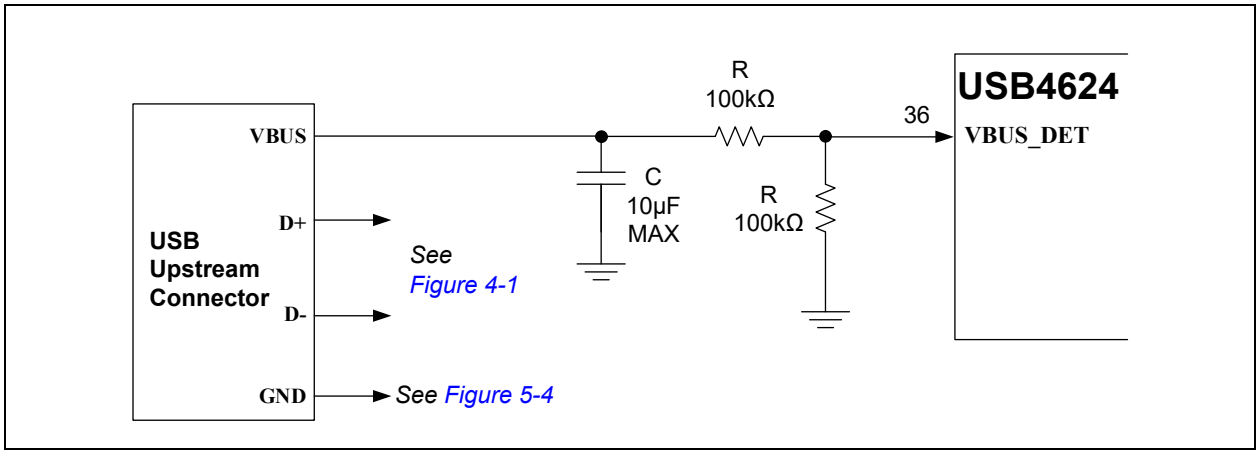
The **VBUS_DET** pin is used by the USB4624 to detect the presence of a USB host. The USB host can also toggle the state of VBUS at any time to force a soft reset and reconnection of the USB4624.

The **VBUS_DET** pin can be tied directly to 3.3V. However, this is not recommended because the ability to force a reset of the hub from the USB host VBUS toggling is lost.

The recommended implementation is shown in Figure 5-1. Note that precise resistor values are not critical and alternate values may be selected as long as:

- The impedance from the **VBUS** pin of the USB connector to the **VBUS_DET** pin is sufficiently high-impedance to minimize pin leakage when VBUS is present before the hub IC is powered on.
- A sufficient voltage level is present on the **VBUS_DET** pin for the full range of VBUS (4.5V-5.5V).

FIGURE 5-1: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS



5.2 Downstream Port VBUS and PRTPWRx/OCSx_N

5.2.1 PRTPWRX

The **PRTPWRx** pin is an output pin that has the following states:

- *PORT OFF*: **PRTPWRx** drives low. The **PRTPWRx** pin only transitions to the PORT ON state through a specific command from the USB host.
- *PORT ON*: **PRTPWRx** drives low. The **PRTPWRx** pin only transitions to the PORT OFF state if:
  - An overcurrent event is sensed on **OCSx_N** pin.
  - A command from the USB host is received, which instructs the hub to disable power.
  - The hub is reset or experiences a POR event.

To ensure minimal BOM cost and simplicity, select a port power controller device with a 3.3V logic level, active-high input. If a device that operates from a 5V logic level is selected, the PRTPWRx signal may need to be boosted using external logic. If a port power controller with active-low input is selected, the PRTPWRx signal must be inverted using external logic.

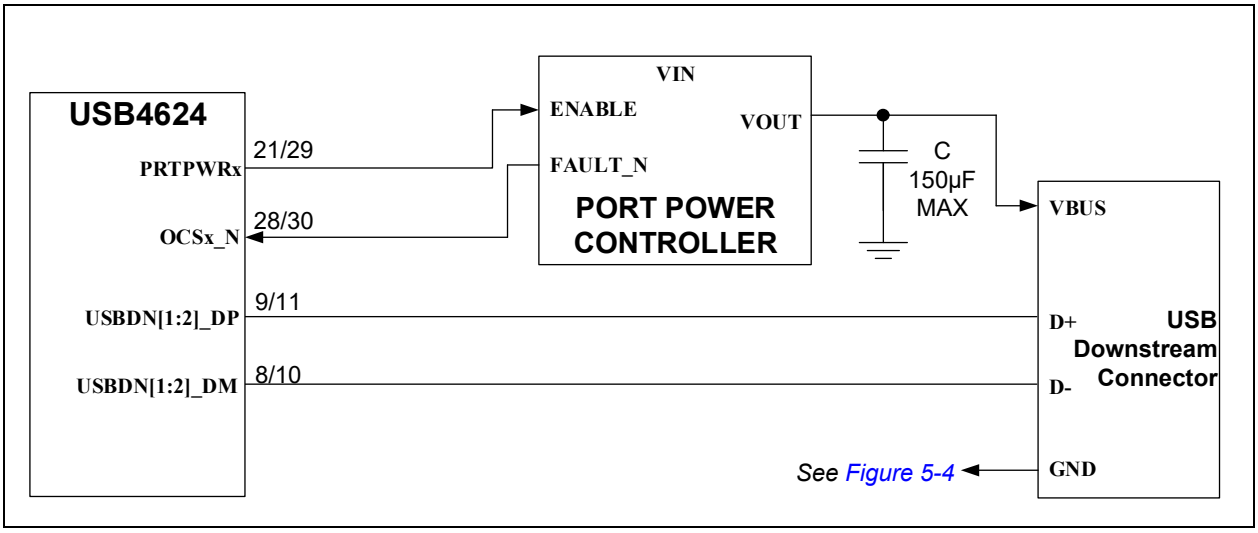
5.2.2 OCSX_N

The **OCSx_N** pin is an input buffer that monitors for overcurrent events. The pin includes an internal pull-up resistor to the 3.3V domain, so an external pull-up resistor is not required. The pin state is ignored when the port is in the PORT OFF state. When the port is in the PORT ON state, an overcurrent event is detected if the state of the pin is detected as low (below the V_{ILI} voltage). When an overcurrent event is detected, the port automatically moves to the PORT OFF state until the USB host can be notified of the overcurrent event.

To ensure minimal BOM cost and simplicity, select a port power controller device with an active-low, open- drain fault indicator output. If a port power controller with active-high fault indicator output is selected, the OCSx_N signal must be inverted using external logic.

A typical VBUS port power controller implementation is shown in Figure 5-2.

FIGURE 5-2: DOWNSTREAM VBUS AND PRTCTL1 CONNECTIONS



Note: The implementation as shown in Figure 5-2 assumes that the port power controller has an active-high Enable input, and an active-low, open-drain style fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

5.3 Downstream Port Type-C Support

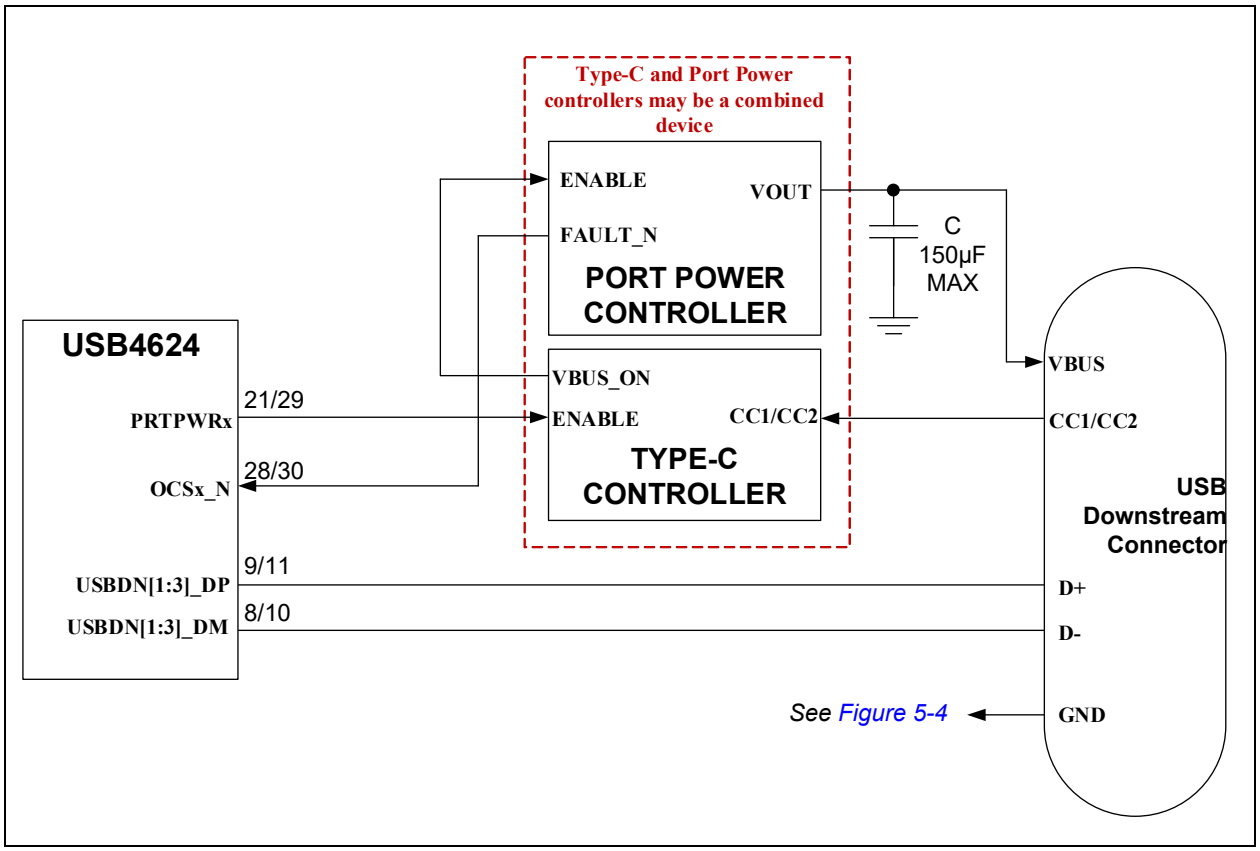
USB4624 may be used with Type-C as the downstream port. This requires a Type-C port controller or combined port power controller and Type-C port controller. The USB4624 simply controls the Type-C port controller in same way it would control a standard Type-A port power controller. The USB4624 does not require any kind of Type-C port status information from the Type-C port controller.The PRTPWRx signal should be connected to an Enable pin on the Type-C controller, and the OCSx_N signal should connect to the fault indicator output of the port power controller.

If the Type-C controller and the port power controller are separate devices, the Type-C controller must control the Enable pin of the port power controller. The **PRTPWRx** pin should not directly control the VBUS enable signal of the port power controller.

A Type-C controller may be configured to signal a 500 mA, 1.5A, or 3.0A port power capability. The selected port power controller should be sized accordingly.

A typical implementation is shown in Figure 5-3.

FIGURE 5-3: DOWNSTREAM VBUS AND PRTCTL1 CONNECTIONS WITH TYPE-C PORT



Note: The implementation as shown in Figure 5-3 assumes that the Type-C controller has an active-high Enable input, and the port power controller has an active-low, open-drain style fault indicator. External polarity inversion through buffers or FETs may be required if the Type-C controller and/or port power controller has different I/O characteristics.

5.4 GND and EARTH Recommendations

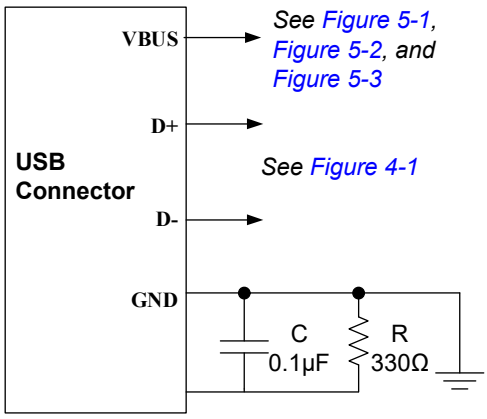
The GND pins of the USB connector must be connected to the PCB with a low impedance path directly to a large GND plane.

The EARTH pins of the USB connector may be connected in one of two ways:

- (*Recommended*) To GND through a resistor and capacitor in parallel. An RC filter can help to decouple and minimize EMI between a PCB and a USB cable.
- Directly to the GND plane.

The recommended implementation is shown in Figure 5-4.

FIGURE 5-4: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS



6.0 CLOCK CIRCUIT

6.1 Crystal and External Clock Connection

A 24.000 MHz (±350 ppm) reference clock is the source for the USB interface and for all other functions of the device. For exact specifications and tolerances, refer to the latest revision of the *USB4624 Data Sheet*.

- **XTAL1/REFCLK** (pin 44) is the clock circuit input for the USB4624. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XTAL2** (pin 43) is the clock circuit output for the USB4624. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- A 1 megohm resistor (1MΩ) is required to be connected across the **XTAL1** and **XTAL2** pins. Failure to place this resistor will result in an unstable crystal operation.
- The crystal loading capacitor values are system-dependent, based on the total C_L specification of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly used formula for calculating the appropriate physical C_1 and C_2 capacitor values is:

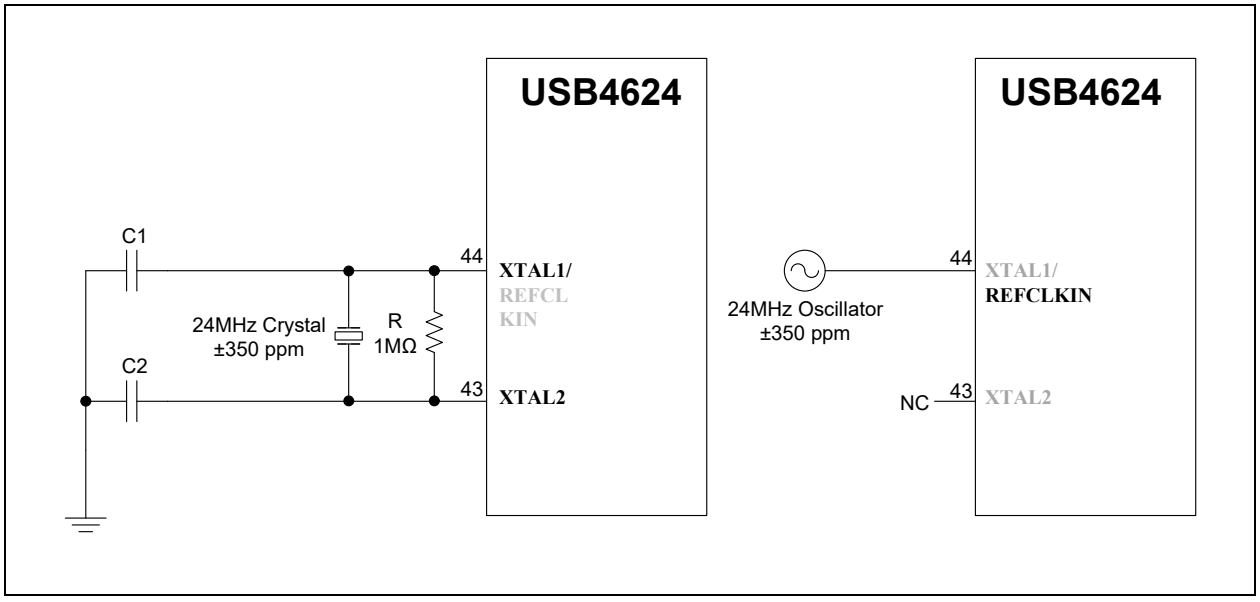
  $C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$

  Where: C_L is the specification from the crystal data sheet, $C_{X1} = C_{stray} + C_1$, $C_{X2} = C_{stray} + C_2$

  Note: C_{stray} is the stray/parasitic capacitance due to PCB layout. It can be assumed to be very small, in the 1-2 pF range, and then verified by physical experiments in the lab if PCB simulation tools are not available.

- Alternately, a 24.000 MHz, 1.2V-3.3V clock oscillator may be used to provide the clock source for the USB4624. When using a single-ended clock source, **XTAL2** should be left floating as a No Connect (NC).

FIGURE 6-1: CRYSTAL AND OSCILLATOR CONNECTIONS



7.0 POWER AND STARTUP

7.1 RBIAS Resistor

RBIAS (pin 46) on the USB4624 must connect to ground through a 12 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the internal circuitry. This should be placed as close as possible to the IC pin, and be given a dedicated, low-impedance path to a ground plane.

7.2 Board Power Supplies

7.2.1 POWER RISE TIME

The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *USB4624 Data Sheet*.

If a monotonic/fast power rail rise cannot be assured, then the RESET_N signal should be controlled by a reset supervisor and only released when the power rail has reached a stable level.

7.2.2 CURRENT CAPABILITY

It is important to size the 5V and 3.3V power rails appropriately. The 5V power supply must be capable of supplying sufficient power for all exposed USB ports concurrently without drooping below the minimum voltage permissible in the USB specification:

- 500 mA per-port for USB2 ports
- 1.5A or 3.0A per Type-C port (depending on setting of the Type-C controller)

The 3.3V power supply must be able to supply enough power to the USB hub IC. It is recommend that 3.3V power rail be sized such that is able to supply the maximum power consumption specification as described in the *USB4624 Data Sheet*.

7.3 Reset Circuit

RESET_N (pin 35) is an active-low reset input. This signal resets all logic and registers within the USB4624. A hardware reset (RESET_N assertion) is not required following power-up. Please refer to the latest copy of the *USB4624 Data Sheet* for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the USB4624 when reset is triggered by the power supply. The values for the “R” resistor and “C” capacitor are not critical and may be adjusted per individual system needs or preferences.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

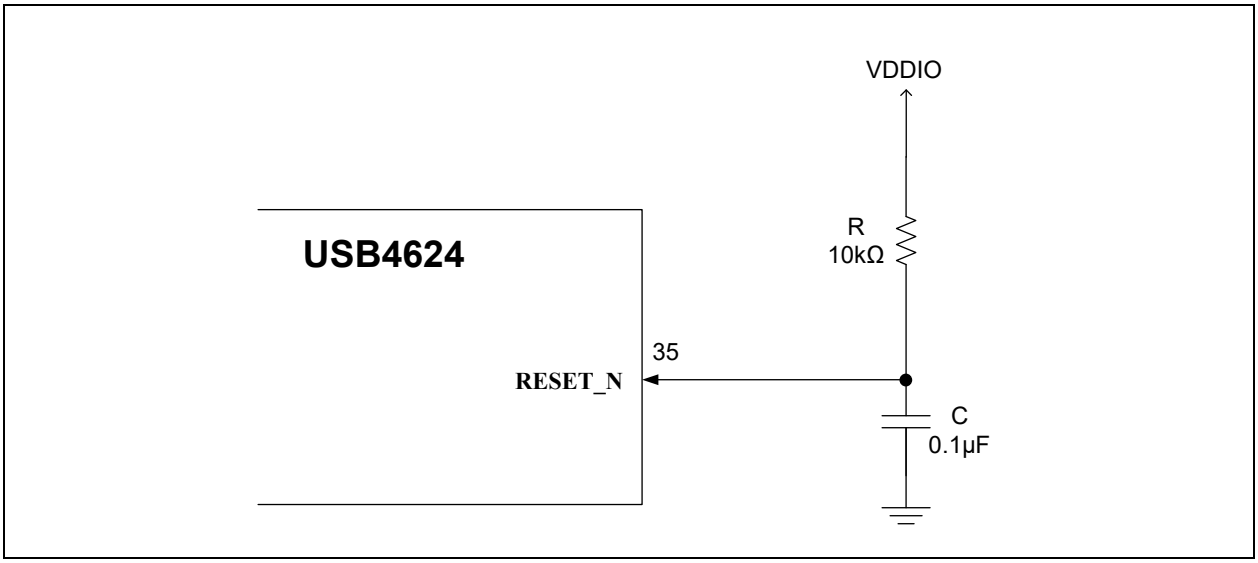
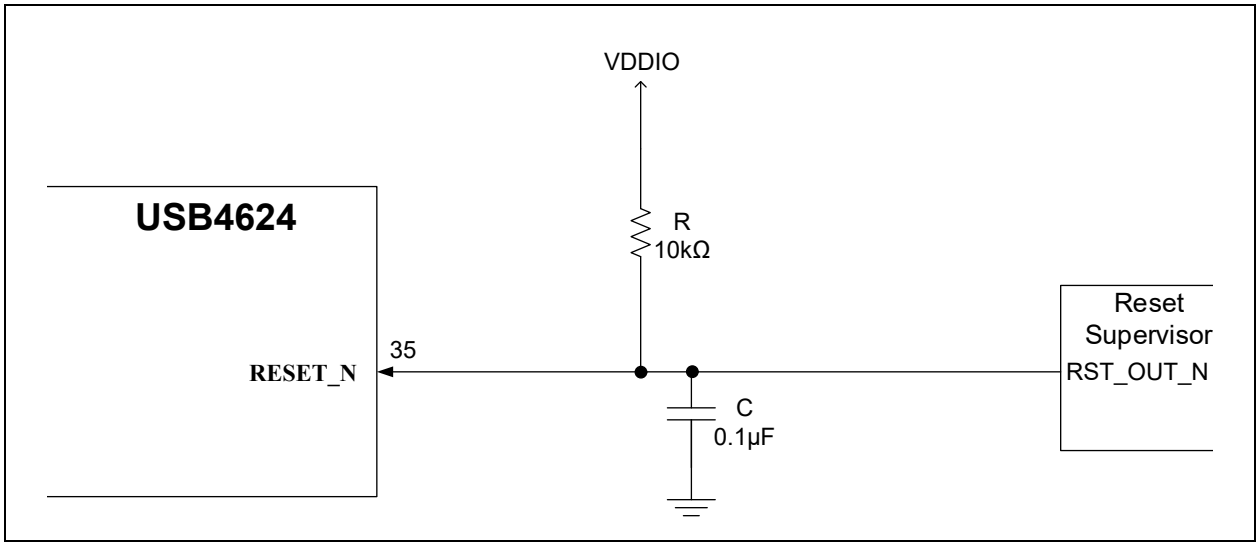


Figure 7-2 details the recommended reset circuit for applications where reset is driven by an external CPU/MCU. The reset out pin (**RST_OUT_N**) from the CPU/MCU provides the warm reset after power-up. The values for the “R” resistor and “C” capacitor are not critical and may be adjusted per individual system needs or preferences.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT



8.0 CONFIGURATION OPTIONS

The USB4624 can be configured in one of three ways:

- EEPROM memory device
- SMBus (via external MCU/SoC)
- Defaults + Hardware Resistor Strap Modifiers (resistor pull-down/pull-up options)

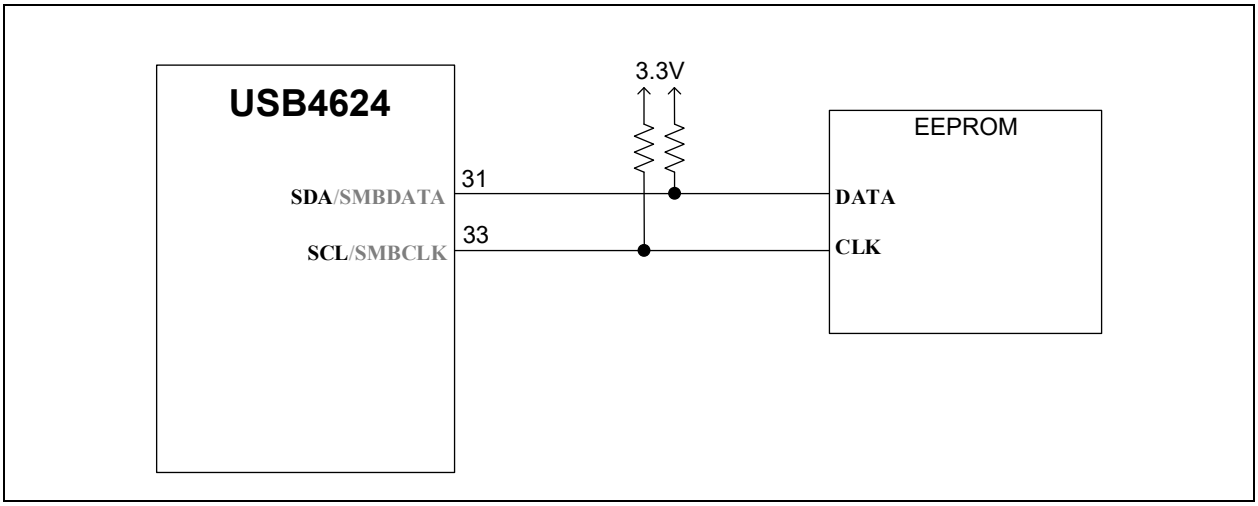
The hub must be configured completely via EEPROM or SMBus. A combined/hybrid approach is not supported.

8.1 Configuration via EEPROM

When configuring via EEPROM, the USB4624 operates as an I^2C master at a fixed 58.6 kHz speed. The EEPROM must be 256x8 and contain the entire register set from 0x00 to 0xFF must be replicated in the EEPROM device. The default values should be obtained from the *USB4624 Data Sheet*.

Note: The EEPROM device must be programmed on board or preprogrammed before PCB assembly. The USB4624 does not have a programming/USB pass-through mechanism.

FIGURE 8-1: RECOMMENDED CONNECTIONS IF CONFIGURED VIA EEPROM



8.2 Configuration via MCU/SoC Memory

8.2.1 MCU/SOC OPERATION SUMMARY

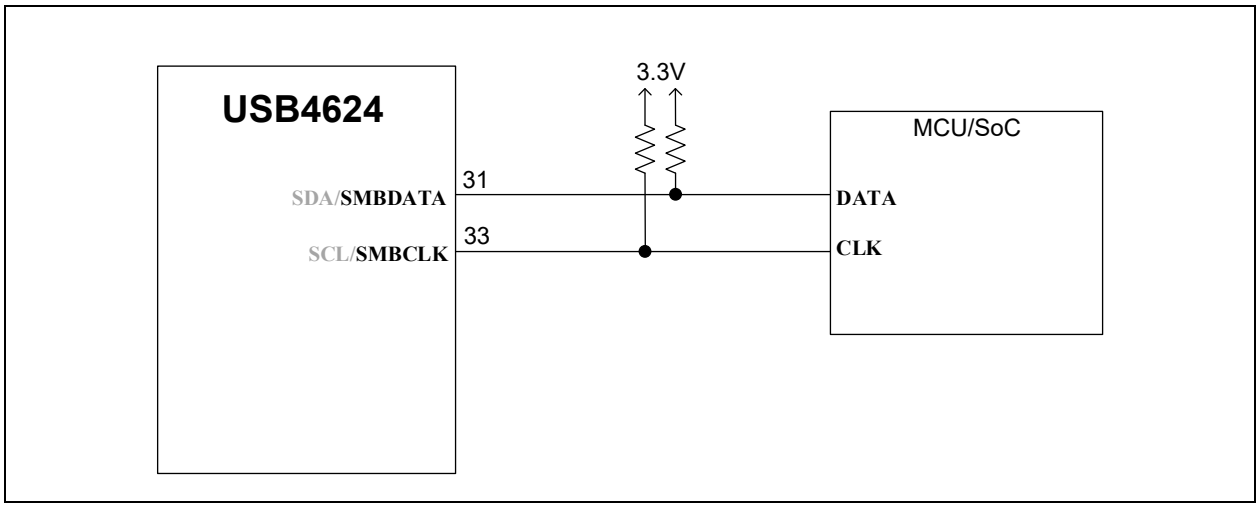
By default, the USB4624 executes based on internal register defaults and an external MCU/SoC device is not explicitly required. If settings that differ from the internal defaults are required by the application, an external MCU/SoC may be used to modify the register settings. Only specific settings that need to be modified from the default must be changed.

The USB4624 supports only one address option: 010_1100b.

8.2.2 MCU/SOC CONNECTION DIAGRAMS

The recommended schematic connections for an MCU/SoC memory device are shown in Figure 8-2.

FIGURE 8-2: RECOMMENDED CONNECTIONS IF CONFIGURED VIA MCU/SOC



8.3 Non-Removable Port Settings

In a typical USB4624 application, downstream ports are routed to a user-accessible USB connector, and hence the downstream port should be configured as a removable port.

The following guidelines can be used to determine which setting to use:

- If the port is routed to a user-accessible USB connector, it is *removable*.
- If the port is routed to a permanently-attached and embedded USB device on the same PCB, or non-user-accessible wiring or cable harness, it is *non-removable*.

The removable/non-removable device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors, which the USB host may use to understand if a port is a user-accessible port, or if the device is a permanently-attached device. Under standard operating conditions, the USB host may or may not modify its operation based upon this information. Certain USB compliance tests are impacted by this setting, so designs that must undergo USB compliance testing and certification must ensure the configuration settings are correct.

Removable port settings can be configured via:

- EEPROM
- I^2C-based MCU/SoC
- Hardware strap options

8.4 Self-Powered/Bus-Powered Settings (Available via SMBus Configuration Only)

In a typical USB4624 application, the hub should be configured as self-powered, which is the default configuration setting.

The following guidelines can be used to determine which setting to use:

- If the entire system (hub included) is powered completely from the Upstream USB connector's **VBUS** pin, and the system is designed to operate using standard USB cabling and any standard USB host, then the hub system is *bus-powered*.
- If the entire system (hub included) is always powered by a separate power connector, then the hub system is *self-powered*.
- If the hub included is part of a larger embedded system with fixed cabling and a fixed USB host, then the hub system is most likely *self-powered* (even if all of the power is derived from the upstream USB connector's **VBUS** pin).

Note: The self-powered/bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors, which the USB host will use to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub and all of

its downstream ports must continue to operate within that 500 mA budget. A USB host will typically limit the downstream ports of a self-powered hub to 100 mA. Any device that connects to a self-powered hub which declares it needs more than 100 mA will be prevented from operating by the USB host.

8.5 Port Disable Straps

If using the port disable strap option, the **USBDP_DNx** and **USBDM_DNx** signals should be pulled high to 3.3V. This connection can be made directly to the 3.3V power net or through a pull-up resistor. The pins may also be shorted together as well to simply layout.

Note: Both USB D+ and D– signals must be pulled high to effectively disable the port. If only one pin is pulled to 3.3V, the port will not be disabled.

8.6 PortSwap

The PortSwap straps allow an end system integrator to swap the polarity of each downstream port individually. This may help to resolve PCB layout issues that would otherwise require cross-overs to correct. Cross-overs usually require one signal of the differential pair to transition to another PCB layer and back, which causes a discontinuity in differential impedance and trace length mismatches that will negatively impact signal integrity.

9.0 EXTERNAL SPI MEMORY

9.1 SPI Operation Summary

By default, the USB4624 executes firmware from an internal read only memory (ROM). The USB4624 supports optional firmware execution from an external SPI Flash device. An SPI Flash device is only required if a custom firmware is required for the application.

The SPI interface can operate at 60 MHz or 30 MHz, and can operate in Dual mode or Quad mode.

The firmware image can be executed in one of two ways:

- *Execute in place:* The firmware is continuously executed directly from the SPI Flash device, and the interface is constantly active.
- *Execute in internal SRAM:* The firmware is loaded into the hub's internal SRAM and executed internally. This may only be supported if the firmware image is smaller than the hub's SRAM size.

  Note: All firmware images are developed, compiled, tested, and provided by Microchip. The SPI interface speed is an OTP-configurable option and only speeds that were specifically tested with the firmware image should be selected. The execution method is configured with the firmware image itself and cannot be changed via configuration.

9.2 Compatible SPI Flash Devices

Microchip recommends SST-brand SPI Flash devices. Microchip has verified compatibility of the following list of SPI Flash devices:

- SST26VF016B
- SST26VF032B
- SST26VF064B
- SST25VF064C
- AT25SF041
- AT26DF081

Other SPI Flash devices may be used, provided that they meet the following minimum requirements:

- Operation at 30 MHz or 60 MHz
- Mode 0 or mode 3
- Memory of 256 kB or larger
- Utilization of the same OpCode commands as with the above list of compatible devices
- Dual mode or Quad mode operation

10.0 HARDWARE CHECKLIST SUMMARY

TABLE 10-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.2, "Ground"	Verify that the grounds are tied together.		
	Section 2.3, "USB-IF-Compliant USB Connectors"	Verify if USB-IF-compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power"	Section 3.0, "Power"	Ensure that **VDD33** is in the range 3.0V to 3.6V, 0.1 µF capacitors are connected to pins 1 and 18, and a 1.0 µF capacitor is connected to pin 9.		
Section 4.0, "USB Signals"	Section 4.1, "USB PHY Interface"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines.		
	Section 4.2, "USB Protection"	Verify that ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB trace.		
Section 5.0, "USB Connectors"	Section 5.1, "Upstream Port VBUS and VBUS_DET"	Verify that the upstream port VBUS has no more than 10 µF capacitance and that the VBUS signal is properly divided down to a 3.3V signal and connected to the **VBUS_DET** pin of the hub.		
	Section 5.2, "Downstream Port VBUS and PRTPWRx/OCSx_N"	If the downstream ports are standard Type-A ports, verify that **PRTPWRx** and **OCSx_N** are properly connected to the Enable pin of the downstream port power controller and the fault indicator output of the port power controller.		
	Section 5.3, "Downstream Port Type-C Support"	If the downstream ports are standard Type-C ports, verify that **PRTPWRx** is properly connected to the Enable pin of the Type-C port controller, and **OCSx_N** is connected to the fault indicator output of the port power controller.		
	Section 5.4, "GND and EARTH Recommendations"	Verify that the USB connector is properly connected to PCB ground on both the **GND** pins and the **SHIELD** pins. It is recommended that an RC filter be placed between the **SHIELD** pins and PCB ground.		
Section 6.0, "Clock Circuit"	Section 6.1, "Crystal and External Clock Connection"	Confirm that the crystal or clock is 24.000 MHz (±350 ppm). If a single-ended clock is used, ensure it is connected to **XTAL1** while leaving **XTAL2** floating. If a crystal is used, ensure that the loading capacitors are appropriately sized for the crystal loading requirement.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 7.0, "Power and Startup"	Section 7.1, "RBIAS Resistor"	Confirm that a 12.0 kΩ 1% resistor is connected between the **RBIAS** pin and PCB ground.		
	Section 7.2, "Board Power Supplies"	Verify that the board power supplies deliver 3.0V-3.6V to the hub power rails, and that the power-on rise time meets the requirement of the hub as defined in the data sheet. If the rise time requirement cannot be met, ensure that the **RESET_N** line is held low until the power regulators reach a steady state.		
	Section 7.3, "Reset Circuit"	Ensure that the RESET_N signal has an external pull-up resistor, or is otherwise properly controlled by an external SoC, MCU, or Reset supervisor device.		
Section 8.0, "Configuration Options"	Section 8.1, "Configuration via EEPROM"	If configuring via EEPROM, ensure that EEPROM is connected to the correct pins and that CFG_SEL0, CFG_SEL1, and CFG_SEL2 are strapped correctly.		
	Section 8.2, "Configuration via MCU/SoC Memory"	If configuring via SoC/MCU, ensure that MCU/SoC is connected to the correct pins and that CFG_SEL0, CFG_SEL1, and CFG_SEL2 are strapped correctly.		
	Section 8.3, "Non-Removable Port Settings"	For all ports that do not route to user-exposed USB connectors, ensure that the port is configured to be non-removable via EEPROM, MCU/SoC, or hardware strap.		
	Section 8.4, "Self-Powered/Bus-Powered Settings (Available via SMBus Configuration Only)"	Ensure that self-powered/bus-powered settings are correct, and that hardware is designed appropriately. For self-powered applications, all power for the board is derived from an external power supply. For bus-powered applications, all power for the board is derived from VBUS sourced by the connected USB host.		
	Section 8.5, "Port Disable Straps"	If any USB ports are unused, ensure that they are properly disabled by either strapping D+ and D– to 3.3V in hardware, or disabled via EEPROM or MCU/SoC.		
	Section 8.6, "PortSwap"	If using the USB PortSwap feature, ensure that USB signal polarity is swapped in the schematic design for each port that is configured to enable PortSwap.		
Section 9.0, "External SPI Memory"	Section 9.1, "SPI Operation Summary"	Determine if a custom SPI FW image is required and which mode of operation the selected SPI Flash device must support.		
	Section 9.2, "Compatible SPI Flash Devices"	Ensure that the selected SPI Flash device is compatible with the hub.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004696A (08-09-22)	Initial release	

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